CA3260, CA3260A

4MHz, BiMOS Operational Amplifier with MOSFET Input/CMOS Output

November 1996

Features

- **MOSFET Input Stage provides**
  - **Very High Z_I = 1.5TΩ (1.5 x 10^{12}Ω) (Typ)**
  - **Very Low I_I = 5pA (Typ) at 15V Operation**
    = 2pA (Typ) at 5V Operation
- **Ideal for Single Supply Applications**
- **Common Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can be Swung 0.5V Below Negative Supply Rail**
- **CMOS Output Stage Permits Signal Swing to Either (Or Both) Supply Rails**

Applications

- **Ground Referenced Single Supply Amplifiers**
- **Fast Sample-Hold Amplifiers**
- **Long Duration Timers/Monostables**
- **Ideal Interface with Digital CMOS**
- **High Input Impedance Wideband Amplifiers**
- **Voltage Followers (e.g. Follower for Single Supply D/A Converter)**
- **Voltage Regulators (Permits Control of Output Voltage Down to 0V)**
- **Wien Bridge Oscillators**
- **Voltage Controlled Oscillators**
- **Photo Diode Sensor Amplifiers**

Description

CA3260A and CA3260 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA3260 series circuits are dual versions of the popular CA3160 series.

Gate protected P-Channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute in single supply applications.

A complementary symmetry MOS (CMOS) transistor pair, capable of swinging the output voltage to within 10mV of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

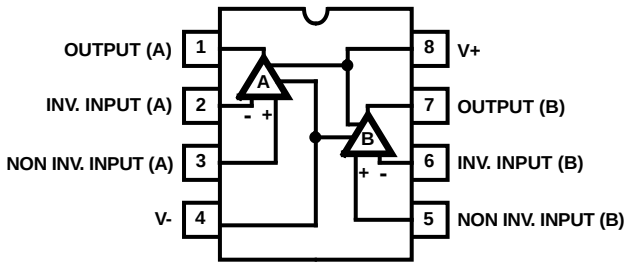
The CA3260 Series circuits operate at supply voltages ranging from 4V to 16V, or ±2V to ±8V when using split supplies. The CA3260A offers superior input characteristics over those of the CA3260.

Ordering Information

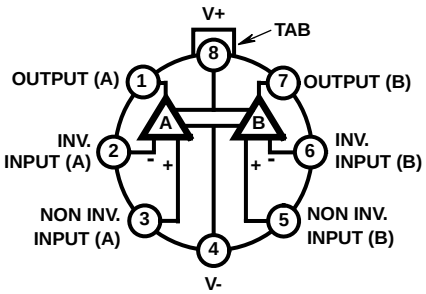
PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
CA3260E	-55 to 125	8 Ld PDIP	E8.3
CA3260T	-55 to 125	8 Pin Metal Can	T8.C
CA3260AE	-55 to 125	8 Ld PDIP	E8.3
CA3260AT	-55 to 125	8 Pin Metal Can	T8.C

Pinouts

CA3260, CA3260A (PDIP)
TOP VIEW



CA3260, CA3260A (METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1266.3**

Absolute Maximum Ratings

DC Supply Voltage (V+ to V-) 16V
DC Input Voltage . . . . . (V+ +8V) to (V- -0.5V)
Differential Input Voltage. 8V
Input Terminal Current 1mA
Output Short Circuit Duration (Note 1) . . . . . Indefinite

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	100	N/A
Metal Can Package	165	75

Maximum Junction Temperature (Metal Can Package) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$, Typical Values Intended Only for Design Guidance

PARAMETER		SYMBOL	TEST CONDITIONS	TYPICAL VALUES		UNITS
				CA3260A	CA3260	
Input Resistance		R_I	$V_S = \pm 7.5V$	1.5	1.5	TΩ
Input Capacitance		C_I	f = 1MHz, $V_S = \pm 7.5V$	4.3	4.3	pF
Unity Gain Crossover Frequency		f_T	$V_S = \pm 7.5V$	4	4	MHz
Slew Rate		SR	$V_S = \pm 7.5V$	10	10	V/µs
Transient Response	Rise Time	t_r	C_L = 25pF, R_L = 2kΩ, A_V = +1, $V_S = \pm 7.5V$	0.09	0.09	µs
	Overshoot	OS		10	10	%
Settling Time (to <0.1%, $V_{IN} = 4V_{P-P}$)		t_S	C_L = 25pF, R_L = 2kΩ, A_V = +1, $V_S = \pm 7.5V$	1.8	1.8	µs
Input Offset Voltage		V_{IO}	V+ = 5V, V- = 0V	2	6	mV
Input Offset Current		I_{IO}	V+ = 5V, V- = 0V	0.1	0.1	pA
Input Current		I_I	V+ = 5V, V- = 0V	2	2	pA
Common Mode Rejection Ratio		CMRR	V+ = 5V, V- = 0V	70	60	dB
Large Signal Voltage Gain		A_{OL}	$V_O = 4V_{P-P}$, R_L = 20kΩ, V+ = 5V, V- = 0V	100	100	kV/V
				100	100	dB
Common Mode Input Voltage Range		V_{ICR}	V+ = 5V, V- = 0V	0 to 2.5	0 to 2.5	V
Supply Current		I+	V_O = 5V, $R_L = \infty$, V+ = 5V, V- = 0V	1	1	mA
			V_O = 2.5V, $R_L = \infty$, V+ = 5V, V- = 0V	1.2	1.2	mA
Power Supply Rejection Ratio		PSRR	$\Delta V_{IO}/\Delta V+$, V+ = 5V, V- = 0V	200	200	µV/V

Electrical Specifications For Each Amplifier at $T_A = 25^oC$, V+ = 15V, V- = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA3260A			CA3260			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$\|V_{IO}\|$	$V_S = \pm 7.5V$	-	2	5	-	6	15	mV
Input Offset Current	$\|I_{IO}\|$	$V_S = \pm 7.5V$	-	0.5	20	-	0.5	30	pA
Input Current	I_I	$V_S = \pm 7.5V$	-	5	30	-	5	50	pA
Large Signal Voltage Gain	A_{OL}	$V_O = 10V_{P-P}$, R_L = 10kΩ	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Common Mode Rejection Ratio	CMRR		80	95	-	70	90	-	dB

Electrical Specifications For Each Amplifier at $T_A = 25^oC$, V+ = 15V, V- = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	CA3260A			CA3260			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Common Mode Input Voltage Range	V_{ICR}		0	-0.5 to 12	10	0	-0.5 to 12	10	V
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V+$ V+ = 17.5V	-	32	150	-	32	320	µV/V
Maximum Output Voltage	$V_{OM}+$	R_L = 10kΩ	11	13.3	-	11	13.3	-	V
	$V_{OM}-$		-	0.002	0.01	-	0.002	0.01	V
	$V_{OM}+$	$R_L = \infty$	14.99	15	-	14.99	15	-	V
	$V_{OM}-$		-	0	0.01	-	0	0.01	V
Maximum Output Current	$I_{OM}+$ Source	V_O = 7.5V	12	22	45	12	22	45	mA
	$I_{OM}-$ Sink		12	20	45	12	20	45	mA
Total Supply Current	I+	$R_L = \infty$							
V_O (Amplifier A) = 7.5V V_O (Amplifier B) = 7.5V			-	9	15.5	-	9	15.5	mA
V_O (Amplifier A) = 0V V_O (Amplifier B) = 0V			-	1.2	3	-	1.2	3	mA
V_O (Amplifier A) = 0V V_O (Amplifier B) = 7.5V			-	5	8.5	-	5	8.5	mA
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		-	6	-	-	8	-	µV/°C
Crosstalk		f = 1kHz	-	120	-	-	120	-	dB

Schematic Diagram