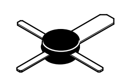
The RF Line
NPN Silicon
RF Low Power Transistor

MRF553

Designed primarily for wideband large signal predriver stages in the VHF frequency range.

- Specified @ 12.5 V, 175 MHz Characteristics
  Output Power = 1.5 W
  Minimum Gain = 11.5 dB
  Efficiency 60% (Typ)
- Cost Effective PowerMacro Package
- Electroless Tin Plated Leads for Improved Solderability
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

1.5 W, 175 MHz
RF LOW POWER
TRANSISTOR
NPN SILICON



CASE 317D–02, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Device Dissipation @ T_C = 75°C (1, 2) Derate above 75°C	P_D	3.0 40	Watts mW/°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	$R_{\theta JC}$	25	°C/W

ELECTRICAL CHARACTERISTICS (T$_A$ = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	30	—	200	—

(continued)

NOTES:
1. T_C, Case temperature measured on collector lead immediately adjacent to body of package.
2. The MRF553 PowerMacro must be properly mounted for reliable operation. AN938, “Mounting Techniques in PowerMacro Transistor,” discusses methods of mounting and heatsinking.

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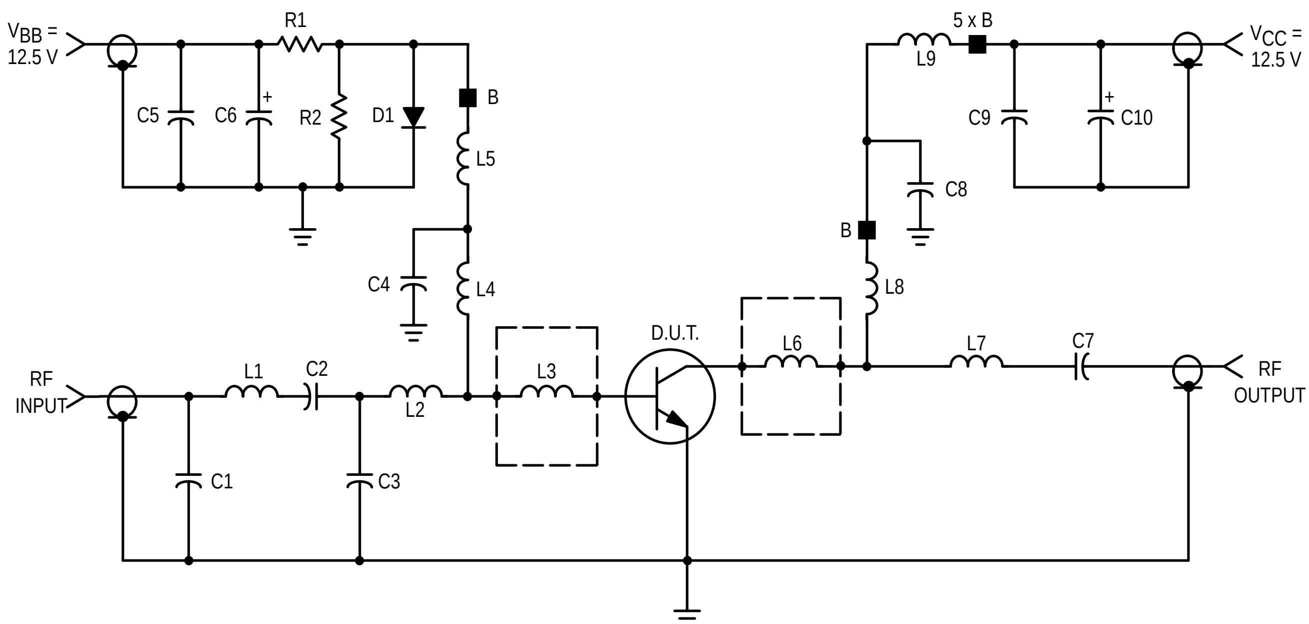
ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	—	12	20	pF
FUNCTIONAL TESTS						
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 175 MHz)	Figures 1, 2	G_{pe}	11.5	13	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 175 MHz)	Figures 1, 2	η	50	60	—	%
Load Mismatch Stress (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 175 MHz, VSWR ≥ 10:1 All Phase Angles)		ψ	No Degradation in Output Power			—



C1 — 36 pF Mini Underwood
C2 — 47 pF Mini Underwood
C3 — 91 pF Mini Underwood
C4 — 68 pF Mini Underwood
C5, C9 — 1.0 µF Erie Red Cap Capacitor
C6, C10 — 0.1 µF, 35 V Tantulum
C7 — 470 pF Chip Capacitor
C8 — 2200 pF Chip Capacitor
R1 — 4.7 kΩ, 1/4 W
R2 — 100 Ω, 1/4 W
D1 — 1N4148 Diode

L1 — 3 Turns, #18 AWG, 0.210″ ID, 3/16″ Length
L2, L4, L7 — 0.62″, #18 AWG Wire Bent into “V”
L3, L6 — 60 x 125 x 250 Mils Copper Pad on 27 Mils Thick Alumina Substrate
L5 — 12 µH Molded Choke
L8 — 7 Turns, #18 AWG, 0.170″ ID, 7/16″ Length
L9 — 1.0″, #18 AWG Wire with 5 Ferrite Beads
B — Ferrite Bead
Board Material — Glass Teflon, ε_r = 2.56, t = 0.0625″

Figure 1. 140–175 MHz Broadband Circuit Schematic

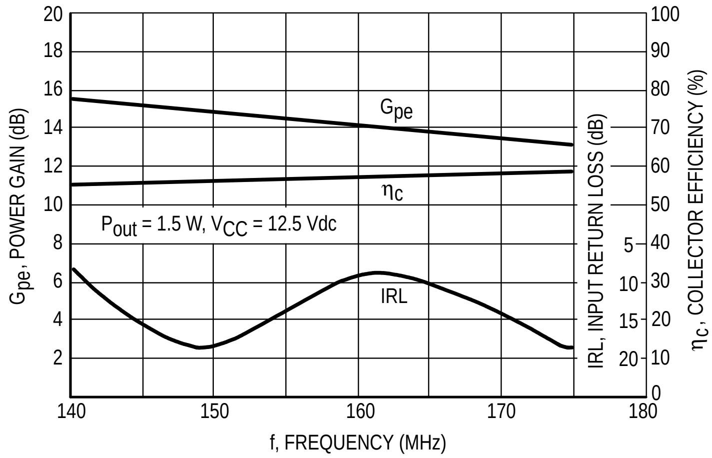


Figure 2. Typical Performance in Broadband Circuit

f Frequency MHz	Z_{in} Ohms						Z_{OL}* Ohms					
	V_{CC} = 7.5 V; P_{in}			V_{CC} = 12.5 V; P_{in}			V_{CC} = 7.5 V; P_{out}			V_{CC} = 12.5 V; P_{out}		
	100 mW	**200 mW**	**300 mW**	**50 mW**	**100 mW**	**150 mW**	**1.0 W**	**1.6 W**	**2.2 W**	**1.1 W**	**2.0 W**	**2.6 W**
140	1.65–j3.6	2.0–j2.6	2.3–j1.2	1.7–j4.1	1.8–j3.1	1.9–j2.7	9.9–j11.1	10.6–j5.1	10–j4.9	28.3–j21.5	16–j20.5	16.3–j16.5
175	2.5–j5.6	2.3–j5.9	2.8–j4.0	2.3–j4.6	2.4–j1.2	2.4–j5.7	12.1–j14.9	7.2–j9.8	8.1–j5.4	30.8–j23.3	11.4–j20.9	11.1–j14.3

f Frequency MHz	Z_{in} Ohms						Z_{OL}* Ohms					
	V_{CC} = 7.5 V; P_{in}			V_{CC} = 12.5 V; P_{in}			V_{CC} = 7.5 V; P_{out}			V_{CC} = 12.5 V; P_{out}		
	50 mW	**100 mW**	**200 mW**	**25 mW**	**50 mW**	**100 mW**	**1.25 W**	**1.5 W**	**2.0 W**	**1.5 W**	**2.25 W**	**3.0 W**
90	2.5–j9.3	2.5–j6.4	2.5–j4.4	1.6–j10.7	2.5–j7.1	2.2–j1.3	31.8–j9.2	32–j8.9	30.2–j10.7	45.8–j7.2	45.2–j3.9	40–j4.5

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Table 1. Z_{in} and Z_{OL} versus Collector Voltage, Input Power, and Output Power

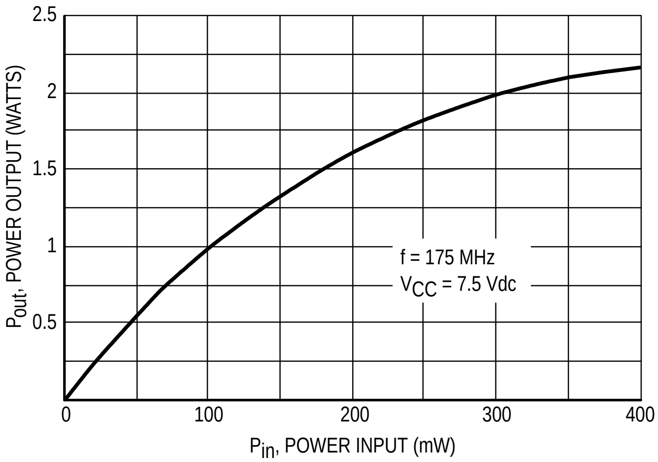


Figure 3. Power Output versus Power Input

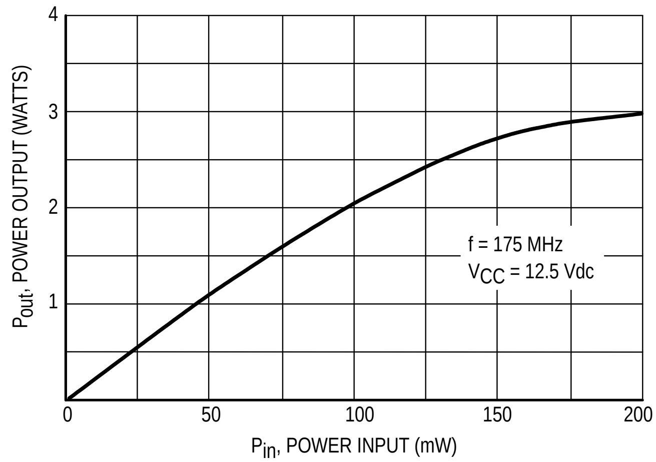


Figure 4. Power Output versus Power Input

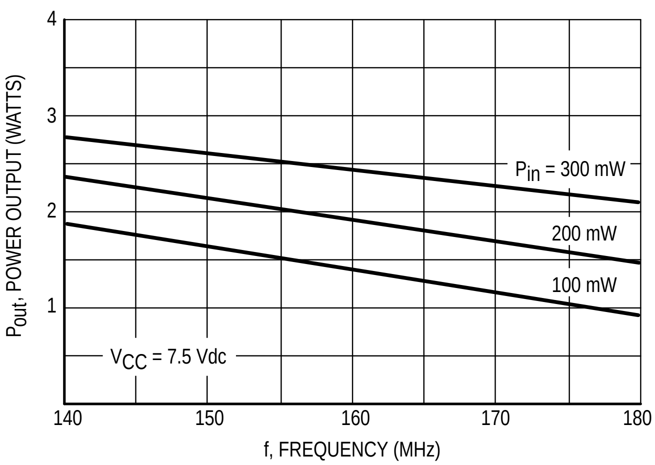


Figure 5. Power Output versus Frequency

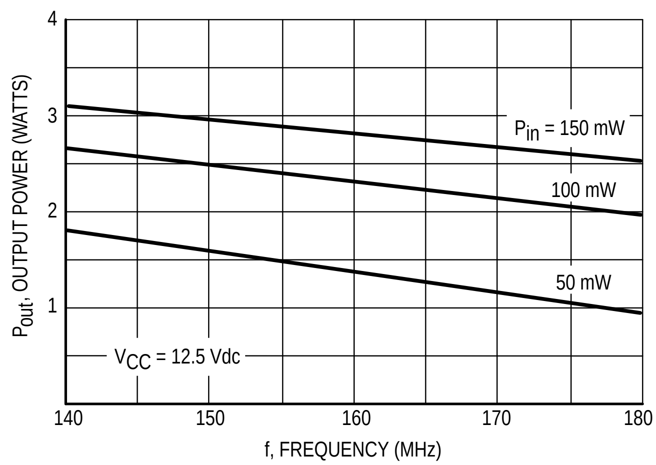


Figure 6. Power Output versus Frequency

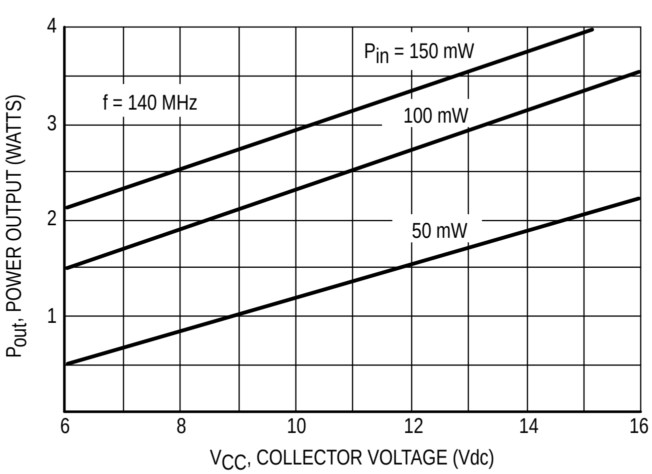


Figure 7. Power Output versus Collector Voltage

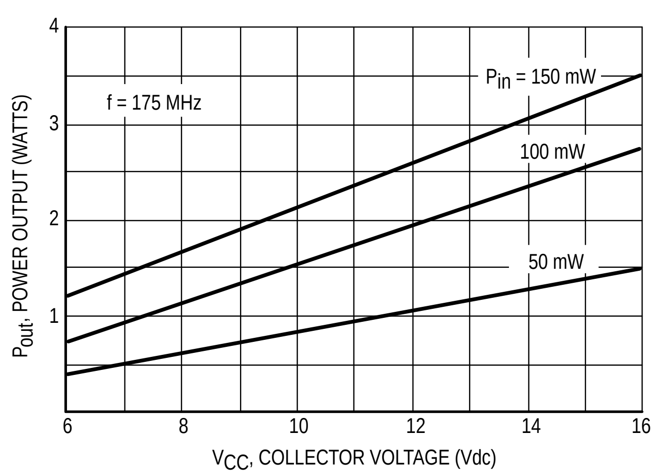
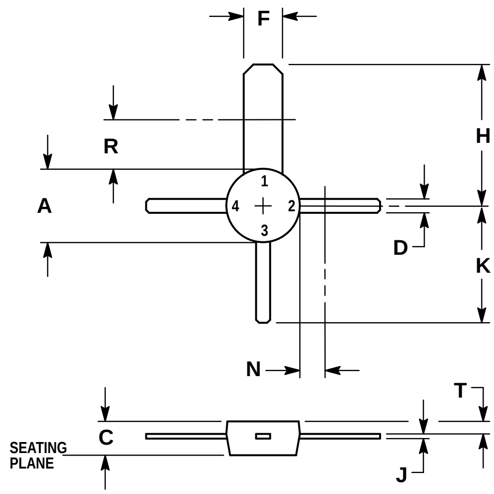


Figure 8. Power Output versus Collector Voltage

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. LEAD DIMENSIONS UNCONTROLLED WITHIN DIMENSION N AND R.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
C	0.075	0.100	1.91	2.54
D	0.033	0.039	0.84	0.99
F	0.097	0.104	2.46	2.64
H	0.348	0.383	8.84	9.72
J	0.008	0.012	0.24	0.30
K	0.285	0.320	7.24	8.12
N	—	0.065	—	1.65
R	—	0.128	—	3.25
T	0.025	0.040	0.64	1.01

STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

CASE 317D–02
ISSUE C

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