The RF TMOS® Line

Power Field Effect Transistor

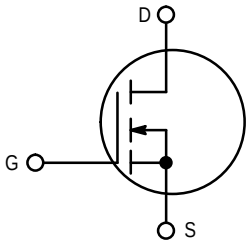
N–Channel Enhancement Mode

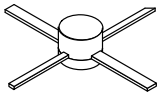
MRF158

2.0 W, to 500 MHz
TMOS
BROADBAND
RF POWER FET

Designed for wideband large–signal amplifier and oscillator applications to 500 MHz.

- Guaranteed 28 Volt, 400 MHz Performance
  Output Power = 2.0 Watts
  Minimum Gain = 16 dB
  Efficiency = 55% (Typical)
- Grounded Source Package for High Gain and Excellent Heat Dissipation (MRF158R)
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.





CASE 305A–01, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	8.0 45	Watts mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

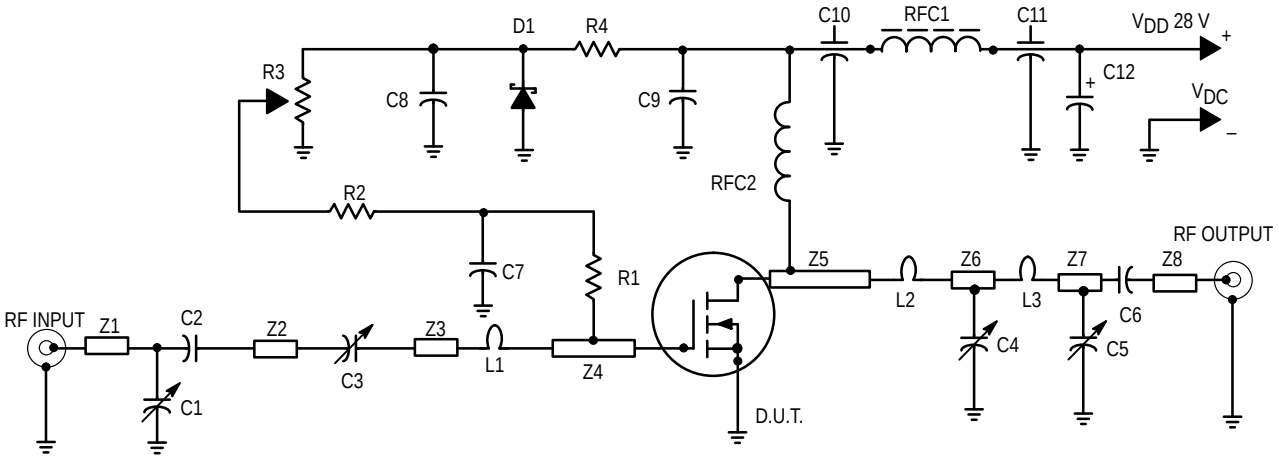
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	13.2	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

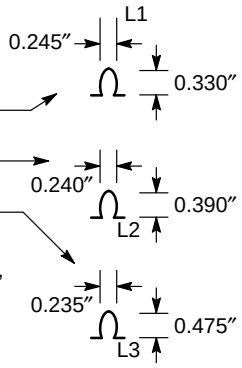
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	0.5	mAdc
Gate–Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (I_D = 10 mA, V_{DS} = 10 V)	$V_{GS(th)}$	1.0	4.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 100 mA)	g_{fs}	50	85	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	3.0	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	4.2	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	0.45	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	G_{ps}	16	20	—	dB
Drain Efficiency (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	η	45	55	—	%
Electrical Ruggedness (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{DD} = 28 V, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	Z_{in}	—	8.8 – j27.37	—	Ohms
Series Equivalent Output Impedance (V_{DD} = 28 V, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	Z_{out}	—	16.96 – j62	—	Ohms



C1, C4, C5 — Johanson Trimmer Capacitor, 2–20 pF
C2, C6 — 270 pF Chip Capacitor
C3 — Arco 404
C7, C8, C9 — 0.1 μF
C10, C11 — 680 pF Feed Through
C12 — 50 μF, 50 V
D1 — 1N5925A Motorola Zener
L1 — #18 AWG, Hairpin 0.825″ long, bend into hairpin
L2 — #18 AWG, Hairpin 0.875″ long, bend into hairpin
L3 — #18 AWG, Hairpin 0.965″ long, bend into hairpin

Board Material — 0.062″, Teflon Fiberglass, 2 oz., Copper clad both sides, ϵ_r = 2.55



R1 — 91 Ω 1/2 Watt
R2 — 10 kΩ 1/2 Watt
R3 — 10 kΩ, 10 Turns Bourns
R4 — 1.8 k 1.4 Watt
RFC1 — Ferroxcube VK200–19/4B
RFC2 — 10 Turns #20 AWG Enameled, 0.250″ ID
Z1 — Microstrip Line 0.150″ wide, 0.420″ long
Z2 — Microstrip Line 0.150″ wide, 0.420″ long
Z3 — Microstrip Line 0.150″ wide, 0.475″ long
Z4 — Microstrip Line 0.150″ wide, 0.825″ long
Z5 — Microstrip Line 0.150″ wide, 0.750″ long
Z6 — Microstrip Line 0.150″ wide, 0.500″ long
Z7 — Microstrip Line 0.150″ wide, 0.500″ long
Z8 — Microstrip Line 0.150″ wide, 0.450″ long

Figure 1. 400 MHz Test Circuit

TYPICAL CHARACTERISTICS

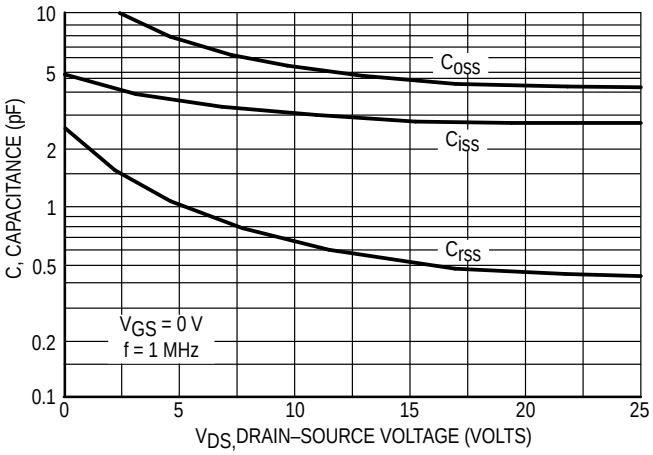


Figure 2. Capacitance versus Drain–Source Voltage

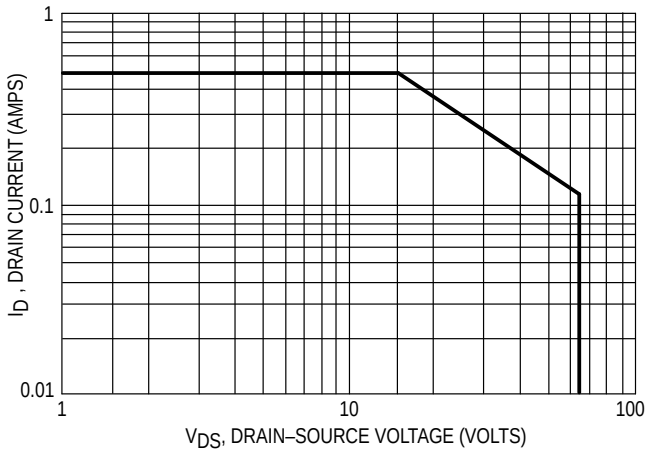


Figure 3. DC Safe Operating Area

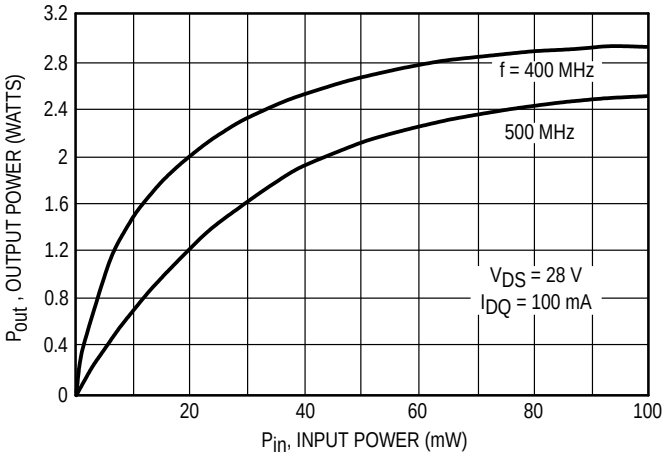


Figure 4. Output Power versus Input Power

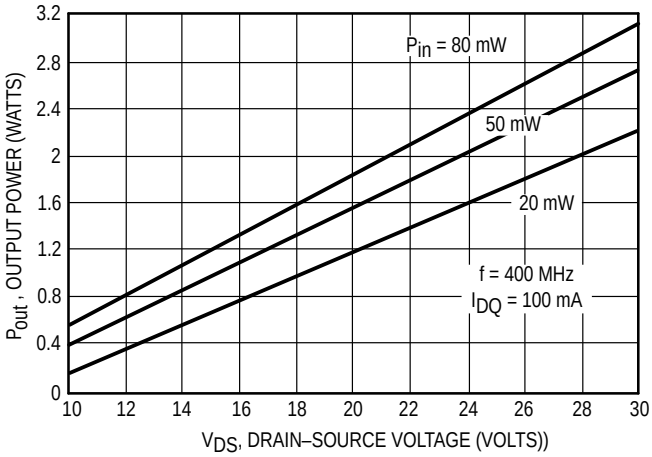
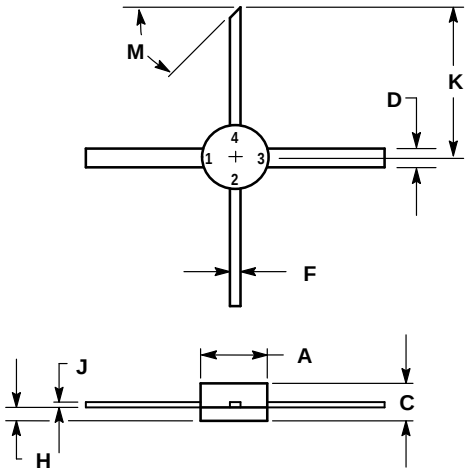


Figure 5. Output Power versus Voltage

Table 1. Typical Common Emitter S–Parameters

V_{DS} (Volts)	I_D (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
28	100	5	1.00	–2.0	3.84	–179	0.003	73	0.97	–2.0
		10	1.00	–2.0	3.81	179	0.004	83	0.97	–2.0
		30	1.00	–7.0	3.74	174	0.011	81	0.97	–6.0
		50	1.00	–11	3.72	170	0.018	78	0.96	–9.0
		100	0.98	–21	3.62	159	0.034	70	0.95	–19
		200	0.93	–41	3.28	137	0.061	52	0.90	–35
		300	0.88	–58	2.88	120	0.077	39	0.86	–50
		400	0.83	–75	2.57	104	0.088	27	0.81	–63
		500	0.79	–87	2.24	91	0.090	17	0.78	–74
		600	0.75	–99	1.94	78	0.084	8.0	0.75	–84
		700	0.73	–110	1.72	68	0.077	2.0	0.75	–93
		800	0.72	–120	1.52	58	0.067	–3.0	0.75	–99
		900	0.71	–130	1.35	48	0.055	–6.0	0.74	–108
		1000	0.71	–139	1.18	40	0.043	–4.0	0.73	–114

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.200	0.220	5.08	5.59
C	0.095	0.130	2.41	3.30
D	0.055	0.065	1.40	1.65
F	0.025	0.035	0.64	0.89
H	0.040	0.050	1.02	1.27
J	0.003	0.007	0.08	0.18
K	0.435	—	11.05	—
M	45 °REF		45 °REF	

STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

CASE 305A–01
ISSUE A

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