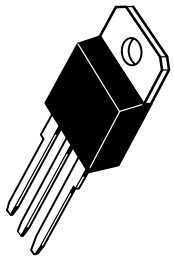
NPN
BDV65B
PNP
BDV64B

Complementary Silicon Plastic Power Darlingtons

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain
  HFE = 1000 (min.) @ 5 Adc
- Monolithic Construction with Built–in Base Emitter Shunt Resistors

DARLINGTONS
10 AMPERES
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60 – 80 – 100 – 120 VOLTS
125 WATTS



CASE 340D–01
SOT 93, TO–218 TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	10 20	Adc
Base Current	I_B	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 125 1.0	 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	°C/W

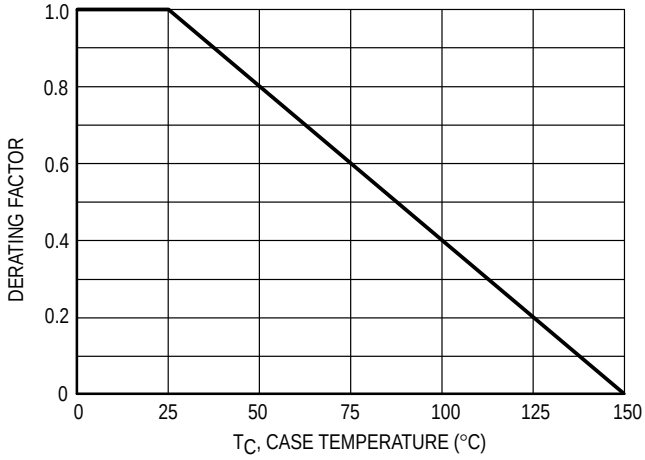


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	0.4	mAdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	—	2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	1000	—	—
Collector–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.02 Adc)	$V_{CE(sat)}$	—	2.0	Vdc
Base–Emitter Saturation Voltage (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	2.5	Vdc

NPN

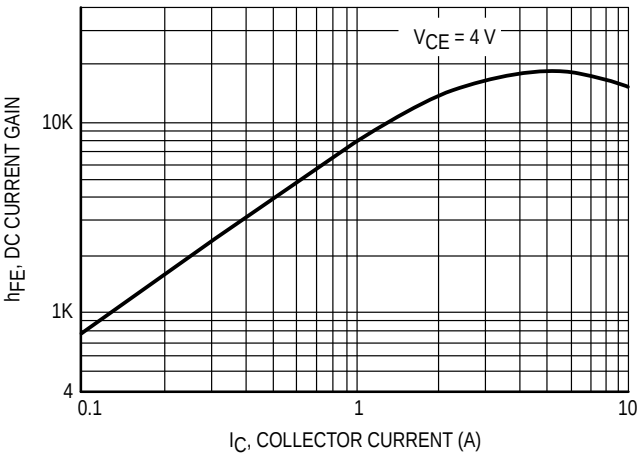


Figure 2. DC Current Gain

PNP

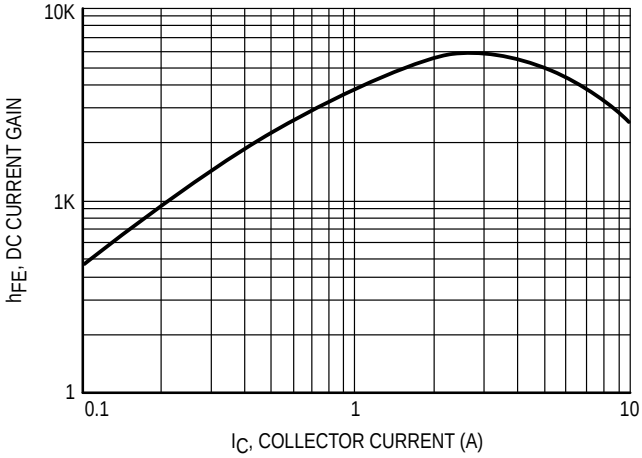


Figure 3. DC Current Gain

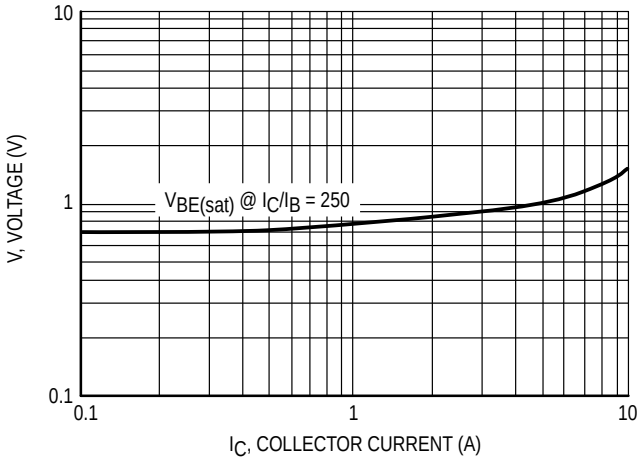


Figure 4. “On” Voltages

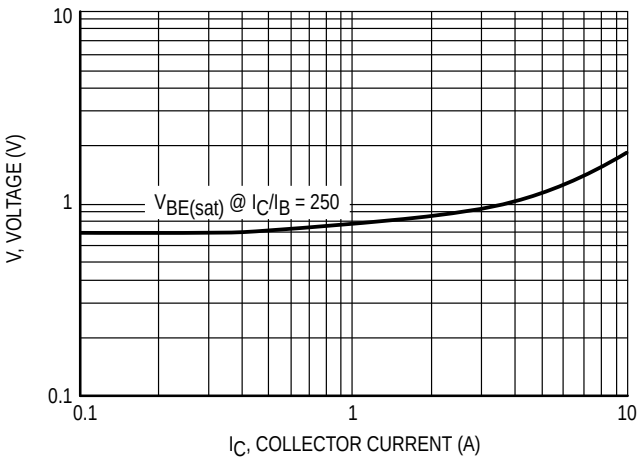


Figure 5. “On” Voltages

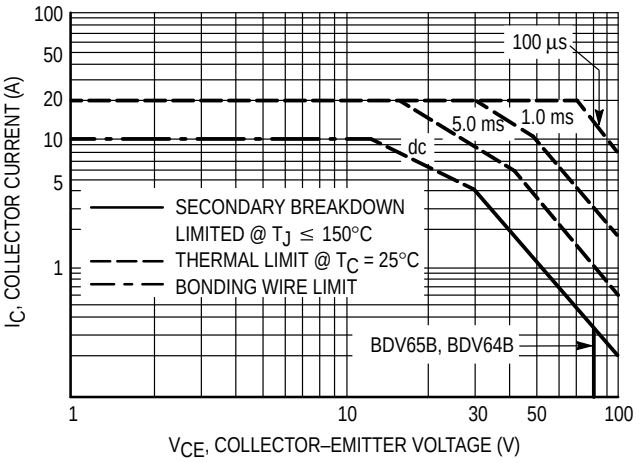


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)}$ = 150°C, T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

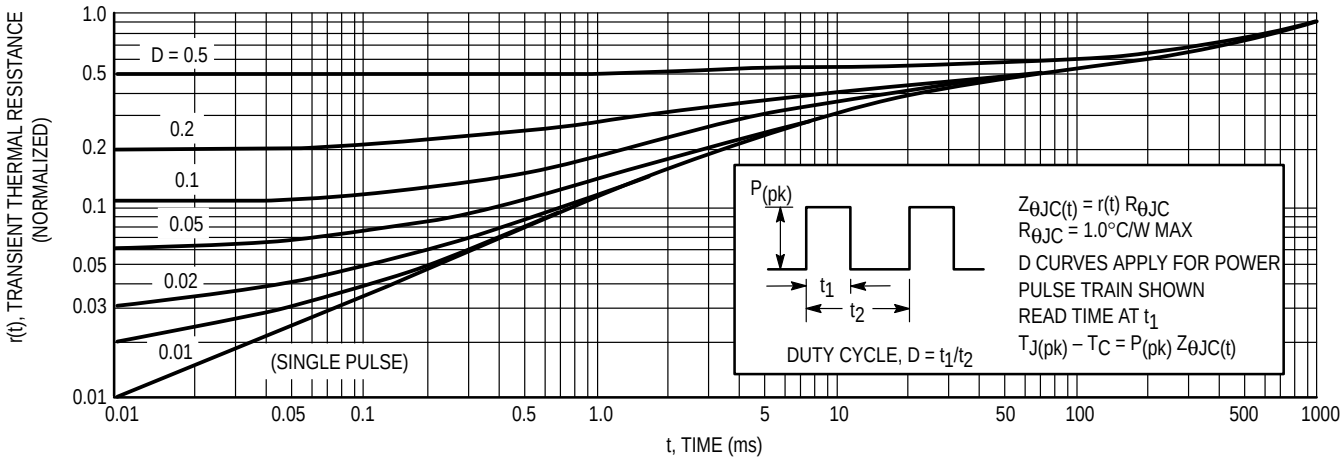
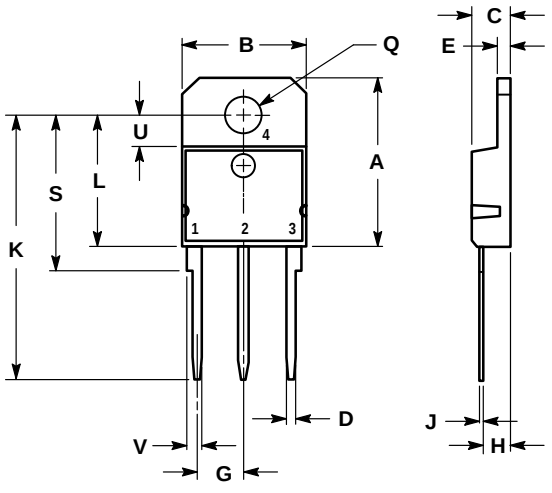


Figure 7. Thermal Response

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.00	19.60	0.749	0.771
B	14.00	14.50	0.551	0.570
C	4.20	4.70	0.165	0.185
D	1.00	1.30	0.040	0.051
E	1.45	1.65	0.058	0.064
G	5.21	5.72	0.206	0.225
H	2.60	3.00	0.103	0.118
J	0.40	0.60	0.016	0.023
K	28.50	32.00	1.123	1.259
L	14.70	15.30	0.579	0.602
Q	4.00	4.25	0.158	0.167
S	17.50	18.10	0.689	0.712
U	3.40	3.80	0.134	0.149
V	1.50	2.00	0.060	0.078

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340D–01
SOT 93, TO–218 TYPE
ISSUE A

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