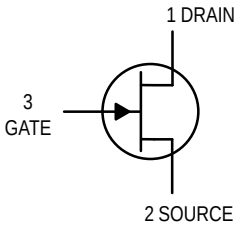
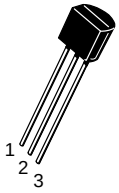
JFET Switching

N–Channel — Depletion



2N5555



CASE 29–04, STYLE 5
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	25	Vdc
Gate–Source Voltage	V_{GS}	25	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Junction Temperature Range	T_J	–65 to +150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate–Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	$V_{(BR)GSS}$	25	—	Vdc
Gate Reverse Current (V_{GS} = 15 Vdc, V_{DS} = 0)	I_{GSS}	—	1.0	nAdc
Drain Cutoff Current (V_{DS} = 12 Vdc, V_{GS} = –10 V) (V_{DS} = 12 Vdc, V_{GS} = –10 V, T_A = 100°C)	$I_{D(off)}$	— —	10 2.0	nAdc μAdc
ON CHARACTERISTICS				
Zero–Gate–Voltage Drain Current(1) (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	15	—	mAdc
Gate–Source Forward Voltage ($I_{G(f)}$ = 1.0 mAdc, V_{DS} = 0)	$V_{GS(f)}$	—	1.0	Vdc
Drain–Source On–Voltage (I_D = 7.0 mAdc, V_{GS} = 0)	$V_{DS(on)}$	—	1.5	Vdc
Static Drain–Source On Resistance (I_D = 0.1 mAdc, V_{GS} = 0)	$r_{DS(on)}$	—	150	Ohms
SMALL–SIGNAL CHARACTERISTICS				
Small–Signal Drain–Source “ON” Resistance (V_{GS} = 0, I_D = 0, f = 1.0 kHz)	$r_{ds(on)}$	—	150	Ohms
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 10 Vdc, f = 1.0 MHz)	C_{rss}	—	1.2	pF
SWITCHING CHARACTERISTICS				
Turn–On Delay Time	(V_{DD} = 10 Vdc, $I_{D(on)}$ = 7.0 mAdc, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = –10 Vdc) (See Figure 1)	$t_{d(on)}$	—	5.0	ns
Rise Time		t_r	—	5.0	ns
Turn–Off Delay Time	(V_{DD} = 10 Vdc, $I_{D(on)}$ = 7.0 mAdc, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = –10 Vdc) (See Figure 1)	$t_{d(off)}$	—	15	ns
Fall Time		t_f	—	10	ns

1. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 3.0%.

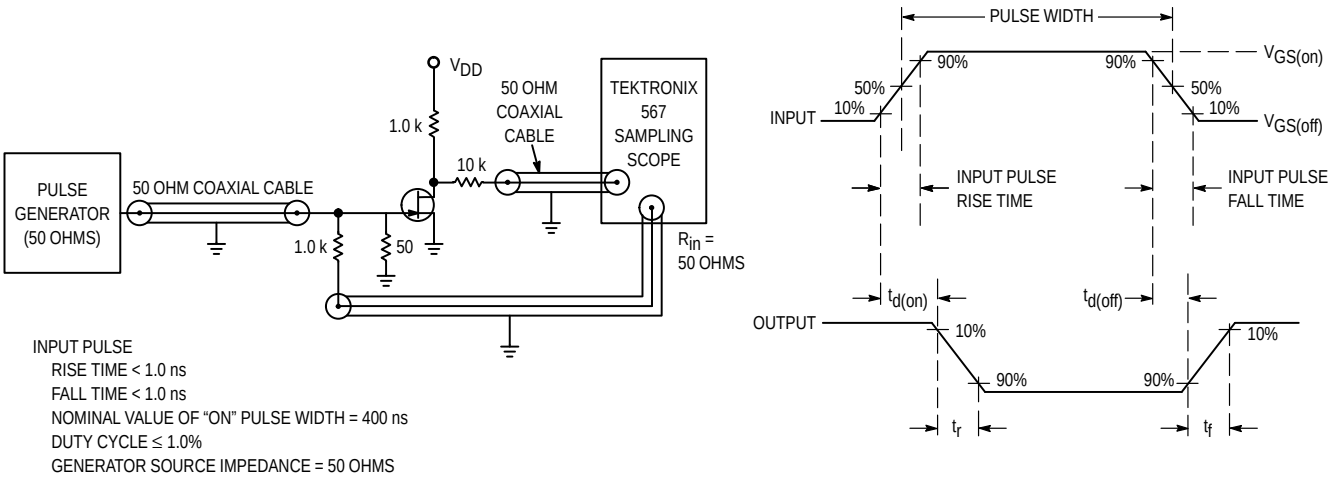


Figure 1. Switching Times Test Circuit

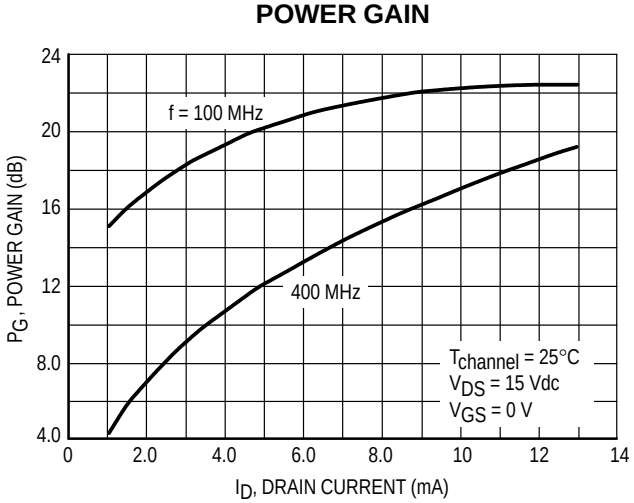
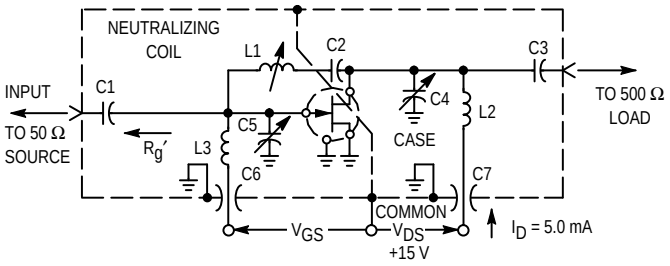


Figure 2. Effects of Drain Current



Adjust V_{GS} for
I_D = 50 mA
V_{GS} < 0 Volts

NOTE: The noise source is a hot–cold body (AIL type 70 or equivalent) with a test receiver (AIL type 136 or equivalent).

Reference Designation	VALUE	
	100 MHz	400 MHz
C1	7.0 pF	1.8 pF
C2	1000 pF	17 pF
C3	3.0 pF	1.0 pF
C4	1–12 pF	0.8–8.0 pF
C5	1–12 pF	0.8–8.0 pF
C6	0.0015 µF	0.001 µF
C7	0.0015 µF	0.001 µF
L1	3.0 µH*	0.2 µH**
L2	0.15 µH*	0.03 µH**
L3	0.14 µH*	0.022 µH**

*L1 17 turns, (approx. — depends upon circuit layout) AWG #28 enameled copper wire, close wound on 9/32″ ceramic coil form. Tuning provided by a powdered iron slug.
L2 4–1/2 turns, AWG #18 enameled copper wire, 5/16″ long, 3/8″ I.D. (AIR CORE).
L3 3–1/2 turns, AWG #18 enameled copper wire, 1/4″ long, 3/8″ I.D. (AIR CORE).

**L1 6 turns, (approx. — depends upon circuit layout) AWG #24 enameled copper wire, close wound on 7/32″ ceramic coil form. Tuning provided by an aluminum slug.
L2 1 turn, AWG #16 enameled copper wire, 3/8″ I.D. (AIR CORE).
L3 1/2 turn, AWG #16 enameled copper wire, 1/4″ I.D. (AIR CORE).

Figure 3. 100 MHz and 400 MHz Neutralized Test Circuit

NOISE FIGURE

($T_{channel}$ = 25°C)

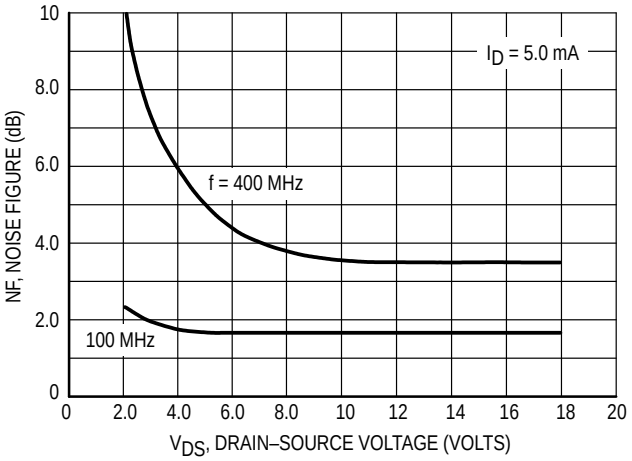


Figure 4. Effects of Drain–Source Voltage

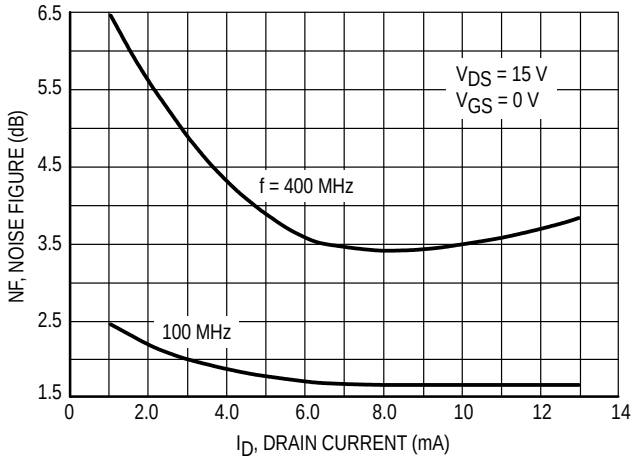


Figure 5. Effects of Drain Current

INTERMODULATION CHARACTERISTICS

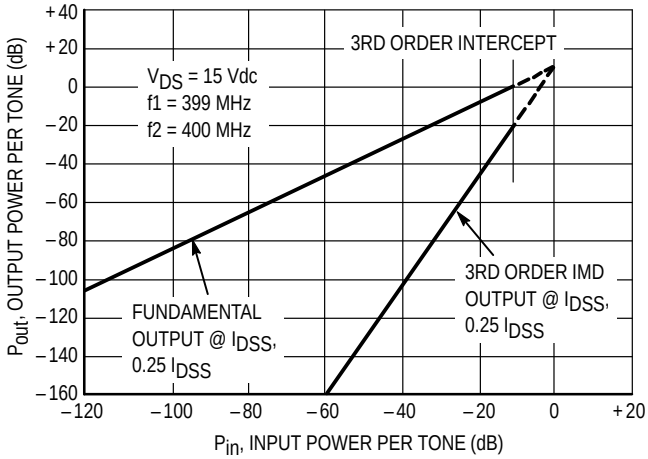


Figure 6. Third Order Intermodulation Distortion

COMMON SOURCE CHARACTERISTICS

ADMITTANCE PARAMETERS

(V_{DS} = 15 Vdc, $T_{channel}$ = 25°C)

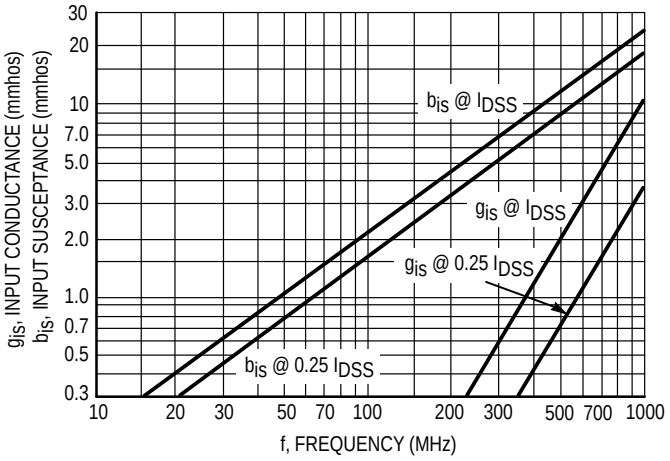


Figure 7. Input Admittance (y_{is})

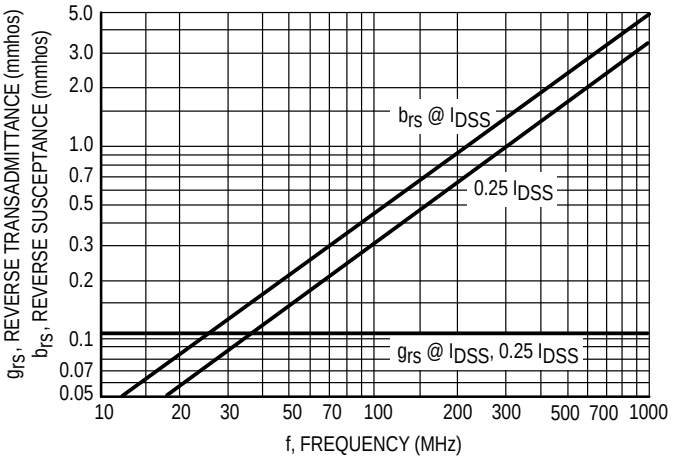


Figure 8. Reverse Transfer Admittance (y_{rs})

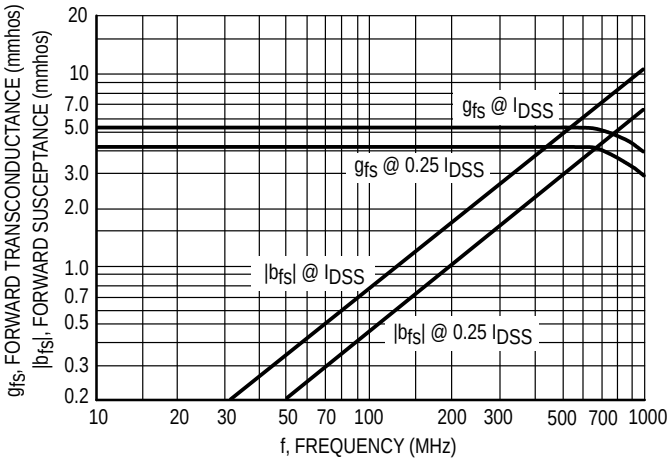


Figure 9. Forward Transadmittance (y_{fs})

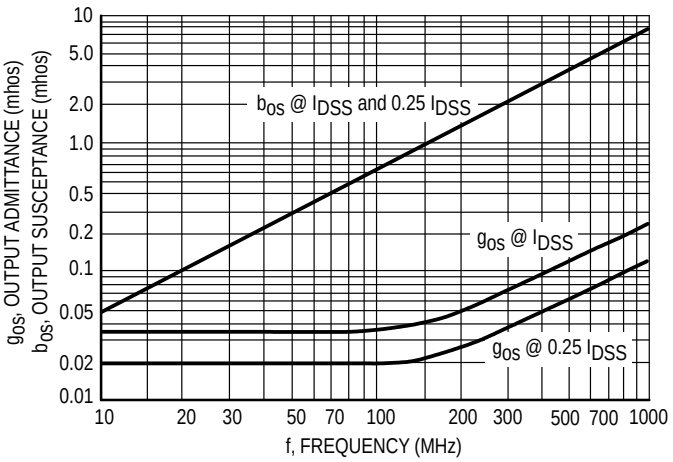


Figure 10. Output Admittance (y_{os})

COMMON SOURCE CHARACTERISTICS

S–PARAMETERS

(V_{DS} = 15 Vdc, $T_{channel}$ = 25°C, Data Points in MHz)

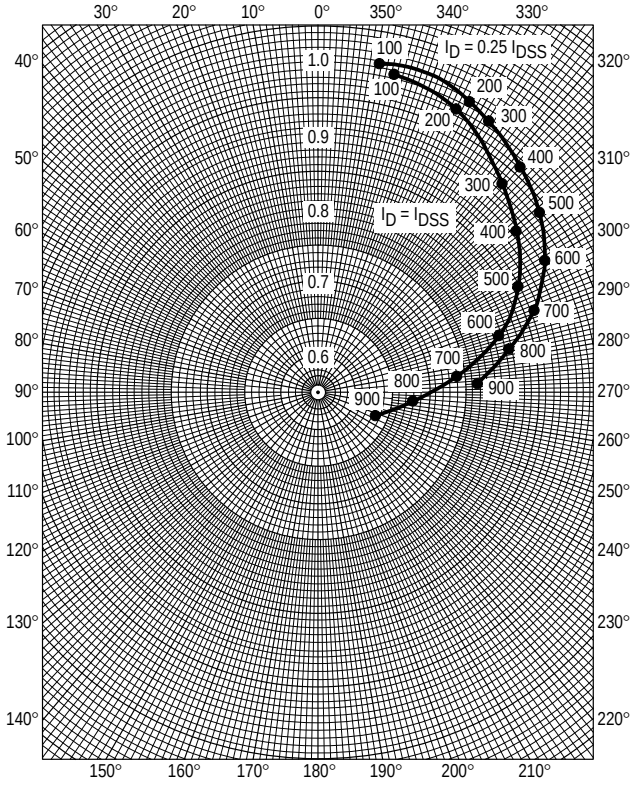


Figure 11. S_{11s}

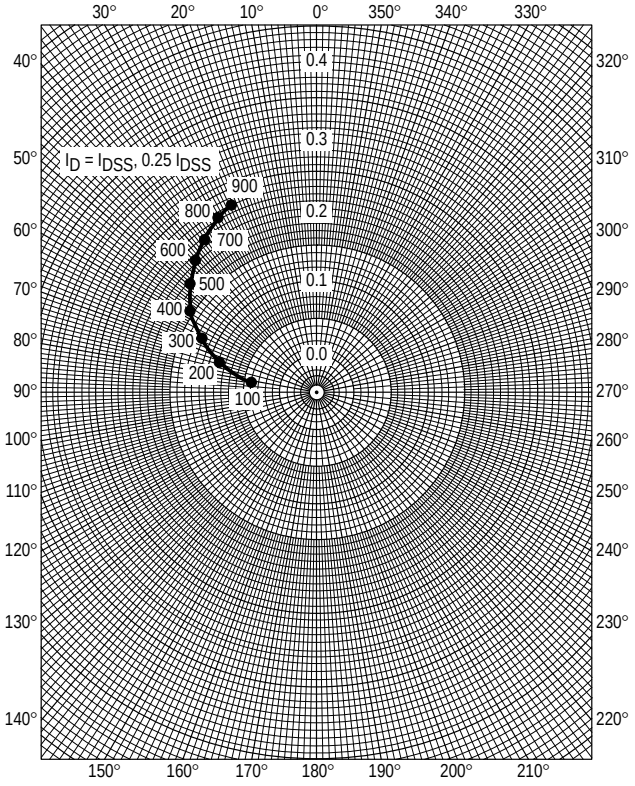


Figure 12. S_{12s}

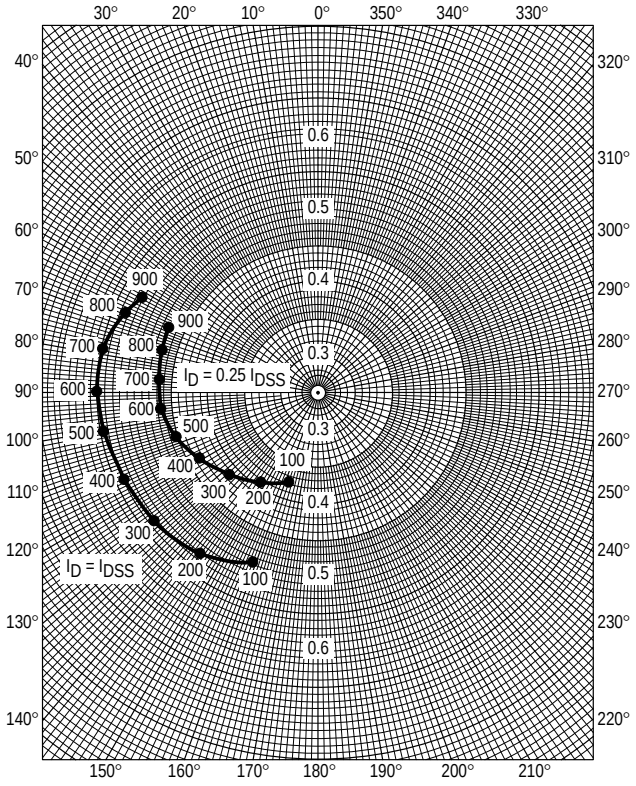


Figure 13. S_{21s}

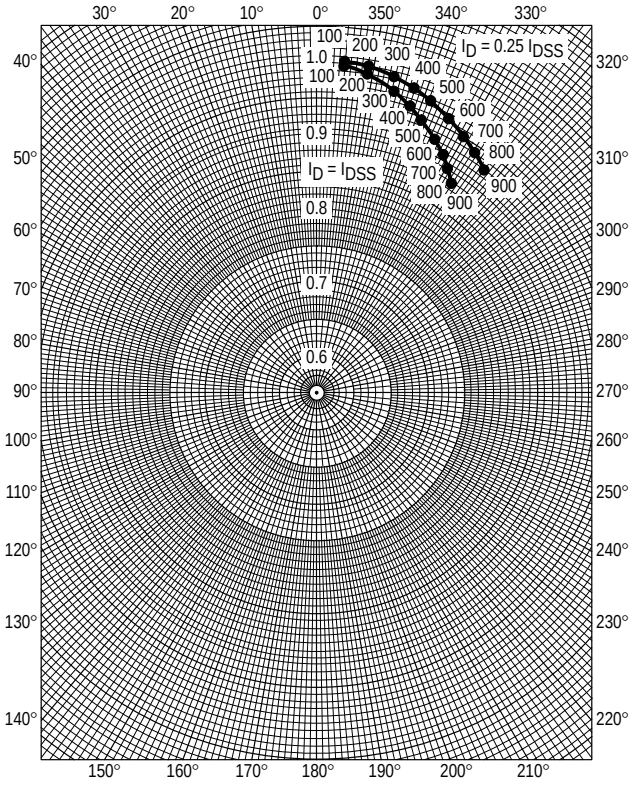


Figure 14. S_{22s}

COMMON GATE CHARACTERISTICS

ADMITTANCE PARAMETERS

(V_{DG} = 15 Vdc, $T_{channel}$ = 25°C)

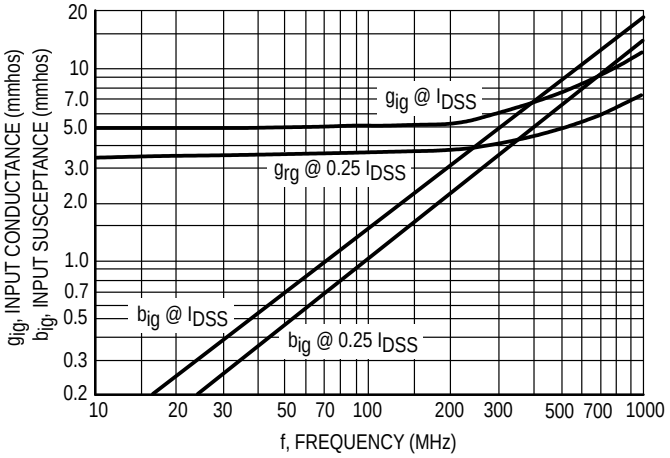


Figure 15. Input Admittance (y_{ig})

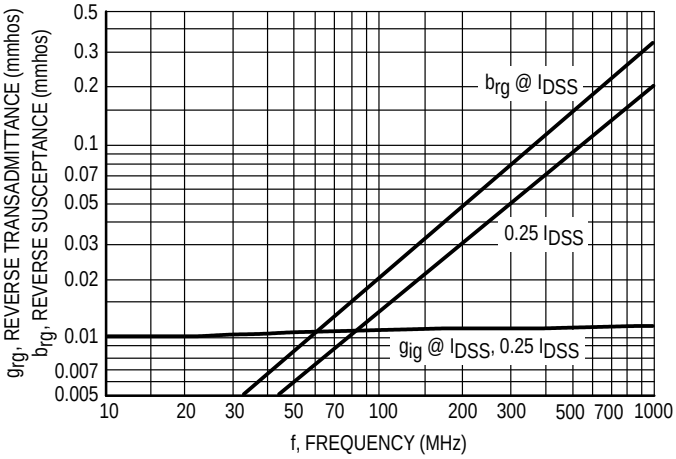


Figure 16. Reverse Transfer Admittance (y_{rg})

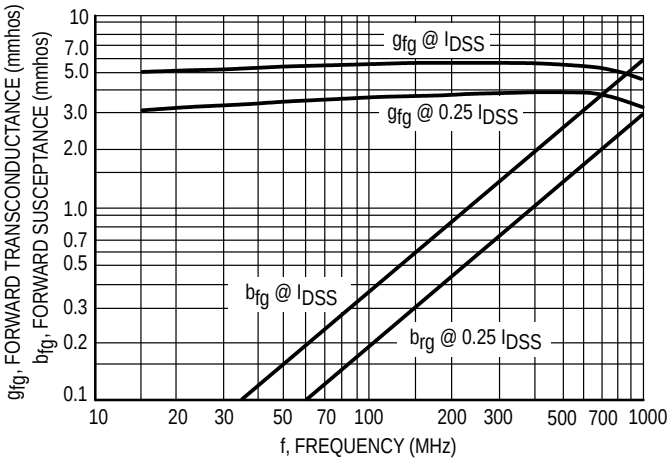


Figure 17. Forward Transfer Admittance (y_{fg})

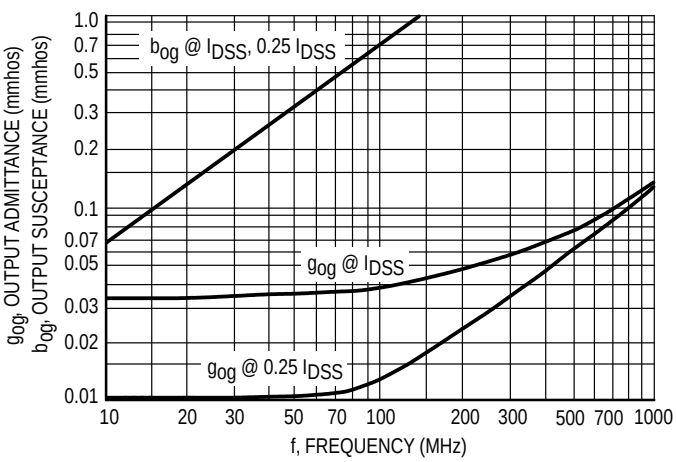


Figure 18. Output Admittance (y_{og})

COMMON GATE CHARACTERISTICS

S–PARAMETERS

(V_{DS} = 15 Vdc, $T_{channel}$ = 25°C, Data Points in MHz)

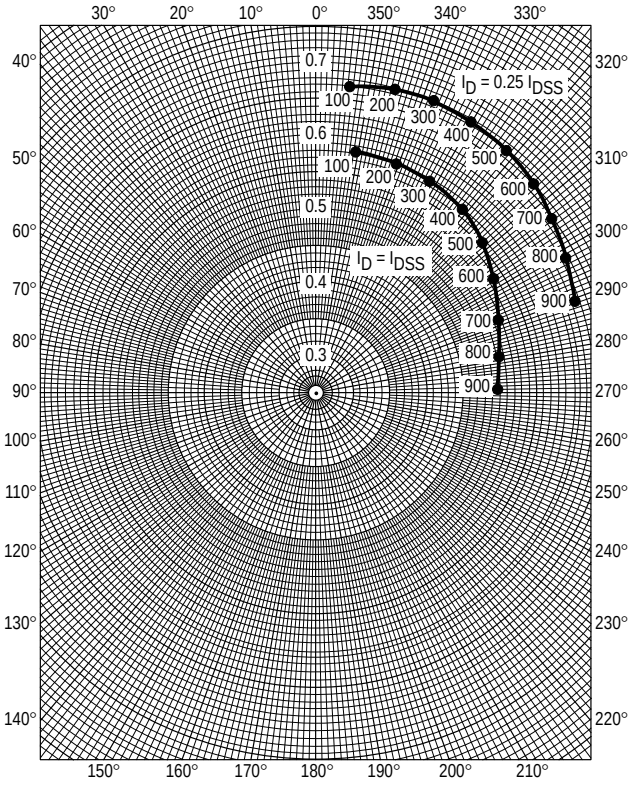


Figure 19. S_{11g}

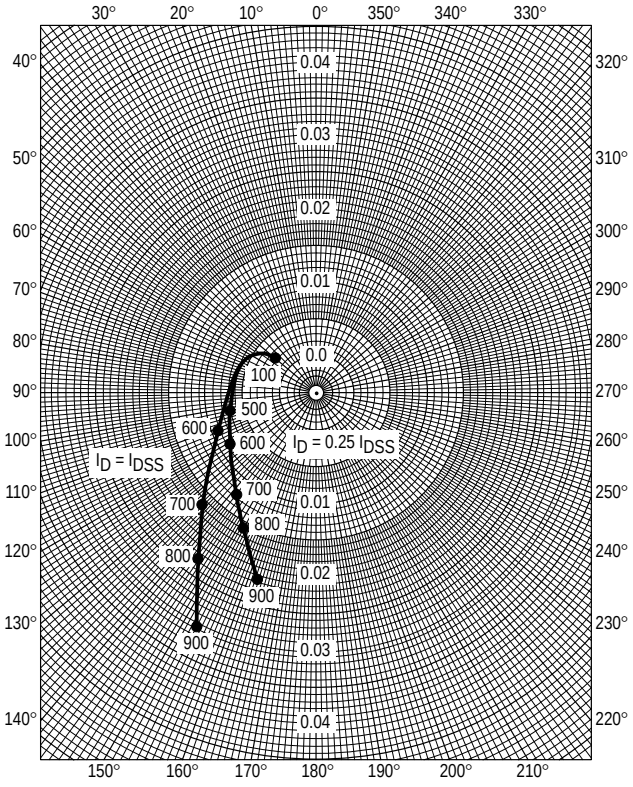


Figure 20. S_{12g}

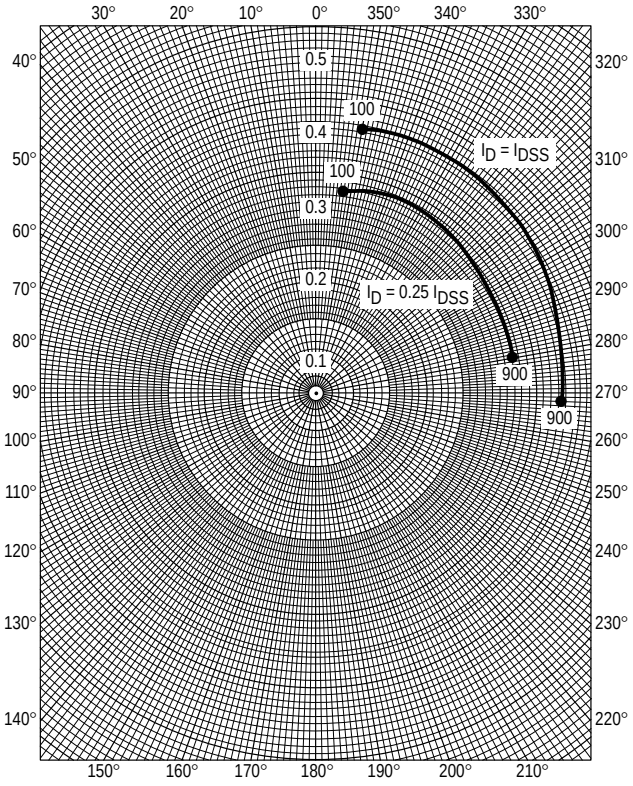


Figure 21. S_{21g}

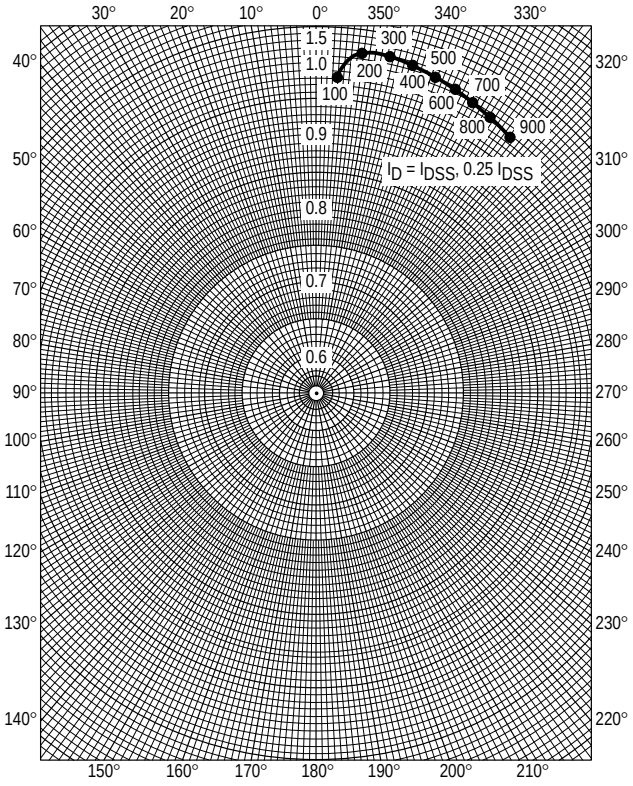
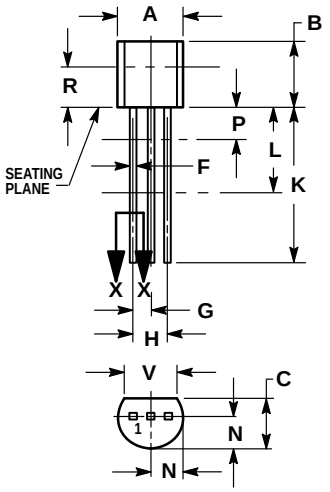
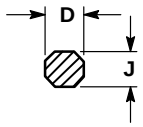


Figure 22. S_{22g}

PACKAGE DIMENSIONS





SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

CASE 029–04
(TO–226AA)
ISSUE AD

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
– US & Canada ONLY 1–800–774–1848

INTERNET: http://motorola.com/sps

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298