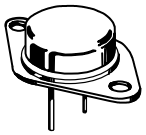
2N6576
2N6577
2N6578

NPN Silicon Power Darlington Transistors

General–purpose EpiBase power Darlington transistors, suitable for linear and switching applications.

- Replacement for 2N3055 and Driver
- High Gain Darlington Performance
- Built–in Diode Protection for Reverse Polarity Protection
- Can Be Driven from Low–Level Logic
- Popular Voltage Range
- Operating Range — –65 to +200°C

15 AMPERE
POWER TRANSISTORS
NPN SILICON
DARLINGTON
60, 90, 120 VOLTS
120 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

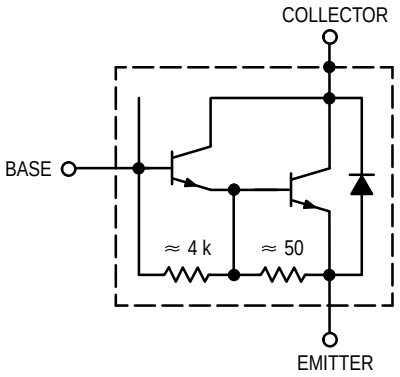
Rating	Symbol	2N6576	2N6577	2N6578	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	60	90	120	Vdc
Collector–Base Voltage	V_{CB}	60	90	120	Vdc
Emitter–Base Voltage	V_{EB}	7.0			Vdc
Collector Current — Continuous — Peak	I_C	15 30			Adc
Base Current — Continuous — Peak	I_B	0.25 0.50			Adc
Emitter Current — Continuous — Peak	I_E	15.25 30.5			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 120 0.685			 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.46	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16″ from Case for 10s.	T_L	265	°C

(1) Indicates JEDEC Registered Data.

DARLINGTON SCHEMATIC



REV 7

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N6576	$V_{CEO(sus)}$	60	—	Vdc
	2N6577		90	—	
	2N6578		120	—	
Collector Cutoff Current (V_{CE} = Rated Value)		I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CER} = Rated $V_{CEO(sus)}$ Value, R_{BE} = 10 kΩ, T_C = 150°C)		I_{CER}	—	5.0	mAdc
Collector Cutoff Current V_{CEX} = Rated $V_{CEO(sus)}$ Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	—	5.0	mAdc
Collector Cutoff Current (V_{CB} = Rated Value)		I_{CBO}	—	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			—
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			100	—	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)			500	5,000	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			2000	20,000	
(I_C = 0.4 Adc, V_{CE} = 3.0 Vdc)			200	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 0.15 Adc)			—	4.0	
(I_C = 10 Adc, I_B = 0.1 Adc)			—	2.8	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 0.15 Adc)			—	4.5	
(I_C = 10 Adc, I_B = 0.1 Adc)			—	3.5	
Collector–Emitter Diode Voltage Drop (I_{EC} = 15 Adc)		VF	—	4.5	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common–Emitter Small–Signal Short–Circuit Current Transfer Ratio (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	10	200	—

SWITCHING CHARACTERISTICS
RESISTIVE LOAD (Figure 2)

Delay Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = 0.1 Adc, t_p = 300 μs, Duty Cycle ≤ 2.0%)	t_d	—	0.15	μs
Rise Time		t_r	—	1.0	μs
Storage Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 0.1 Adc, t_p = 300 μs, Duty Cycle ≤ 2.0%)	t_s	—	2.0	μs
Fall Time		t_f	—	7.0	μs

* Indicates JEDEC Registered Data
(1) Pulse test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

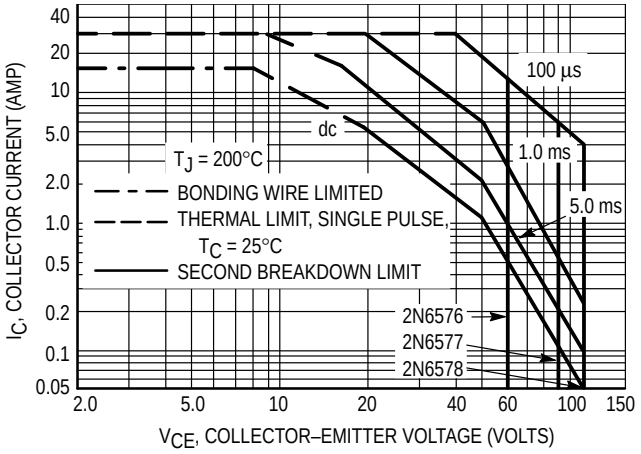


Figure 1. Rated Forward Biased Safe–Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%.

$T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

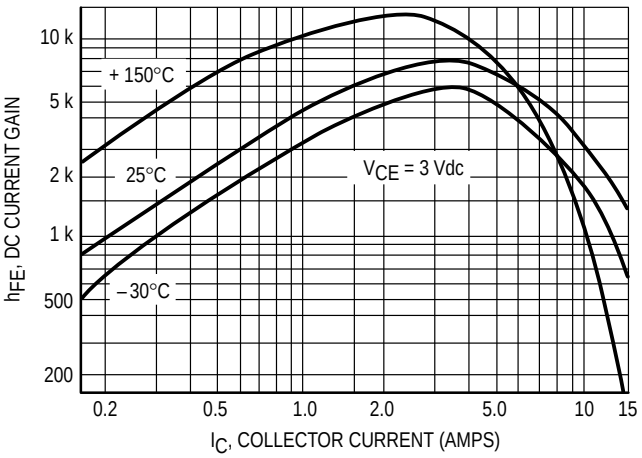


Figure 2. DC Current Gain

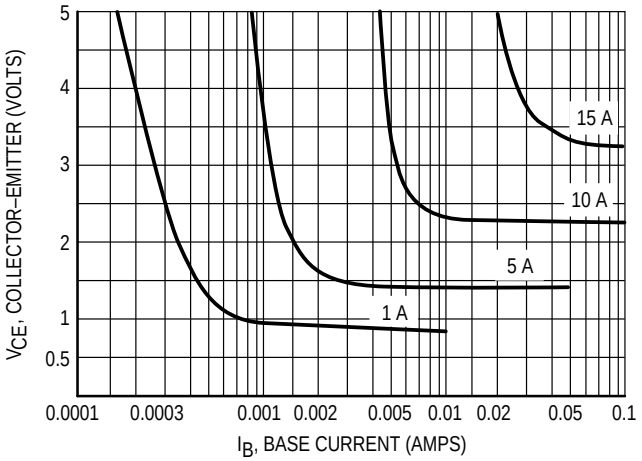


Figure 3. Collector Saturation Region

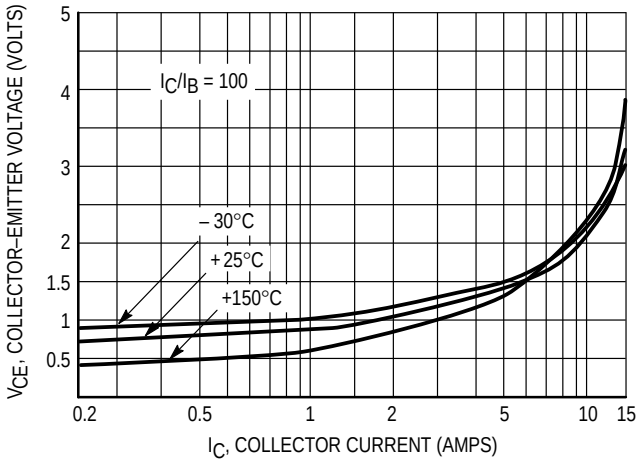


Figure 4. Collector Saturation Voltage

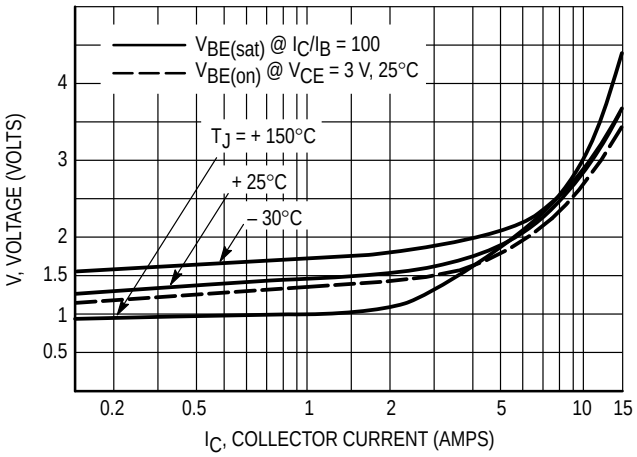


Figure 5. Base–Emitter Voltage

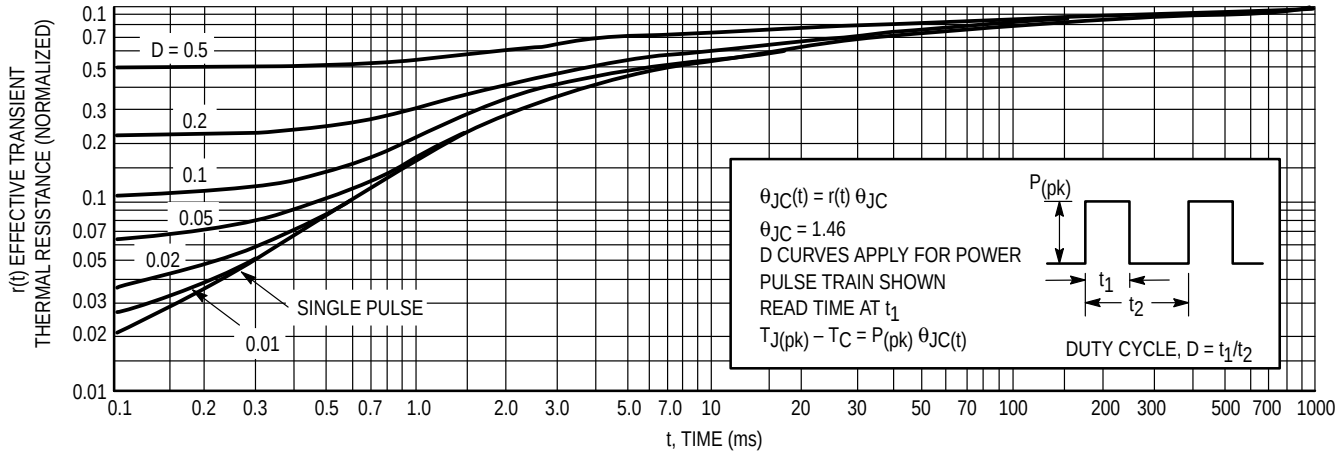
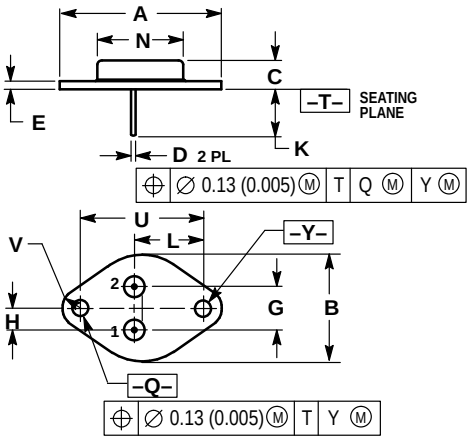


Figure 6. Thermal Response

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 1–07
TO–204AA (TO–3)
ISSUE Z

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