

## Active Errata List

- PGM: PSCxRB Fuse
- PSC: Prescaler
- PSC: PAOCnA and PAOCnB Register Bits (Asynchronous output control)
- PSC: PEVxA/B Flag Bits
- PSC : Output Polarity in Centered Mode
- PSC : Output Activity
- VREF
- DALI
- DAC: Register Update

## Errata History

Mask Revision	Lot Number	Errata List
REV A	04103x	1, 2, 3, 4, 5, 6, 7, 8, 9

## Errata Description

### 1. PGM: PSCxRB Fuse

The use of PSCxRB fuse can make the ISP fail.

#### Workaround:

When PSCxRB fuses are used, use the parallel programming mode to load a new program version.

### 2. PSC: Prescaler

The use of PSC's prescaler blocks the sample of PSC inputs during the two first cycles following the set of PSC run bit.

#### Workaround:

Clear the prescaler PPREx bit when stopping the PSC (prun = 0), and set them to appropriate value when starting the PSC (prun = 1), these bits are in the same PCTL register.

### 3. PSC: PAOCnA and PAOCnB Register Bits (Asynchronous output control)

These register bits are malfunctioning.

#### Workaround:

Do not use this feature.

### 4. PSC: PEVxA/B flag bits

These flags are set when a fault arises, but can also be set during the fault itself.

#### Workaround:

Don't clear these flags before the fault disappears.

### 5. PSC: Output Polarity in Centered Mode

In centered mode, PSCOUTn1 outputs are not inverted, so they are active at the same time as PSCOUTn0.

#### Workaround:

Use an external inverter (or a driver with inverting output) to drive the load on PSCOUTn1.



## AVR MCUs

AT90PWM2

AT90PWM3

## Errata Sheet



**6. PSC : POACnA/B Output Activity**

These register bits are not implemented in rev A.

**Workaround:**

Do not use this feature.

**7. VREF**

**Remark:** To have Internal Vref on AREF pin select an internal analog feature such as DAC or ADC.

**8. DALI**

Some troubles on Dali extension when edges are not symmetric.

**Workaround:**

Use an optocoupler providing symmetric edges on Rx and Tx DALI lines.

**9. DAC: Register Update**

Registers DACH & DACH are not written when the DAC is not enabled.

**Workaround:**

Enable DAC with DAEN before writing in DACL & DACH. To prevent an unwanted zero output on DAC pin, enable DAC output, with DAOE afterwards.



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