DATA SHEET

TDA9143
I²C-bus controlled, alignment-free PAL/NTSC/SECAM decoder/sync processor

Preliminary specification
File under Integrated Circuits, IC02

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Semiconductors

PHILIPS

I²C-bus controlled, alignment-free PAL/NTSC/SECAM decoder/sync processor

TDA9143

FEATURES

- Multi-standard colour decoder and sync processor for PAL, NTSC and SECAM
- PALplus helper blanking and EDTV-2 blanking
- I²C-bus controlled
- I²C-bus addresses hardware selectable
- Pin compatible with TDA9141
- Alignment free
- Few external components
- Designed for use with baseband delay lines
- Integrated video filters
- Adjustable luminance delay
- Noise detector with I²C-bus read-out
- Norm/no_norm detector with I²C-bus read-out
- CVBS or Y/C input, with automatic detection possibility
- CVBS output, provided I²C-bus address 8A is used
- Vertical divider system
- Two-level sandcastle signal
- VA synchronization pulse (3-state)
- HA synchronization pulse or clamping pulse CLP input/output
- Line-locked clock output (6.75 MHz or 6.875 MHz) or stand-alone I²C-bus output port
- Stand-alone I²C-bus input/output port
- Colour matrix and fast YUV switch
- Comb filter enable input/output with subcarrier frequency
- Internal bypass mode of external delay line for NTSC applications
- Low power standby mode with 3-state YUV outputs
- Fast blanking detector with I²C-bus read-out
- Blanked or unblanked sync on Y_{out} by I²C-bus bit BSY
- Internal MACROVISION gating for the horizontal PLL enabled by bus bit EMG.

GENERAL DESCRIPTION

The TDA9143 is an I²C-bus controlled, alignment-free PAL/NTSC/SECAM decoder/sync processor with blanking facilities for PALplus and EDTV-2 signals. The TDA9143 has been designed for use with baseband chrominance delay lines, and has a combined subcarrier frequency/comb filter enable signal for communication with a PAL/NTSC comb filter.

The IC can process both CVBS input signals and Y/C input signals. The input signal is available on an output pin, in the event of a Y/C signal, it is added into a CVBS signal.

The sync processor provides a two-level sandcastle, a horizontal pulse (CLP or HA pulse, bus selectable) and a vertical (VA) pulse. When the HA pulse is selected, a line-locked clock (LLC) signal is available at the output port pin (6.75 MHz or 6.875 MHz).

A fast switch can select either the internal Y signal with the UV input signals, or YUV signals made of the RGB input signals. The RGB input signals can be clamped with either the internal or an external clamping signal.

Two pins with an input/output port and an output port of the I²C-bus are available.

The I²C-bus address of the TDA9143 is hardware programmable.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9143	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current		50	60	70	mA
$V_{CVBS(p-p)}$	CVBS input voltage (peak-to-peak value)	top sync-white	–	1.0	1.43	V
$V_{Y(p-p)}$	luminance input voltage (peak-to-peak value)	top sync-white	–	1.0	1.43	V
$V_{C(p-p)}$	chrominance burst input voltage (peak-to-peak value)		–	0.3	0.6	V
$V_{Y(out)}$	luminance black-white output voltage		–	1.0	–	V
$V_{U(out)(p-p)}$	U output voltage (peak-to-peak value)	standard colour bar	–	1.33	–	V
$V_{V(out)(p-p)}$	V output voltage (peak-to-peak value)	standard colour bar	–	1.05	–	V
$V_{SC(bl)}$	sandcastle blanking voltage level		2.2	2.5	2.8	V
$V_{SC(clamp)}$	sandcastle clamping voltage level		4.2	4.5	4.8	V
V_{VA}	VA output voltage		4.0	5.0	5.5	V
V_{HA}	HA output voltage		4.0	5.0	5.5	V
$V_{LLC(p-p)}$	LLC output voltage amplitude (peak-to-peak value)		250	500	–	mV
$V_{R,G,B(p-p)}$	RGB input voltage (peak-to-peak value)	0 to 100% saturation	–	0.7	1.0	V
$V_{clamp(I/O)}$	clamping pulse input/output voltage		–	5.0	–	V
$V_{sub(p-p)}$	subcarrier output voltage amplitude (peak-to-peak value)		150	200	300	mV
V_{OPORT}	port output voltage		4.0	5.0	5.5	V

BLOCK DIAGRAM

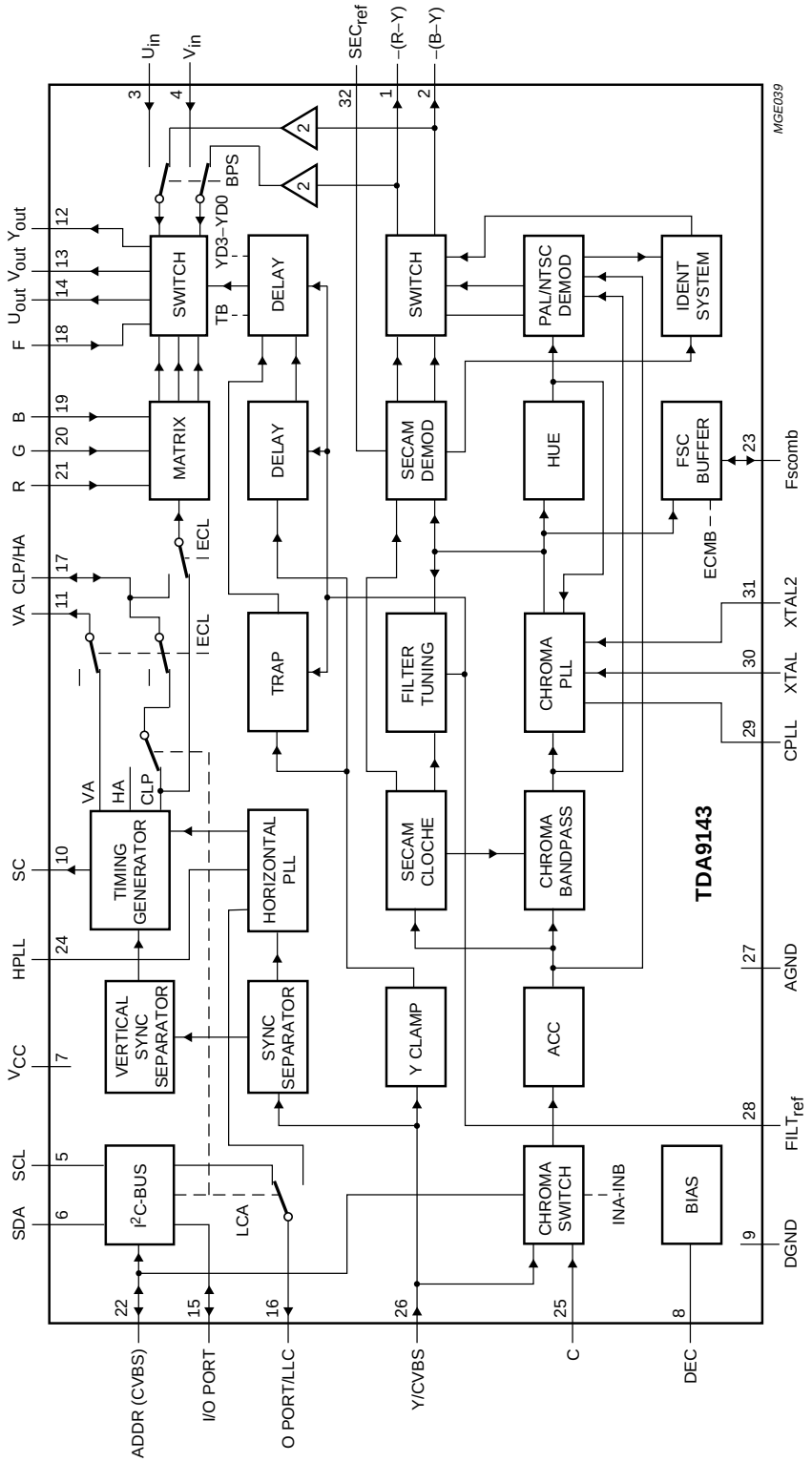


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
–(R–Y)	1	output signal for –(R–Y)
–(B–Y)	2	output signal for –(B–Y)
U_{in}	3	chrominance U input
V_{in}	4	chrominance V input
SCL	5	serial clock input
SDA	6	serial data input/output
V_{CC}	7	positive supply voltage
DEC	8	digital supply decoupling
DGND	9	digital ground
SC	10	sandcastle output
VA	11	vertical acquisition synchronization pulse
Y_{out}	12	luminance output
V_{out}	13	chrominance V output
U_{out}	14	chrominance U output
I/O PORT	15	input/output port
O PORT/LLC	16	output port/line-locked clock output
CLP/HA	17	clamping pulse/HA synchronization pulse input/output
F	18	fast switch select input
B	19	BLUE input
G	20	GREEN input
R	21	RED input
ADDR (CVBS)	22	I²C-bus address input (CVBS output)
Fscomb	23	comb filter status input/output
HPLL	24	horizontal PLL filter
C	25	chrominance input
Y/CVBS	26	luminance/CVBS input
AGND	27	analog ground
$FILT_{ref}$	28	filter reference decoupling
CPLL	29	colour PLL filter
XTAL	30	reference crystal input
XTAL2	31	second crystal input
SEC_{ref}	32	SECAM reference decoupling

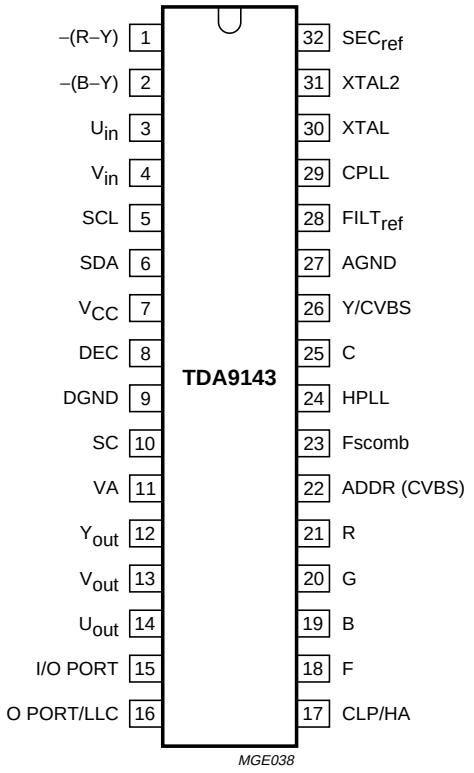


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA9143 is an I²C-bus controlled, alignment-free PAL/NTSC/SECAM colour decoder/sync processor which has been designed for use with baseband chrominance delay lines. For PALplus and EDTV-2 (60 Hz) signals blanking facilities are included.

In the standard operating mode the I²C-bus address is 8A. If the address input is connected to the positive supply rail the address will change to 8E.

Input switch

CAUTION
The voltage on the chrominance pin must never exceed 5.5 V. If it does, the IC enters a test mode.

The TDA9143 has a two pin input for CVBS or Y/C signals which can be selected via the I²C-bus. The input selector also has a position in which it automatically detects whether a CVBS or Y/C signal is on the input. In this input selector position, standard identification first takes place on an added Y/CVBS and C input signal.

After that, both chrominance signal input amplitudes are checked once and the input with the strongest chrominance burst signal is selected. The input switch status is read out by the I²C-bus via output bit YC. The auto input detector indicates YC = 1 for a VBS input signal (no chrominance component).

CVBS output

In the standard operating mode with I²C-bus address 8A, a CVBS output signal is available on the address pin, which represents either the CVBS input signal or the Y/C input signal, added into a CVBS signal.

RGB colour matrix

CAUTION
The voltage on the U_{in} pin must never exceed 5.5 V. If it does, the IC enters a test mode.

The TDA9143 has a colour matrix to convert RGB input signals into YUV signals. A fast switch, controlled by the signal on pin F and enabled by I²C-bus via EFS (enable fast switch), can select between these YUV signals and the YUV signals of the decoder. Mode FRGB = 1 (forced RGB) overrules EFS and switches the matrixed RGB inputs to the YUV outputs.

The Y signal is internally connected to the switch. The −(R−Y) and −(B−Y) output signals of the decoder first have to be delayed in external baseband chrominance delay lines. The outputs of the delay lines must be connected to the UV input pins. If the RGB signals are not synchronous with the selected decoder input signal, clamping of the RGB input signals is possible by I²C-bus selection of ECL (external RGB clamp mode) and by feeding an external clamping signal to the CLP pin.

Also in external RGB clamp mode the VA output will be in a high impedance OFF-state. The YUV outputs can be put in 3-state mode by bus bit LPS (low power standby mode).

Standard identification

The standards which the TDA9143 can decode depend upon the choice of external crystals. If a 4.4 MHz and a 3.6 MHz crystal are used then SECAM, PAL 4.4/3.6 and NTSC 4.4/3.6 can be decoded. If two 3.6 MHz crystals are used then only PAL 3.6 and NTSC 3.6 can be decoded.

Which 3.6 MHz standards can be decoded depends upon the exact frequencies of the 3.6 MHz crystals. In an application where not all standards are required only one crystal is sufficient; in this instance the crystal must be connected to the reference crystal input (pin 30). If a 4.4 MHz crystal is used it must always be connected to the reference crystal input. Both crystals are used to provide a reference for the filters and the horizontal PLL, however, only the reference crystal is used to provide a reference for the SECAM demodulator. To enable the calibrating circuits to be adjusted exactly, two bits from I²C-bus subaddress 00 are used to indicate which crystals are connected to the IC.

The standard identification circuit is a digital circuit without external components. The search loop is illustrated in Fig.3. The decoder (via the I²C-bus) can be forced to decode either SECAM or PAL/NTSC (but not PAL or NTSC). Crystal selection can also be forced. Information concerning standard and which crystal is selected and whether the colour killer is ON or OFF is provided by the read out.

Using the forced-mode does not affect the search loop, it does however prevent the decoder from reaching or staying in an unwanted state. The identification circuit skips impossible standards (e.g. SECAM when no 4.4 MHz crystal is fitted) and illegal standards (e.g. in forced mode). To reduce the risk of wrong identification, PAL has priority over SECAM. Only line identification is used for SECAM. For a vertical frequency of 60 Hz, SECAM can be blocked to prevent wrong identification by means of bus bit SAF.

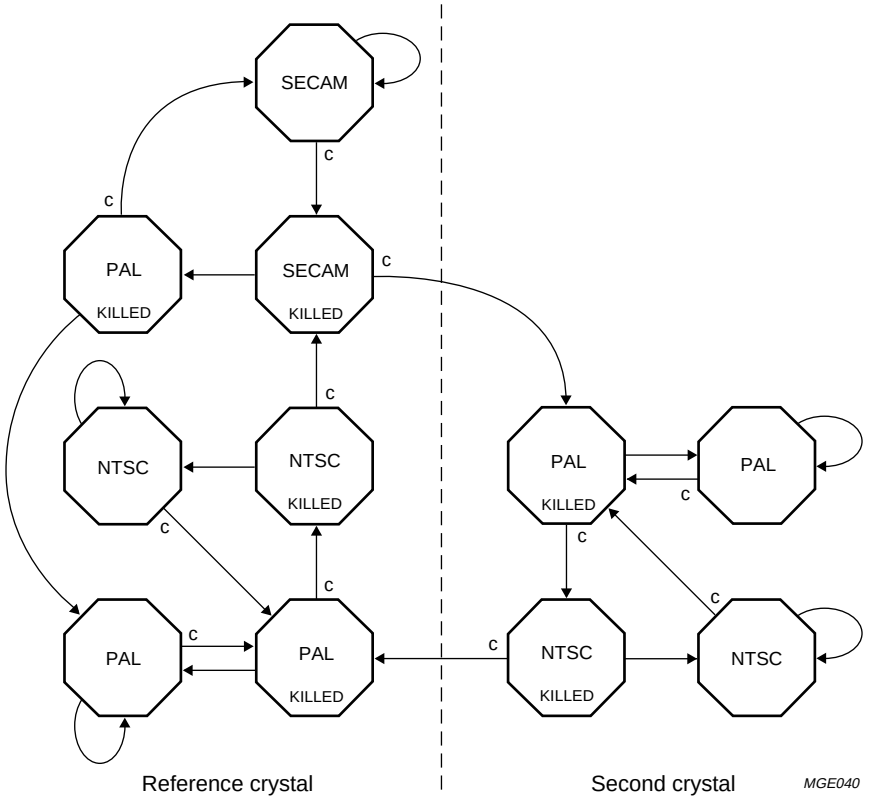


Fig.3 Search loop of the identification circuit.

Integrated filters

All chrominance bandpass and notch filters, including the luminance delay line, are an integral part of the IC. The filters are gyrator-capacitor type filters. The resonant frequency of the filters is controlled by a circuit that uses the active crystal to tune the SECAM Cloche filter during the vertical flyback time. The remaining filters and the luminance delay line are matched to this filter. The filters can be switched to either 4.43 MHz, 4.29 MHz or 3.58 MHz. The switching is controlled by the standard identification circuit. The luminance notch used for SECAM has a lower Q-factor than the notch used for PAL/NTSC. The notches are provided with a little preshoot to obtain a symmetrical step response. In Y/C mode the chrominance notch filters are bypassed, to preserve full signal bandwidth. For a CVBS signal the chrominance notch filters can be bypassed by bus selection of bit TB (trap bypass). The delay of the colour difference signals –(R–Y) and –(B–Y) in the chrominance signal path and the external chrominance delay lines when used, can be fitted to the luminance signal by I²C-bus in 40 ns steps.

The typical luminance delay can be calculated:

delay ≈ 90 + $\overline{SAK}\cdot\overline{SBK}$ {170 + 40($\overline{FRQ}\cdot\overline{TB}$)} + 160(YD3) + 160(YD2) + 80(YD1) + 40(YD0) [ns].

Colour decoder

The PAL/NTSC demodulator employs an oscillator that can operate with either crystal (3.6 MHz or 4.4 MHz). If the I²C-bus indicates that only one crystal is connected, it will always connect to the crystal on the reference crystal input (pin 30).

The Hue signal which is adjustable by I²C-bus, is gated during the burst for NTSC signals.

The SECAM demodulator is an auto-calibrating PLL demodulator which has two references. The reference crystal, to force the PLL to the desired free-running frequency and the bandgap reference, to obtain the correct absolute value of the output signal. The VCO of the PLL is calibrated during each vertical blanking period, when the IC is in search mode or in SECAM mode.

If the reference crystal is not 4.4 MHz the decoder will not produce the correct SECAM signals. Especially for NTSC applications an internal bypass mode of the external baseband delay line (for instance TDA4665) is added, controlled by bus bit BPS (bypass mode) and with a gain of 2. The bypass mode is not available for SECAM.

Comb filter interfacing

The frequency of the active crystal is fed to the Fscomb output, which can be connected to an external comb filter IC (e.g. SAA4961). When bus bit ECMB is LOW, the subcarrier frequency is suppressed and its DC value is LOW. With ECMB HIGH, the DC value is HIGH with the subcarrier frequency present, and I²C-bus output bit YC and the input switch are always forced in the Y/C mode, unless an external current sink (e.g. from the comb filter) prevents this, as pin Fscomb also acts as input pin. In this event the subcarrier frequency is still present on the same DC HIGH level.

PALplus and EDTV-2 helper blanking

For blanking of PALplus or EDTV-2 helper lines, the helper blanking can extend the vertical blanking of the Y, R–Y and B–Y outputs. Additional helper blanking bits (HOB, HBC) and norm/not norm (NRM) indication determine whether the helper signal has to be blanked or conditionally blanked depending on the signal-to-noise ratio bit SNR. Table 1 is valid in a 50 Hz or 60 Hz mode.

Table 1 Helper blanking modes

HOB	HBC	SNR	HELPER BLANKING
0	X	X	OFF
1	0	X	ON
1	1	0	OFF
1	1	1	ON

For PALplus (50 Hz, 625 lines) outside the letter box area blanking is possible and takes place on lines 275 to 371 and 587 to 59.

For EDTV-2 (system M, 60 Hz, 525 lines) outside the letter box area blanking is possible and takes place on lines 230 to 312 and 493 to 49 (1).

(1) For system M, line numbers start with the first equalizing pulse in field 1, but the internal line counter starts counting at the first vertical sync pulse in field 1. This line number notation is used here and in Fig.7.

Provided a NORM sync condition is present, with bus bit HBO = 1 and HBC = 0 blanking is activated. Conditional blanking is possible with HBO = 1 and HBC = 1 and SNR = 1.

The black level of the luminance signal is internally clamped with a large time constant to an internal reference black level. This black level is used as fill-in value for the Y signal during blanking.

Fast blanking detector

To detect the presence of a fast blanking signal, a circuit is added which indicates this event if in more than one line per field a blanking pulse is present at the fast blanking input (F). More than one line per field is chosen to prevent switching-off at every spike detected on the fast blanking input. The detector output FBA (fast blanking active) can be read-out by the I²C-bus.

Blanked/unblanked sync

By means of the I²C-bus bit BSY (blanked sync) output signal Y_{out} will be presented with or without its composite sync part. At BSY = 0 the composite sync is present on Y_{out}. When activated, helper blanking takes place only during helper lines scan. At BSY = 1 the black level is filled in during the line blanking interval and vertical blanking interval. When activated, the helper blanking extends the vertical blanking.

Sync processor (φ_1 loop)

The main part of the sync circuit is an oscillator running at $440 \times f_H$ (6.875 MHz), provided that I²C-bus address 8A is used or $432 \times f_H$ (6.75 MHz) for 8E. Its frequency is divided by 440 or 432 to lock the φ_1 loop to the incoming signal.

The time-constant of the loop can be selected by the I²C-bus (fast, auto or slow). In the fast mode the fast time-constant is chosen independent of signal conditions. In the auto mode the medium time-constant is present with a fast time constant during the vertical retrace period (‘field boost’). If the noise detector indicates a noisy video signal the time-constant switches to slow with a smaller field boost, which is also the time-constant for the slow mode. In case of a slow time constant sync gating takes place in a 6 μs window around the separated sync pulse. In case of no sync lock, both the auto and the slow mode have a medium time constant, to ensure reliable catching.

The noise content of the video signal is determined by a noise detector circuit. This circuit measures the noise at top sync during a 15 line period every field (65 lines after start VA pulse). When the noise level supersedes the

detector threshold in two consecutive fields, noise is indicated and bus bit SNR is set.

The free-running frequency of the oscillator is determined by a digital control circuit that is locked to the active crystal. When a power-on-reset pulse is detected the frequency of the oscillator is switched to a frequency of about 10 MHz (23 kHz horizontal frequency) to protect the horizontal output transistor. The oscillator frequency is calibrated to 6.875 MHz or 6.75 MHz after receiving data on subaddress 01 for the first time after power-on-reset detection.

To ensure that this procedure does not fail it is absolutely necessary to send subaddress 00 before subaddress 01. Subaddress 00 contains the crystal indication bits and when subaddress 01 is received the line oscillator calibration will be initiated (for the start-up procedure after power-on-reset detection, see the I²C-bus protocol). The calibration is terminated when the oscillator frequency reaches 6.875 MHz or 6.75 MHz.

The φ_1 loop can be opened using the I²C-bus. This is to facilitate On Screen Display (OSD) information. If there is no input signal or a very noisy input signal, the φ_1 loop can be opened to provide a stable line frequency, and thus a stable picture.

The sync part also delivers a two-level sandcastle signal, which provides a combined horizontal and vertical blanking signal and a clamping pulse for the display section of the TV.

MACROVISION sync gating

A dedicated gating signal for the separated sync pulses, starting 11 lines after the detection of a vertical sync pulse until picture scan starts, can be used to improve the behaviour of the horizontal PLL with respect to the unwanted disturbances caused by the pseudo-sync pulses in video signals with MACROVISION anti-copy guard signals. This sync gating excludes the pseudo-sync pulses and can only take place in the auto and fast φ_1 time constant mode, provided I²C-bus bit SNR = 0 and I²C-bus bit EMG = 1. I²C-bus bit EMG = 1 enables and EMG = 0 disables this sync gating in the horizontal PLL.

Vertical divider system

The vertical divider system has a fully integrated vertical sync separator.

The divider can accommodate both 50 Hz and 60 Hz systems; it can either determine the field frequency automatically or it can be forced to the desired system via the I²C-bus. A block diagram of the vertical divider system is illustrated in Fig.4.

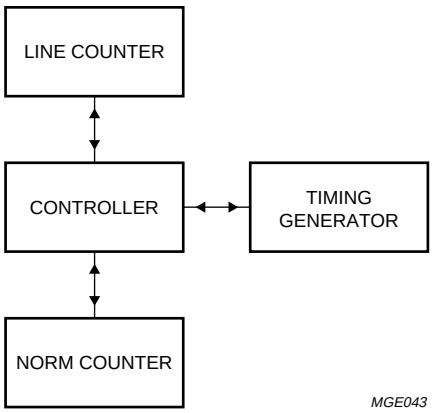


Fig.4 Block diagram of the vertical divider system.

The divider system operates at twice the horizontal frequency. The line counter receives enable pulses at this frequency, thereby counting two pulses per line. A state diagram of the controller is shown in Fig.5. Because it is symmetrical only the right-hand part will be described.

Depending on the previously found vertical frequency, the controller will be in one of the COUNT states. When the line counter has counted 488 pulses (i.e. 244 lines of the video input signal), the controller will move to the next state depending on the output of the norm counter. This can be either NORM, NEAR_NORM or NO_NORM, depending on the position of the vertical sync pulse in the previous fields. When the controller is in the NORM state it generates the vertical sync pulse (VSP) automatically and then, when the line counter is at LC = 626, moves to the WAIT state. In this condition it waits for the next pulse of the double line frequency signal, and then moves to the COUNT state of the current field frequency. When the controller returns to the COUNT state, the line counter will be reset half a line after the start of the vertical sync pulse of the video input signal. The NORM window normally looks within one line width and a sudden half line delay of the vertical sync pulse change can therefore be neglected.

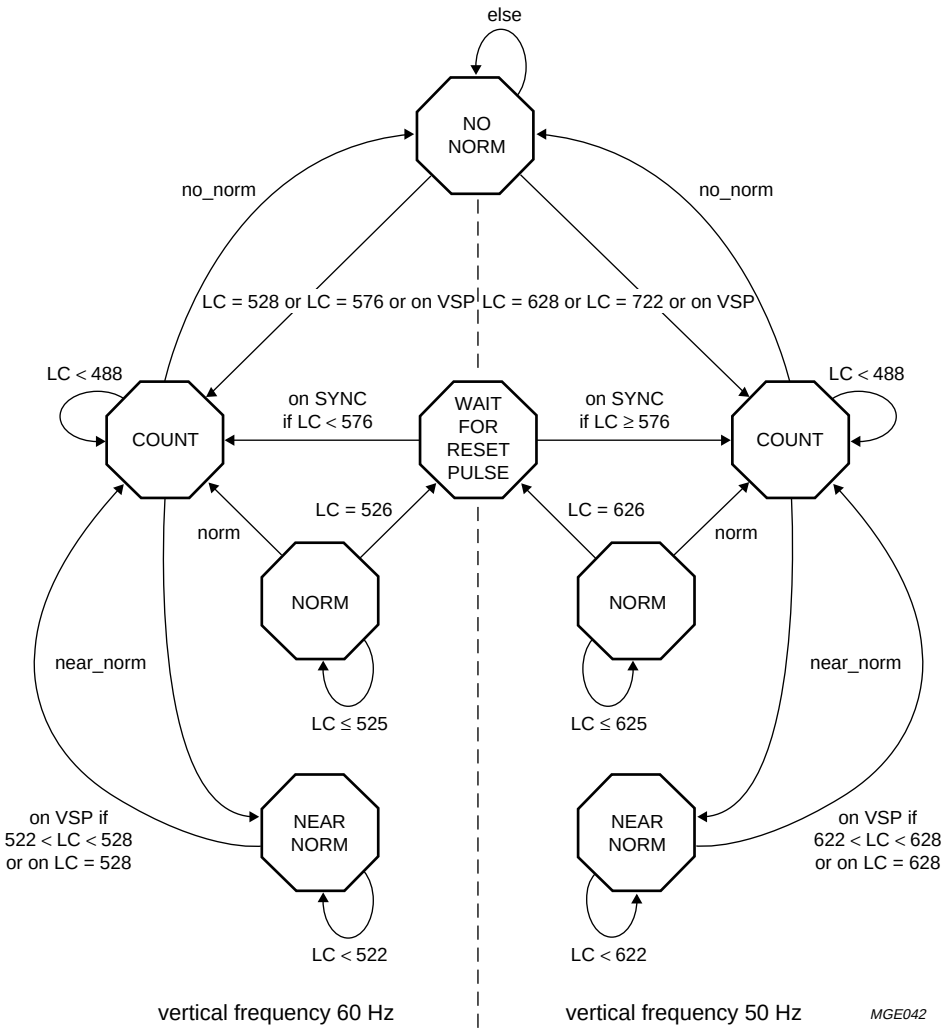


Fig.5 State diagram of the vertical divider system.

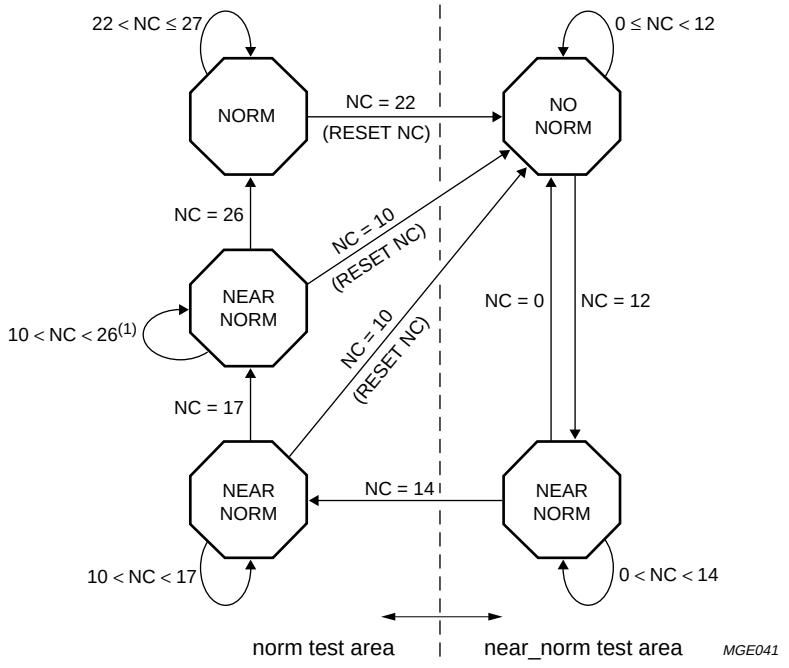
When the controller is in the NEAR_NORM state it will move to the COUNT state if it detects the vertical sync pulse within the NEAR_NORM window (i.e. 622 < LC < 628). If no vertical sync pulse is detected the controller will move back to the COUNT state when the line counter reaches LC = 628. The line counter will then be reset.

When the controller is in the NO_NORM state, it will move to the COUNT state when it detects a vertical sync pulse and reset the line counter. If a vertical sync pulse is not detected before LC = 722 (if the φ_1 loop is locked in forced mode) it will move to the COUNT state and reset the line counter. If the φ_1 loop is not locked the controller will return to the COUNT state when LC = 628.

The forced mode option keeps the controller in either the left-hand side (60 Hz) or the right-hand side (50 Hz) of the state diagram.

Figure 6 illustrates the state diagram of the norm counter which is an up/down counter that increases its counter value by 1 if it finds a vertical sync pulse within the selected window. If not, it decreases the counter value by 1 (or 2, see Fig.6). In the NEAR_NORM and NORM states the first correct vertical sync pulse after one or more incorrect vertical sync pulses is processed as an incorrect pulse. This procedure prevents the system from staying in the NEAR_NORM or NORM state if the vertical sync pulse is correct in the first field and incorrect in the second field.

In case of no sync lock (SLN = 1) the norm counter is reset to NO_NORM (wide search window), for fast vertical catching when switching between video sources. Fast switching between different channels however can still result in a continuous horizontal sync lock situation, when the channel is changed before the norm counter has reached the NORM state. To provide faster vertical catching in this case, measures have been taken to prevent the norm counter to count down to zero before reaching the NO_NORM state (see left-hand of Fig.6). Bus bit FWW (forced wide window) enables the norm counter to stay in the NO_NORM state if desired. The norm/no_norm status is read out by bus bit NRM.



(1) VSP found: count 1 up; no VSP found: count 2 down.

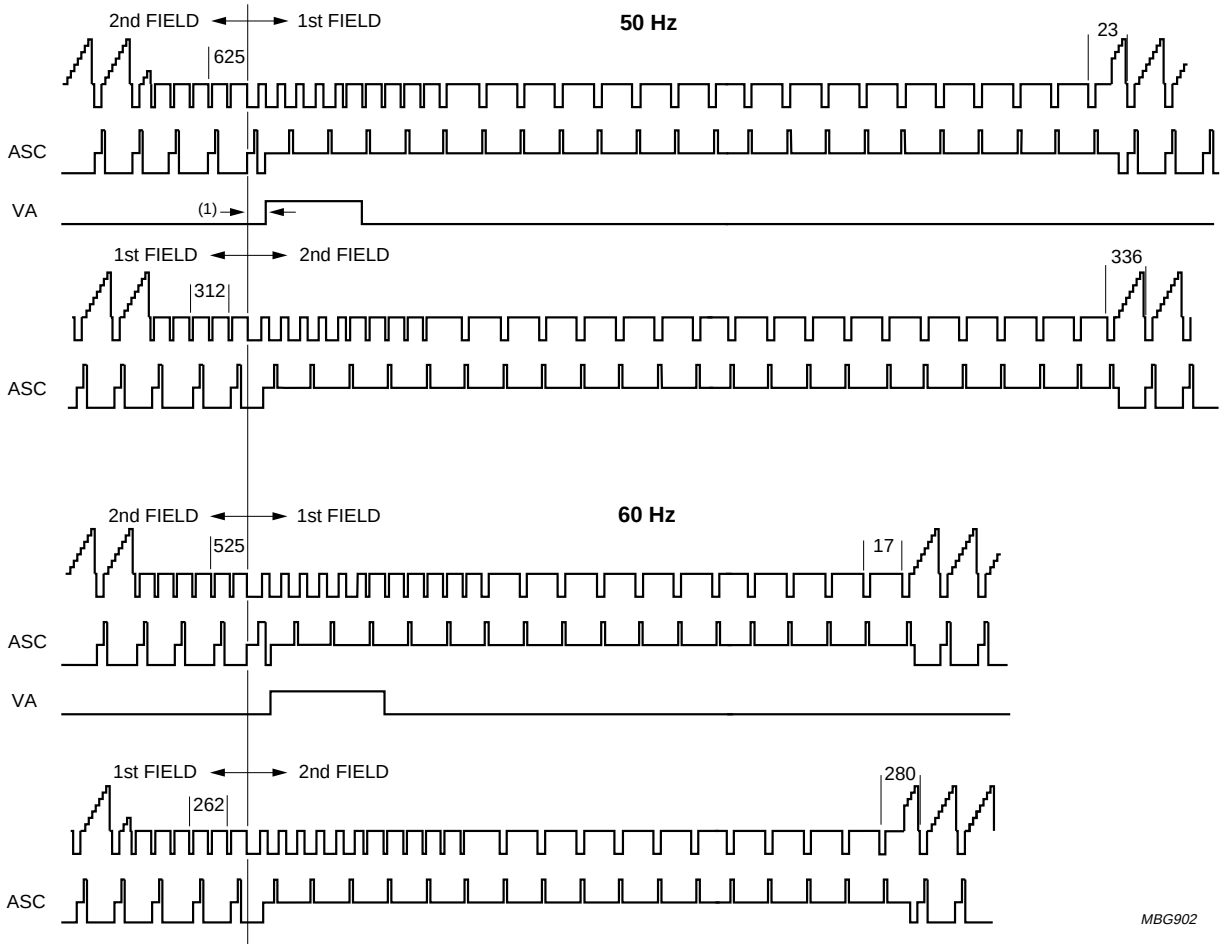
Fig.6 State diagram of the norm counter.

Output port and in/output port

Two stand-alone ports are available for external use. These ports are I²C-bus controlled, the output port by bus bit OPB and the input/output port by bus bit OPA. Bus bit OPA is an open-drain output, to enable input port functionality. The pin status is read out by bus via output bit IP.

Sandcastle

Figure 7 illustrates the timing of the acquisition sandcastle (ASC) and the VA pulse with respect to the input signal. The sandcastle signal is according to the two-level 5 V sandcastle format. An external vertical guard current can overrule the sink current to enable blanking purposes.



(1) See Vertical Section in “Characteristics”

Fig.7 Acquisition sandcastle signal and VA pulse timing diagram.

I²C-bus

For address 8A, an unconnected pin 22 is sufficient as this pin is also a CVBS output. Do not short-circuit the input to ground. If the address input is connected to the positive supply rail, the address changes from 8A to 8E.

Table 2 Slave address (8A)

SLAVE ADDRESS	A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
8A	1	0	0	0	1	X	1	X

Valid subaddresses: 00 to 03 and 17 to 18 (Hex).
Only the five least significant bits of the subaddress bytes are recognized. Auto-increment mode is available for subaddresses. The output addresses 00 and 01 can only be read in auto-increment mode. The I²C-bus transceiver is designed for a maximum clock frequency (f_{SCL}) of 100 kHz.

Table 3 Input bytes

SUB ADDRESS	MSB			DATA BYTE				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
00	INA	INB	TB	ECMB	FOA	FOB	XA	XB
01	FORF	FORS	OPA	OPB	POC	FM	SAF	FRQF
02	EFS	ECL	HU5	HU4	HU3	HU2	HU1	HU0
03	LCA	FWW	–	–	–	–	–	–
.	.	.	.	.	.	.	.	.
17	–	–	HOB	HBC	BSY	–	–	–
18	BPS	LPS	FRGB	EMG	YD3	YD2	YD1	YD0

Table 4 Output (status) bytes

OUTPUT ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
00	POR	FSI	YC	SL	IP	SAK	SBK	FRQ
01	–	–	–	FBA	NRM	SNR	SXA	SXB

Start up procedure: read the status byte until POR = 0; send subaddress 18 with the LPS bit indicating normal operation (LPS = 0); send subaddress 00 with the crystal indicator bits (XA and XB) indicating that only one crystal is connected to the IC(1); wait for 50 ms; send subaddress 01; wait for at least 50 ms; set XA,XB to the actual crystal configuration.

Each time before the data in the IC is refreshed, the status byte must be read. If POR = 1, then the above procedure must be carried out to restart the IC. As long as POR = 1, sending subaddress 01 does not start the line oscillator calibration. POR is reset when the status register is read out and can only be reset when the supply voltages exceed the POR detection levels mentioned in the Bias Generator characteristics (see Chapter “Characteristics”).
Failure to stick to the above procedure may result in an incorrect horizontal frequency after power-up or a power-dip.

Remark: if the presence of output signals HA/CLP and/or VA is required after power-up of the IC, subaddress 02 with the ECL bit indicating ECL = 0 must be sent before sending subaddress 00.

(1) To be absolutely sure that the line oscillator is calibrated with the appropriate crystal frequency data, it is possible to check the received values of the crystal indication bits via status bits SXA and SXB.

INPUT SIGNALS

Table 5 Source select; note 1

INA	INB	SOURCE
0	0	CVBS
0	1	YC
1	–	auto CVBS/YC

Note

1. When ECMB = 1 and no current is drawn from the Fscomb pin, source select is forced to be YC.

Table 6 Trap bypass; note 1

TB	CONDITION
0	trap not bypassed
1	trap bypassed

Note

1. The chrominance trap is always bypassed in YC mode.

Table 7 Comb filter enable

ECMB	CONDITION
0	comb filter disabled
1	comb filter enabled

Table 8 φ_1 time constant

FOA	FOB	MODE
0	0	auto
0	1	slow
1	–	fast

Table 9 Crystal indication

XA	XB	CRYSTAL
0	0	2×3.6 MHz
0	1	1×3.6 MHz
1	0	1×4.4 MHz
1	1	1×3.6 MHz and 1×4.4 MHz

Table 10 Forced field frequency

FORF	FORS	FIELD FREQUENCY
0	0	auto; 60 Hz if no lock
0	1	60 Hz
1	0	50 Hz
1	1	auto; 50 Hz if no lock

Table 11 Output value I/O port

OPA	LEVEL
0	LOW
1	HIGH

Table 12 Output value O port

OPB	LEVEL
0	LOW
1	HIGH

Table 13 φ_1 loop control

POC	CONDITION
0	φ_1 loop closed
1	φ_1 loop open

Table 14 Forced standard; note 1

FM	SAF	FRQF	STANDARD
0	–	–	auto search
1	0	0	PAL/NTSC second crystal
1	0	1	PAL/NTSC reference crystal
1	1	0	black and white
1	1	1	SECAM reference crystal

Note

1. If XA and XB indicate that only one crystal is connected to the IC and FM and FRQF force it to use the second crystal, then colour will be switched off. When SAF = 0, SECAM 60 Hz is disabled; when SAF = 1, SECAM 60 Hz is enabled.

Table 15 Enable fast switch

EFS	CONDITION
0	fast switch disabled
1	fast switch enabled, when FRGB = 0

Table 16 External RGB clamp mode

ECL	CONDITION
0	off; internal clamp pulse is used
1	on; external clamp pulse has to be supplied to CLP pin

Table 17 Forced RGB mode

FRGB	CONDITION
0	YUV, when disabled via EFS
1	forced RGB

Table 18 YUV outputs as a function of EFS, FRGB and Fast switch F

EFS	FRGB	F	SELECTED INPUTS
0	0	–	YUV
–	1	–	RGB
1	0	0	YUV
1	0	1	RGB

Table 19 Hue

FUNCTION	ADDRESS	DIGITAL NUMBER
Hue	HU5 to HU0	000000 = –45°
		111111 = +45°

Table 20 Line-locked clock active

LCA	CONDITION
0	OPB/CLP mode
1	LLC/HA mode

Table 21 Forced wide window

FWW	CONDITION
0	auto window mode
1	forced wide window

Table 22 PALplus/EDTV-2 helper blanking (Y, U, V)

HOB	HBC	SNR	BLANKING
0	–	–	off
1	0	–	on
1	1	0	off
1	1	1	on

Table 23 Blanked sync on Y_{out}

BSY	CONDITION
0	unblanked sync
1	blanked sync

Table 24 Baseband delay line bypass; note 1.

BPS	CONDITION
0	no bypass
1	baseband delay line bypassed

Note

1. SECAM cannot be bypassed.

Table 25 Low power standby mode

LPS	CONDITION
0	normal operation
1	low power standby

Table 26 Enable MACROVISION gating

EMG	CONDITION
0	disable gating
1	enable gating

Table 27 Luminance delay control

YD3 to YD0	CONDITION
0000	–280 ns
1111	+160 ns

OUTPUT SIGNALS

Table 28 Power-on reset

POR	CONDITION
0	normal mode
1	power-down mode

Table 29 Field frequency indication

FSI	CONDITION
0	50 Hz
1	60 Hz

Table 30 Input switch mode

YC	CONDITION
0	CVBS mode
1	Y/C mode

Table 31 φ_1 lock indication

SL	CONDITION
0	not locked
1	locked

Table 32 Input value I/O port

IP	LEVEL
0	LOW
1	HIGH

Table 33 Standard read-out

SAK	SBK	FRQ	STANDARD
0	0	0	PAL second crystal
0	0	1	PAL reference crystal
0	1	0	NTSC second crystal
0	1	1	NTSC reference crystal
1	0	0	illegal forced mode
1	0	1	SECAM reference crystal
1	1	–	colour off

Table 34 Fast blanking active

FBA	CONDITION
0	no fast blanking detected
1	fast blanking detected

Table 35 Norm/no_norm indication in vertical divider system

NRM	CONDITION
0	no_norm or near_norm
1	norm

Table 36 Signal-to-noise ratio

SNR	CONDITION
0	S/N > 20 dB
1	S/N < 20 dB

Table 37 Crystal indication read-out

SXA	SXB	CRYSTAL
0	0	2×3.6 MHz
0	1	1×3.6 MHz
1	0	1×4.4 MHz
1	1	1×3.6 MHz and 1×4.4 MHz

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		–	–	9.0	V
I_{CC}	supply current		–	–	70	mA
P_{tot}	total power dissipation		–	–	630	mW
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		–10	–	+70	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	48	K/W

QUALITY SPECIFICATION

Quality level in accordance with *"SNW-FQ-611-E"* is applicable for ESD protection, human body model: ±3000 V, 100 pF, 1500 Ω on all pins. Machine model: ±300 V, 200 pF, 0 Ω on all pins. The number of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9397 750 00192.

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; I²C-bus address 8A; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 7)						
V_{CC}	supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current		50	60	70	mA
P_{tot}	total power dissipation		360	480	620	mW
I_{CC}	low power supply current		12	16	22	mA
Input switch						
Caution: the voltage on pin 25 must never exceed 5.5 V, if it does, the IC enters a test mode						
Y/CVBS INPUT (PIN 26)						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	top sync-white	–	1.0	1.43	V
Z_i	input impedance		60	–	–	kΩ
C_i	input capacitance		–	–	5	pF
$I_{i(bias)}$	input bias current		–	3.3	–	μA
C INPUT (PIN 25)						
$V_{i(p-p)}$	input burst voltage (peak-to-peak value)		–	0.3	0.6	V
Z_i	input impedance		60	–	–	kΩ
C_i	input capacitance		–	–	5	pF
CVBS OUTPUT (PIN 22); ONLY FOR ADDRESS 8A						
$V_{o(p-p)}$	output voltage (peak-to-peak value)	top sync-white	–	1.0	–	V
Z_o	output impedance		–	–	500	Ω
B	bandwidth at –3 dB	C_L = 15 pF	7	–	–	MHz
V_{tsl}	top-sync voltage level		2.2	2.8	3.4	V
Bias generator (pin 8)						
$V_{D(DEC)}$	digital supply voltage		4.8	5.0	5.2	V
$V_{det(CC)}$	POR detection level for power supply		5.7	6.0	6.3	V
$V_{det(DEC)}$	POR detection level for DEC pin		4.0	4.3	4.6	V
$I_{L(DEC)}$	current load on digital supply	sum of pins 8, 11, 16, 17	–	–	2.0	mA
Subcarrier regeneration						
GENERAL; note 1						
CR	catching and holding range					
	reference crystal		±500	–	–	Hz
	second crystal		±450	–	–	Hz
φ	phase shift for 80% deviation of catching range		–	–	5	deg
Z_i	input impedance					
	reference crystal and second crystal		0.80	1.00	1.20	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FSCOMB OUTPUT (PIN 23)						
$V_{sub(p-p)}$	subcarrier output voltage amplitude (peak-to-peak value)	C_L = 15 pF	150	200	300	mV
V_{cen}	comb enable voltage level		4.0	4.2	5.0	V
V_{cdis}	comb disable voltage level		–	0.1	1.4	V
I_{sink}	sink current to undo forced Y/C mode of input switch		0.4	–	1.0	mA
R_{GND}	value of grounded resistor to undo forced Y/C mode of input switch		4	–	10	kΩ
ACC						
	ACC control range		–20	–	+6	dB
	change of –(R–Y) and –(B–Y) signals over range		–	–	1	dB
	colour killer treshold					
	PAL/NTSC		–34	–31	–28	dB
	SECAM		–31	–28	–25	dB
	kill/unkill hysteresis		–	3	–	dB
Demodulators –(R–Y) and –(B–Y) outputs (pins 1 and 2)						
GENERAL						
	ratio of –(B–Y) to –(R–Y)	standard colour bar	1.20	1.27	1.34	
TC	temperature coefficient of –(R–Y) and –(B–Y) amplitude		–	–	0.1	%/K
	spread of –(R–Y) to –(B–Y) ratio between standards		–1	–	+1	dB
$V_{-(R-Y)}$	output level of –(R–Y) output during blanking level		1.7	2.1	2.5	V
$V_{-(B-Y)}$	output level of –(B–Y) output during blanking level		1.7	2.0	2.5	V
B	bandwidth at –3 dB		600	670	750	kHz
Z_o	output impedance		–	–	500	Ω
ΔV_{CC}	supply voltage dependence		–	–	2	%/V
φ	hue phase shift (NTSC only)		±35	±45	±55	deg
PAL/NTSC DEMODULATOR						
$V_{-(R-Y)(p-p)}$	–(R–Y) output voltage (peak-to-peak value)	standard colour bar	480	540	605	mV
$V_{-(B-Y)(p-p)}$	–(B–Y) output voltage (peak-to-peak value)	standard colour bar	610	685	765	mV
$V_{res(p-p)}$	8.8 MHz residue (peak-to-peak value)	both outputs	–	–	15	mV
$V_{res(p-p)}$	7.2 MHz residue (peak-to-peak value)	both outputs	–	–	20	mV
$V_{res(p-p)}$	4.4 and 3.6 MHz residue	both outputs	–	–	tbf	mV
S/N	signal-to-noise ratio	0 to 1 MHz	46	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAL DEMODULATOR						
$V_{R(p-p)}$	½H ripple (peak-to-peak value)		–	–	20	mV
φ	demodulator phase error		–	–	5	deg
SECAM DEMODULATOR						
$V_{-(R-Y)(p-p)}$	–(R–Y) output voltage (peak-to-peak value)	standard colour bar	0.96	1.08	1.21	V
$V_{-(B-Y)(p-p)}$	–(B–Y) output voltage (peak-to-peak value)	standard colour bar	1.22	1.37	1.53	V
f_{os}	black level offset frequency		–	–	7	kHz
S/N	signal-to-noise ratio	0 to 1 MHz	40	–	–	dB
$V_{res(p-p)}$	7.8 MHz to 9.4 MHz residue (peak-to-peak value)		–	–	30	mV
f_{pole}	pole frequency of de-emphasis		77	85	93	kHz
	ratio of pole and zero frequency		–	3	–	
V_{cal}	calibration voltage		3	4	5	V
NL	non linearity		–	–	3	%
Filters						
TUNING						
V_{tune}	tuning voltage		1.5	3	6	V
LUMINANCE DELAY; YD3 to YD0 = 1011						
$t_{d(on)}$	delay time colour on	f_{sc} = 3.6 MHz; TB = 0	555	580	605	ns
		f_{sc} = 3.6 MHz and 4.4 MHz; TB = 1	515	540	565	ns
$t_{d(off)}$	delay time colour off		350	370	390	ns
$t_{d(tun)}$	delay time tuning range	15 steps YD3 to YD0; note 2	–280	–	+160	ns
CHROMINANCE TRAP						
f_o	notch frequency	f_{sc} = 3.6 MHz	3.53	3.58	3.63	MHz
		f_{sc} = 4.4 MHz	4.37	4.43	4.49	MHz
		SECAM	4.23	4.29	4.35	MHz
		Y/C and B/W mode	not active			
B	bandwidth at –3 dB	f_{sc} = 3.6 MHz	2.60	2.80	3.00	MHz
		f_{sc} = 4.4 MHz	3.20	3.50	3.80	MHz
		SECAM	2.90	3.20	3.50	MHz
$f_{sc(sup)}$	subcarrier suppression		26	–	–	dB
CHROMINANCE BANDPASS						
f_{res}	resonant frequency	f_{sc} = 3.6 MHz	3.40	3.58	3.76	MHz
		f_{sc} = 4.4 MHz	4.21	4.43	4.65	MHz
B	bandwidth at –3 dB	f_{sc} = 3.6 MHz	1.05	1.20	1.35	MHz
		f_{sc} = 4.4 MHz	1.25	1.40	1.55	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CLOCHE FILTER						
f_{res}	resonant frequency	SECAM	4.26	4.29	4.31	MHz
B	bandwidth at −3 dB	SECAM	241	268	295	kHz
Sync input (pin 26)						
VIDEO INPUT						
$V_{Y/CVBS(p-p)}$	sync pulse amplitude (peak-to-peak value)		35	300	600	mV
	slicing level		40	47	55	%
t_d	delay of sync pulse due to internal filter		0.2	0.3	0.4	µs
N_{th}	noise detector threshold level		18	20	22	dB
H	hysteresis		2	3	5	dB
t_d	delay between internally separated vertical sync pulse and video signal		12	18.5	27	µs
Horizontal section						
CLP OUTPUT (OPB/CLP MODE); HA OUTPUT (LLC/HA) MODE (BOTH ON PIN 17)						
V_{OH}	HIGH level output voltage		4.0	5	5.5	V
V_{OL}	LOW level output voltage		–	0.2	0.4	V
I_{sink}	sink current		2	–	–	mA
I_{source}	source current		2	–	–	mA
$t_{W(HA)}$	HA pulse width (32 LLC pulses)		–	4.65	–	µs
t_d	delay between middle of horizontal sync pulse and middle of HA	note 3	0.3	0.45	0.6	µs
$t_{W(CLP)}$	CLP pulse width (25 LLC pulses)		–	3.65	–	µs
t_d	delay between middle of horizontal sync pulse and start of CLP pulse	note 3	3.0	3.2	3.4	µs
σ	6σ jitter	φ_1 in auto mode	–	–	5	ns
FIRST LOOP (φ_1)						
Δf	frequency deviation when not locked		–	–	1.5	%
ΔV_{CC}	supply voltage dependence		–	40	–	Hz/V
f_{CR}	catching range		±625	–	–	Hz
f_{HR}	holding range		–	–	±1.0	kHz
ϕ	static phase shift		–	–	0.1	µs/kHz
LLC OUTPUT (PIN 16); LLC/HA MODE						
f_o	output frequency					
	$440 \times f_H$	50 Hz standard	–	6.875	–	MHz
	$440 \times f_H$	60 Hz standard	–	6.923	–	MHz
$V_{o(p-p)}$	output amplitude (peak-to-peak value)		0.25	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_o	DC output voltage level		–	2.5	–	V
t_d	delay between negative edge of LLC and positive edge of HA pulse	C_L = 15 pF	10	20	40	ns
Vertical section						
VERTICAL OSCILLATOR						
f_{fr}	free running frequency	FORF = 1; divider ratio 628	–	50	–	Hz
		FORF = 0; divider ratio 528	–	60	–	Hz
f_{LR}	frequency locking range		43	–	64	Hz
LR	divider locking range		488	625	722	
VA OUTPUT (PIN 11); ECL = 0						
V_{OH}	HIGH level output voltage		4.0	5	5.5	V
V_{OL}	LOW level output voltage		–	0.2	0.4	V
I_{sink}	sink current		2	–	–	mA
I_{source}	source current		2	–	–	mA
$t_{W(VA)}$	VA pulse width					
	$2.5/f_H$	50 Hz standard	–	160	–	µs
	$3/f_H$	60 Hz standard	–	192	–	µs
t_d	delay between start of vertical sync pulse and positive edge of VA	note 4; see Fig.7	–	35	–	µs
Z_o	output impedance	ECL = 1	3	–	–	MΩ
Sandcastle output (pin 10)						
V_o	zero level output voltage		0	0.5	1	V
I_{sink}	sink current		0.5	0.7	0.9	mA
HORIZONTAL AND VERTICAL BLANKING						
V_{bl}	blanking voltage level		2.2	2.5	2.8	V
I_{source}	source current		0.5	0.7	0.9	mA
I_{ext}	external current required to force the output to the blanking level		1.0	–	3.0	mA
$t_{W(H)}$	horizontal blanking pulse width	69 LLC pulses	–	10.0	–	µs
t_d	delay between start of horizontal blanking and start of clamping pulse	44 LLC pulses	–	6.4	–	µs
CLAMPING PULSE						
V_{clamp}	clamping voltage level		4.2	4.5	4.8	V
I_{source}	source current		0.5	0.7	0.9	mA
$t_{W(clamp)}$	clamping pulse width	25 LLC pulses	–	3.6	–	µs
t_d	delay between middle sync of input and start of clamping pulse	note 3	3.0	3.2	3.4	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
YUV/RGB switches; note 5						
Caution: the voltage on pin 3 must never exceed 5.5 V, if it does, the IC enters a test mode						
RGB INPUTS (PINS 21, 20, AND 19 RESPECTIVELY); note 5						
$V_{i(p-p)}$	input voltage (peak-to-peak value)		–	0.7	1	V
Z_i	input impedance		3	–	–	MΩ
C_i	input capacitance		–	–	5	pF
UV INPUTS (PINS 3 AND 4 RESPECTIVELY); note 5						
$V_{i(p-p)}$	U input voltage (peak-to-peak value)		–	1.33	1.90	V
$V_{i(p-p)}$	V input voltage (peak-to-peak value)		–	1.05	1.50	V
Z_i	input impedance (both inputs)		3	–	–	MΩ
C_i	input capacitance (both inputs)		–	–	5	pF
Y OUTPUT (PIN 12)						
$V_{o(p-p)}$	U output voltage	black-white	–	1.00	–	V
$V_{o(p-p)}$	PALplus output voltage	black-white	–	0.80	–	V
Z_o	output impedance		–	–	250	Ω
V_o	DC output voltage level	black level	2.7	3.0	3.3	V
S/N	signal-to-noise ratio	f = 0 to 5 MHz	–	52	–	dB
V_{os}	offset voltage Y_{black} to re-inserted black		–	–	10	mV
G_v	voltage gain from $Y/CVBS_i$ to Y_o		 1.35	 1.43	 1.50	
UV OUTPUTS (PINS 14 AND 13); note 5						
$V_{o(p-p)}$	U output voltage (peak-to-peak value)		–	1.33	1.90	V
$V_{o(p-p)}$	V output voltage (peak-to-peak value)		–	1.05	1.50	V
Z_o	output impedance (both outputs)		–	–	250	Ω
V_o	DC output voltage level		2.3	2.6	2.9	V
G_v	voltage gain from U_{in} to U_{out} from V_{in} to V_{out}		 0.94 0.94	 0.97 0.97	 1.00 1.00	
GENERAL						
V_{diff}	difference between black levels of YUV outputs in RGB mode and YUV mode	sync locked mixed RGB/YUV via fast blanking	–	–	10	mV
NL	non-linearity	any input to any output	–	–	5	%
B	bandwidth at –3 dB	any input to any output; C_L = 15 pF	7	–	–	MHz
α_c	crosstalk between RGB and UV_{in} signals on UV_{out}	f = 0 to 5 MHz	–	–	–50	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B	bandwidth at –1 dB	any input to any output; C_L = 15 pF	5	–	–	MHz
t_{clamp}	internal Y clamping time constant		–	10	–	ms
FAST SWITCH F (PIN 18)						
V_{IL}	LOW level input voltage	UV switched on	0	–	0.5	V
V_{IH}	HIGH level input voltage	RGB switched on	0.9	–	3.0	V
t_d	switching delay	between F and YUV	–	–	20	ns
EXTERNAL CLAMP INPUT (PIN 17)						
V_{IL}	LOW level input voltage (pin CLP)	no clamping	0	–	0.6	V
V_{IH}	HIGH level input voltage (pin CLP)	clamping	2.4	–	5.5	V
$t_{W(clamp)}$	clamping pulse width	note 6	1.8	3.5	–	µs
$V_{os(clamp)}$	clamping offset voltage on UV outputs		–	–	10	mV
Z_i	input impedance	ECL = 1	3	–	–	MΩ
Colour matrix						
G_v	voltage gain					
	from R to Y_{out}		0.41	0.43	0.45	
	from G to Y_{out}		0.80	0.84	0.88	
	from B to Y_{out}		0.15	0.16	0.17	
	from R to U_{out}		0.41	0.43	0.45	
	from G to U_{out}		0.80	0.84	0.88	
	from B to U_{out}		1.21	1.27	1.33	
	from R to V_{out}		0.95	1.00	1.05	
	from G to V_{out}		0.80	0.84	0.88	
	from B to V_{out}		0.15	0.16	0.17	
Output and in/output port						
O PORT (PIN 16); OPB/CLP MODE						
V_{OH}	HIGH level output voltage		4.0	5	5.5	V
V_{OL}	LOW level output voltage		–	0.2	0.4	V
I_{sink}	sink current		100	–	–	µA
I_{source}	source current		100	–	–	µA
I/O PORT; OPB/CLP MODE						
V_{OH}	HIGH level output voltage		–	–	V_{CC}	V
V_{OL}	LOW level output voltage		–	0.2	0.4	V
I_{sink}	sink current		2	–	–	mA
V_{IH}	HIGH level input voltage		2.0	–	–	V
V_{IL}	LOW level input voltage		–	–	0.6	V

Notes to the characteristics

1. All frequency variations are referred to 3.58 MHz or 4.43 MHz carrier frequency. All oscillator specifications are measured with the Philips crystal series 9920 520 0047x and 9920 520 0048x. The oscillator circuit is insensitive to the spurious responses of the crystal. The typical crystal parameters for the crystals mentioned above are:
   a) Load resonance frequency f_0 = 4.433619 MHz or 3.579545 MHz (C_L = 20 pF).
   b) Motional capacitance $C_M = 20.6 \times f_F$ (4.43 MHz crystal) or $14.7 \times f_F$ (3.58 MHz crystal).
   c) Parallel capacitance C_0 = 5 pF for both crystals.
   d) The minimum detuning range can only be specified if both the IC and the crystal tolerances are known and the general specifications given for the subcarrier regeneration are therefore valid for the specified crystal series. In the figure tolerances of the crystal with respect to nominal frequency, motional capacitance and ageing have been taken into account and have been counted for by Gaussian addition.
   Whenever different typical crystal parameters are used, the following equation might be helpful for calculating the impact on the detuning capabilities:
   e) Detuning range proportional to: $\frac{C_M}{\left(1 + \frac{C_O}{C_L}\right)^2}$
   f) The resulting detuning range should be corrected for temperature shift and supply deviation of both the IC and the crystal. For the above mentioned crystals, the actual load capacitance in the application should be C_L = 18 pF to account for parasitic capacitance on and off chip. For 3-norm applications with two crystals connected to one pin, the maximum load capacitance of the crystal pin should not exceed 12 pF.
2. YD3 and YD2 are equal significant bits, both representing a 160 ns delay step. YD1 represents 80 ns and YD0 represents a 40 ns delay step.
3. This delay is partially caused by the low-pass filter at the sync separator input.
4. The delay between the positive edge of VA and the first negative edge of HA (or positive edge of CLP) after VA is 34.5 μs for field 1 and 2.5 μs for field 2 (17 LLC pulses with or without $\frac{1}{2 \times f_H}$ respectively).
5. The output signals of the demodulator are called –(R–Y) and –(B–Y) in this specification. The colour difference input and output signals of the YUV switch are called UV signals. However, these signals do not have the amplitude correction factor of real UV signals. They are called UV signals and not –(R–Y) and –(B–Y) to prevent confusion between the colour difference signals of the demodulator and the colour difference signals of the YUV switch.
6. The maximum external clamping pulse width is the minimum available blanking level time of the supplied RGB signals.

TEST AND APPLICATION INFORMATION

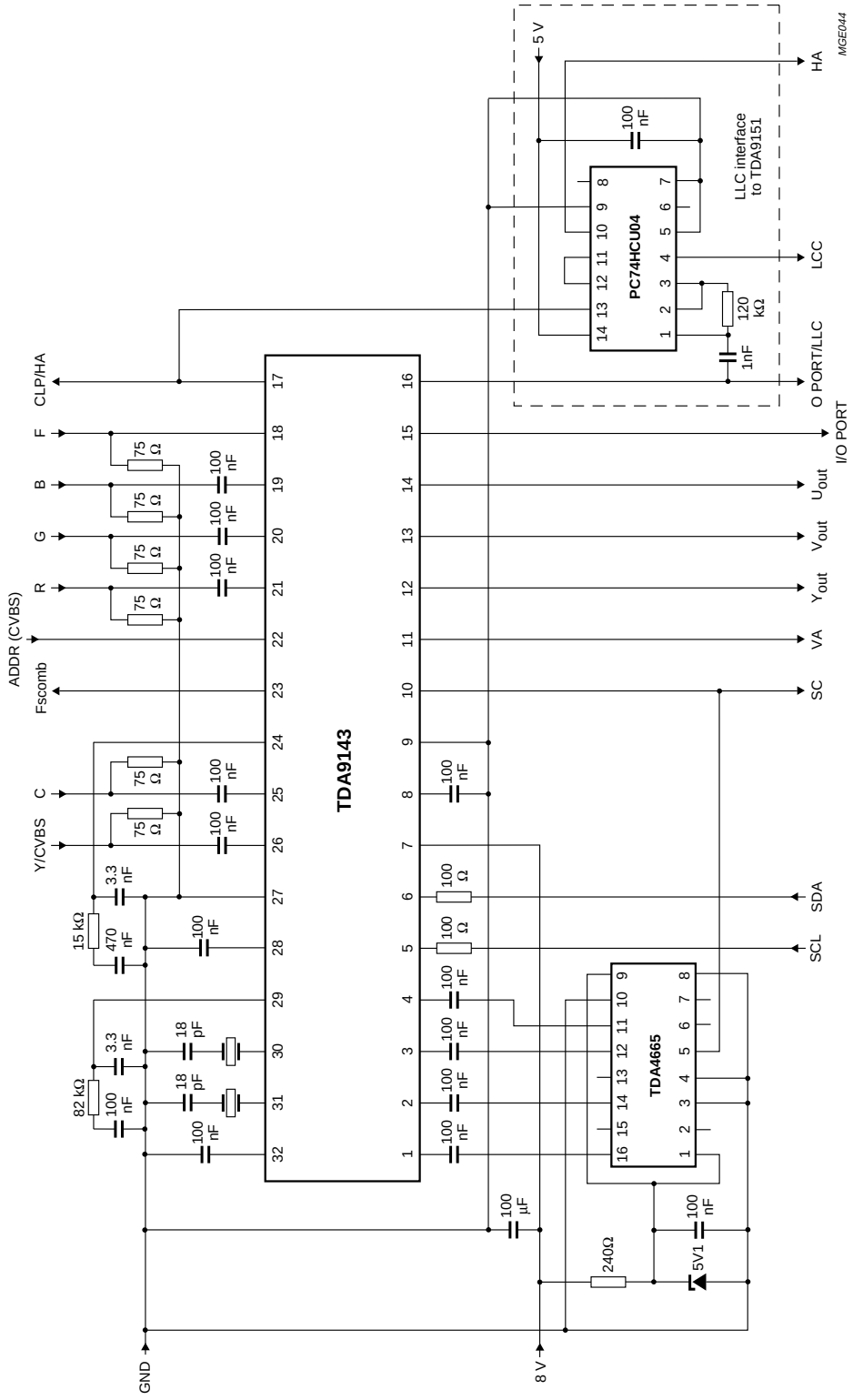
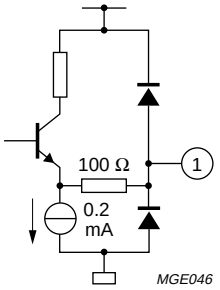
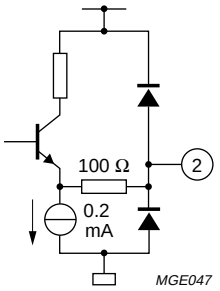
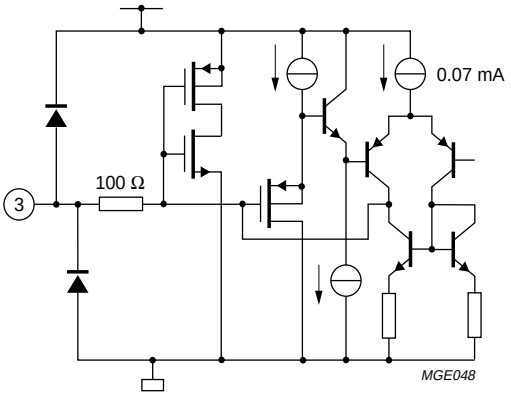
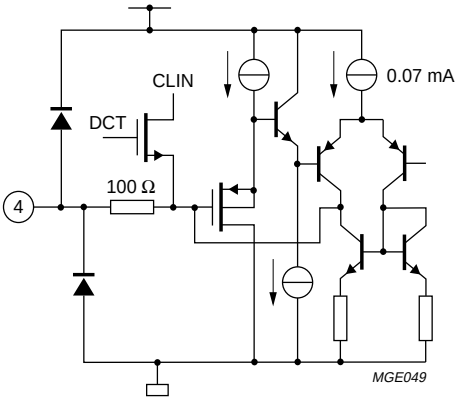
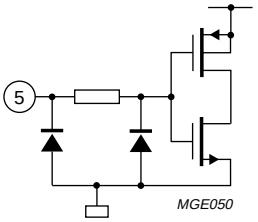
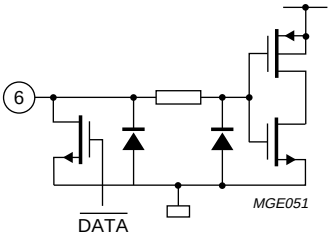
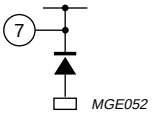
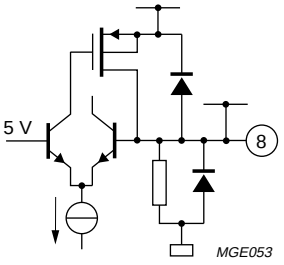


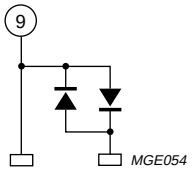
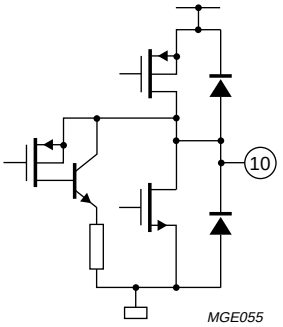
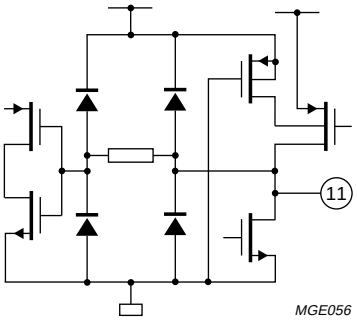
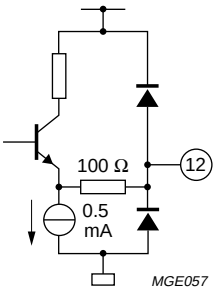
Fig.8 Application circuit.

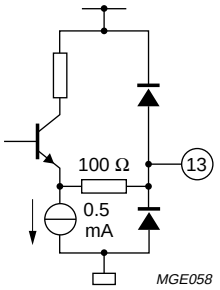
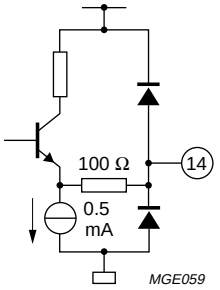
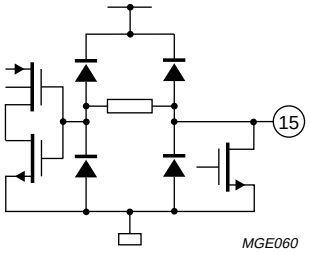
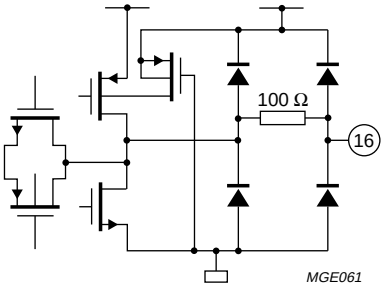
Pins 28 and 32 are sensitive to leakage currents.
Keep the analog and digital ground currents well separated.
The decoupling capacitor between pins 8 and 9 must be placed as close to the IC as possible.

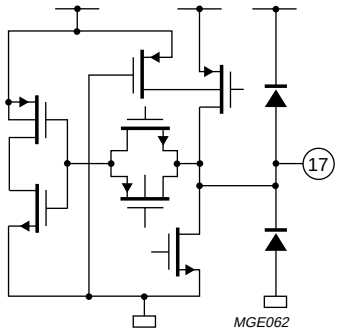
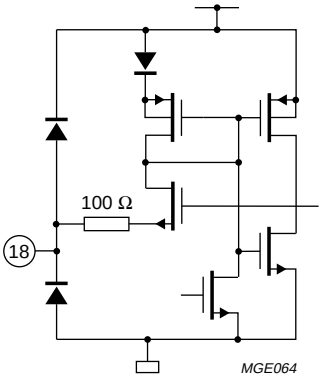
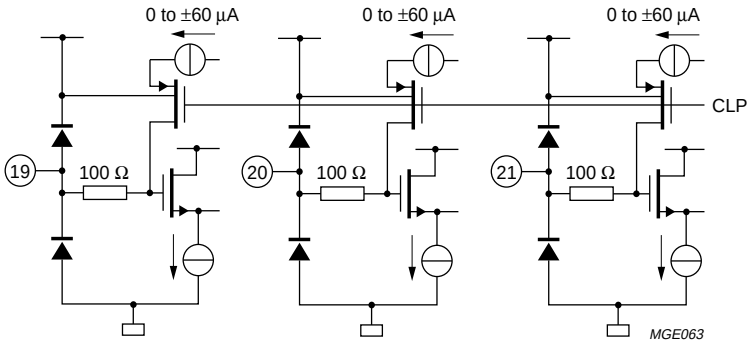
EQUIVALENT PIN CIRCUITS

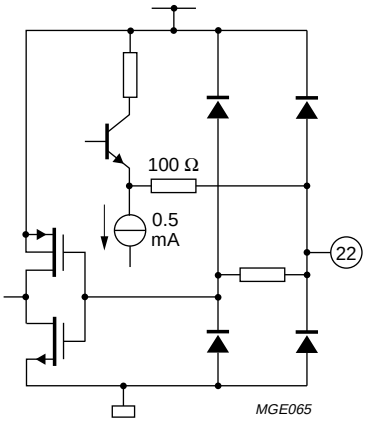
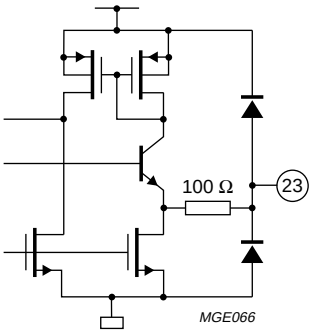
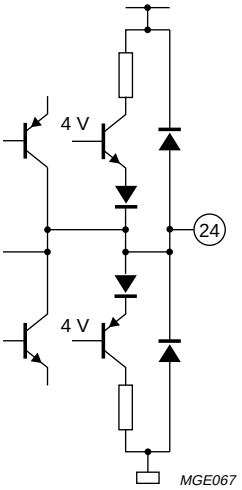
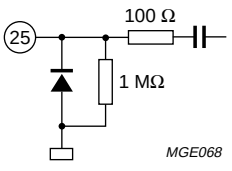
PIN	SYMBOL	EQUIVALENT PIN CIRCUIT
1	−(R−Y)	
2	−(B−Y)	
3	U_{in}	

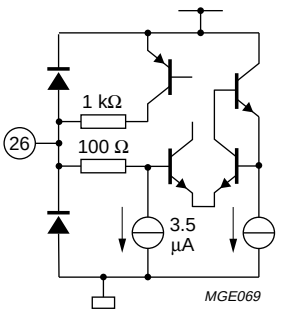
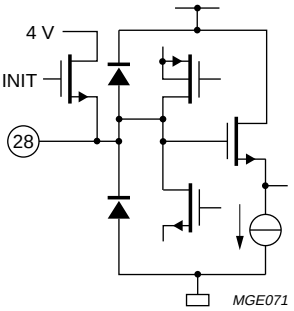
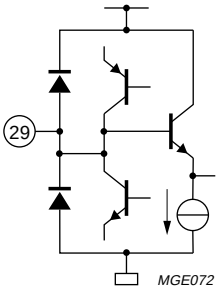
PIN	SYMBOL	EQUIVALENT PIN CIRCUIT
4	V_{in}	
5	SCL	
6	SDA	
7	V_{CC}	
8	DEC	

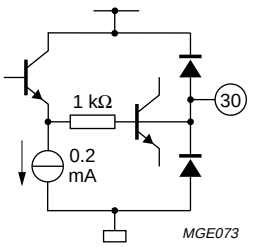
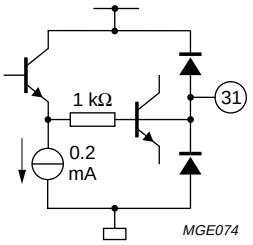
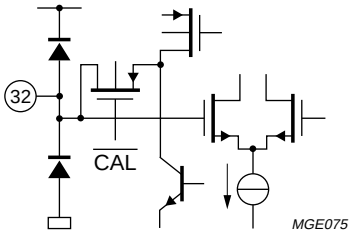
PIN	SYMBOL	EQUIVALENT PIN CIRCUIT
9	DGND	
10	SC	
11	VA	
12	Y_{out}	

PIN	SYMBOL	EQUIVALENT PIN CIRCUIT
13	V_{out}	
14	U_{out}	
15	I/O PORT	
16	O PORT/LLC	

PIN	SYMBOL	EQUIVALENT PIN CIRCUIT
17	CLP/HA	
18	F	
19	B	
20	G	
21	R	

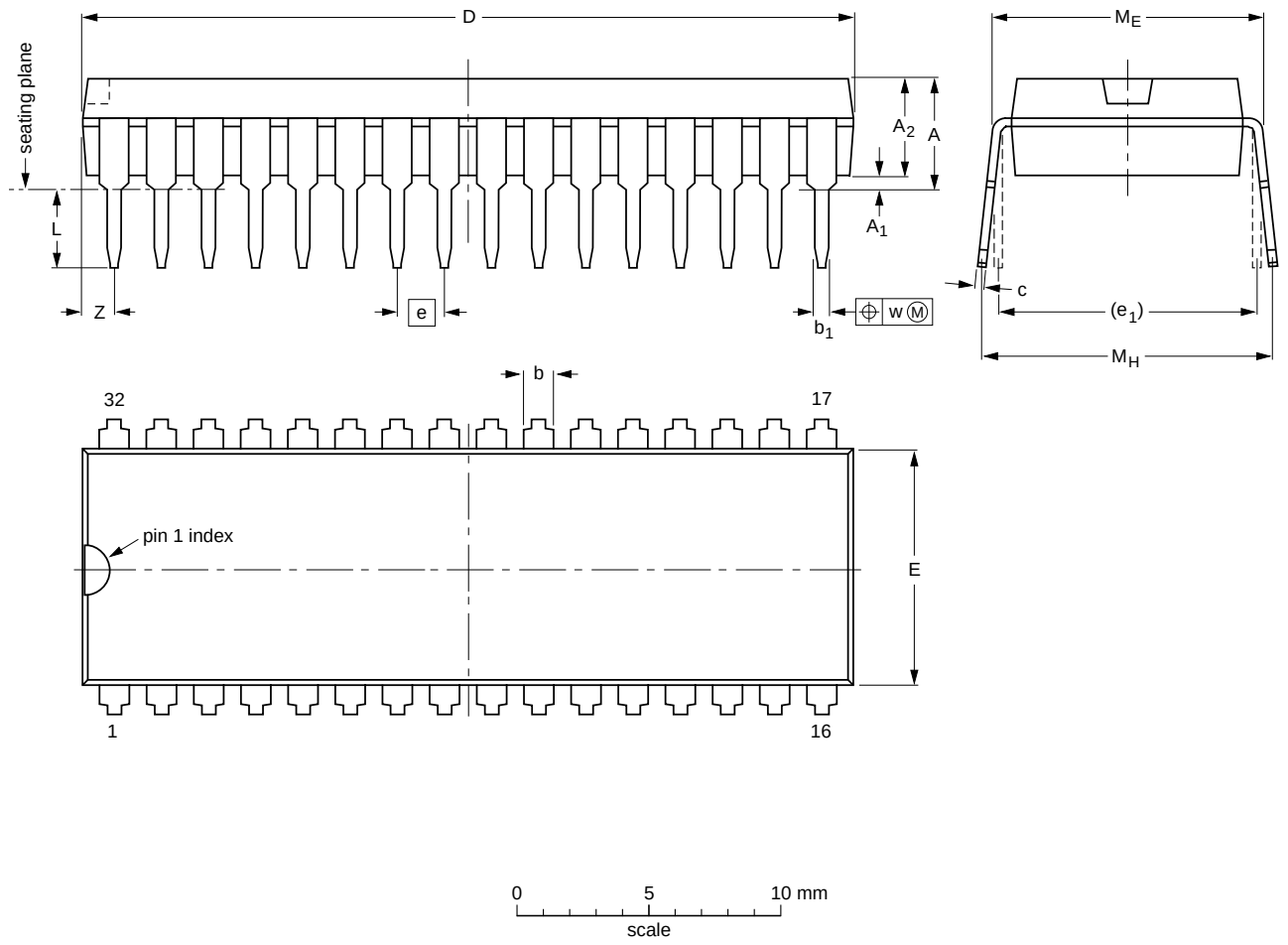
PIN	SYMBOL	EQUIVALENT PIN CIRCUIT
22	ADDR (CVBS)	
23	Fscomb	
24	HPLL	
25	C	

PIN	SYMBOL	EQUIVALENT PIN CIRCUIT
26	Y/CVBS	
27	AGND	analog ground
28	$FILT_{ref}$	
29	CPLL	

PIN	SYMBOL	EQUIVALENT PIN CIRCUIT
30	XTAL	
31	XTAL2	
32	SEC_{ref}	

PACKAGE OUTLINE

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.