# DATA SHEET

# TDA8786; TDA8786A
## 10-bit analog-to-digital interface for CCD cameras

Objective specification
File under Integrated Circuits, IC02

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Semiconductors

PHILIPS

# 10-bit analog-to-digital interface for CCD cameras

# TDA8786; TDA8786A

## FEATURES

- Correlated double sampling (CDS), AGC, soft clipper, pre- blanking, 10-bit ADC and reference regulator included
- Fully programmable via a 3-wire serial interface
- Sampling frequency up to 18 MHz
- AGC gain from 3.5 dB to 33.5 dB (in 0.1 dB steps)
- Programmable soft clipper for white compression (starting at 40% of the input signal)
- Standby mode available for each block for power saving applications
- 6 dB fixed gain analog output for analog iris control
- 8-bit and 10-bit DAC included for analog settings
- Low power consumption of only 400 mW (typ.)
- 5 V operation and 2.5 to 5 V operation for the digital outputs
- Active control pulse: TDA8786 = HIGH; TDA8786A = LOW
- TTL compatible inputs, TTL and CMOS compatible outputs.

## GENERAL DESCRIPTION

The TDA8786; TDA8786A is a 10-bit analog-to-digital interface for CCD cameras. The device includes a correlated double sampling circuit, AGC, a soft clipper circuit and a low power 10-bit analog-to-digital converter (ADC) together with its reference voltage regulator.

The AGC and soft clipper circuits are controlled by on-chip DACs via a serial interface.

A 10-bit DAC controls the ADC input clamp level.

A pre-blanking function is also included.

An additional DAC is provided for additional system controls; its output voltage range is 1 V (p-p) which is available at pin OFD.

## APPLICATIONS

- CCD camera systems.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{CCA}$ | analog supply voltage | | 4.5 | 4.75 | 5.5 | V |
| $V_{CCD}$ | digital supply voltage | | 4.5 | 4.75 | 5.5 | V |
| $V_{CCO}$ | digital outputs supply voltage | | 2.5 | 2.6 | 5.5 | V |
| $I_{CCA}$ | analog supply current | | – | 67 | – | mA |
| $I_{CCD}$ | digital supply current | | – | 15 | – | mA |
| $I_{CCO}$ | digital outputs supply current | $f_{CLK}$ = 18 MHz; $C_L$ = 20 pF; ramp input | – | 1 | – | mA |
| $ADC_{res}$ | ADC resolution | | – | 10 | – | bits |
| $V_{iCDS(p-p)}$ | CDS input voltage (peak-to-peak value) | | – | 400 | 1200 | mV |
| $G_{CDS}$ | CDS output amplifier gain | | – | 6 | – | dB |
| $f_{ss(max)}$ | maximum clock frequency | | 18 | – | – | MHz |
| $AGC_{dyn}$ | AGC dynamic range | | – | 30 | – | dB |
| $P_{tot}$ | total power consumption | | – | 400 | – | mW |

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| TDA8786 | LQFP48 | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |
| TDA8786A | | | |

## BLOCK DIAGRAM

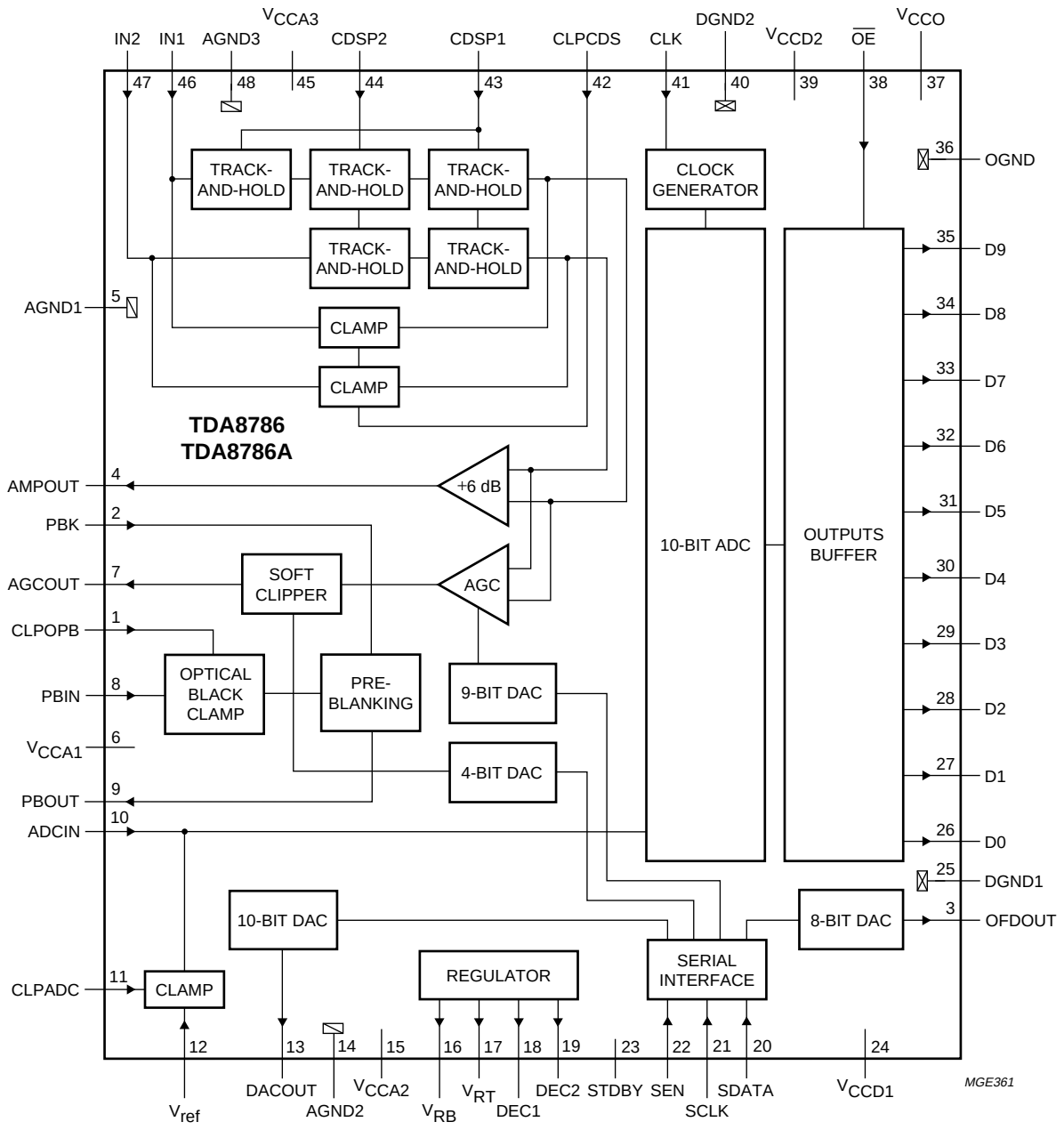



Fig.1 Block diagram.

**PINNING**

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| CLPOPB | 1 | optical black clamp control pulse input (active HIGH for TDA8786, active LOW for TDA8786A) |
| PBK | 2 | pre-blanking control pulse input; if PBK is HIGH (LOW) the signal is replaced by the optical black level for TDA8786 (TDA8786A) |
| OFDOUT | 3 | analog output of the additional 8-bit control DAC (controlled via the serial interface) |
| AMPOUT | 4 | CDS amplifier output (fixed gain = +6 dB) |
| AGND1 | 5 | analog ground 1 |
| $V_{CCA1}$ | 6 | analog supply voltage 1 |
| AGCOUT | 7 | AGC and soft clipper amplifier signal output |
| PBIN | 8 | optical black clamp and pre-blanking block signal input (from AGCOUT via a capacitor) |
| PBOUT | 9 | optical black clamp and pre-blanking block signal output |
| ADCIN | 10 | ADC analog signal input (from PBOUT or AGCOUT via a capacitor) |
| CLPADC | 11 | clamp control input for ADC analog input signal clamp (active HIGH for TDA8786 and active LOW for TDA8786A) |
| $V_{ref}$ | 12 | ADC input clamp reference voltage (normally connected to pin VRB or DACOUT) |
| DACOUT | 13 | DAC output for ADC clamp level |
| AGND2 | 14 | analog ground 2 |
| $V_{CCA2}$ | 15 | analog supply voltage 2 |
| $V_{RB}$ | 16 | ADC reference voltage (BOTTOM) code 0 |
| $V_{RT}$ | 17 | ADC reference voltage (TOP) code 1023 |
| DEC1 | 18 | decoupling 1 (decoupled to ground via a capacitor) |
| DEC2 | 19 | decoupling 2 (decoupled to ground via a capacitor) |
| SDATA | 20 | serial data input for the 4 control DACs (9-bit DAC for AGC gain, 4-bit DAC for soft clipper; additional 8-bit DAC for OFD output voltage; 10-bit DAC for ADC clamp level and the standby mode per block; see Table 1) |
| SCLK | 21 | serial clock input for the control DACs and their serial interface; see Table 1 |
| SEN | 22 | enable input for the serial interface shift register (active when SEN = logic 0); see Table 1 |
| STDBY | 23 | standby control pin (active HIGH); all the output bits are logic 0 when standby is enabled |
| $V_{CCD1}$ | 24 | digital supply voltage 1 |
| DGND1 | 25 | digital ground 1 |
| D0 | 26 | ADC digital output 0 (LSB) |
| D1 | 27 | ADC digital output 1 |
| D2 | 28 | ADC digital output 2 |
| D3 | 29 | ADC digital output 3 |
| D4 | 30 | ADC digital output 4 |
| D5 | 31 | ADC digital output 5 |
| D6 | 32 | ADC digital output 6 |
| D7 | 33 | ADC digital output 7 |
| D8 | 34 | ADC digital output 8 |
| D9 | 35 | ADC digital output 9 (MSB) |
| OGND | 36 | digital output ground |

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| $V_{CCO}$ | 37 | digital output supply voltage |
| $\overline{OE}$ | 38 | output enable (LOW: digital outputs active; HIGH: digital outputs high impedance) |
| $V_{CCD2}$ | 39 | digital supply voltage 2 |
| DGND2 | 40 | digital ground 2 |
| CLK | 41 | ADC clock input |
| CLPCDS | 42 | CDS clamp control input (active HIGH for TDA8786; active LOW for TDA8786A) |
| CDSP1 | 43 | CDS control pulse input 1 (active HIGH for TDA8786; active LOW for TDA8786A) |
| CDSP2 | 44 | CDS control pulse input 2 (active HIGH for TDA8786; active LOW for TDA8786A) |
| $V_{CCA3}$ | 45 | analog supply voltage 3 |
| IN1 | 46 | input signal 1 from CCD (usually black channel) |
| IN2 | 47 | input signal 2 from CCD (usually video channel) |
| AGND3 | 48 | analog ground 3 |

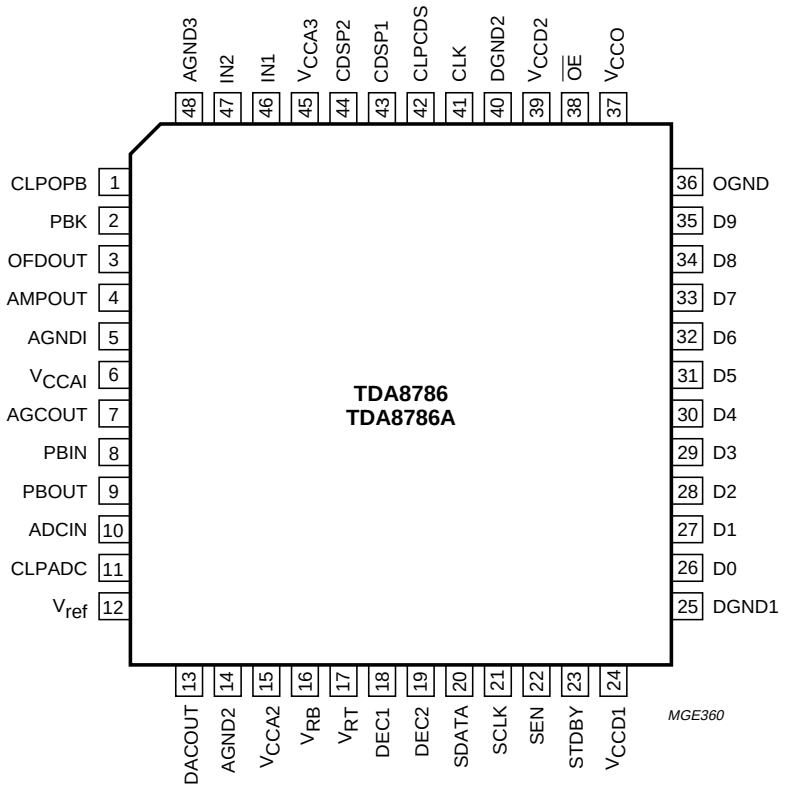



Fig.2 Pin configuration.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ | analog supply voltage | note 1 | –0.3 | +7.0 | V |
| $V_{CCD}$ | digital supply voltage | note 1 | –0.3 | +7.0 | V |
| $V_{CCO}$ | output stages supply voltage | note 1 | –0.3 | +7.0 | V |
| $\Delta V_{CC}$ | supply voltage difference | | | | |
| | between $V_{CCA}$ and $V_{CCD}$ | | –1.0 | +1.0 | V |
| | between $V_{CCA}$ and $V_{CCO}$ | | –1.0 | +4.0 | V |
| | between $V_{CCD}$ and $V_{CCO}$ | | –1.0 | +4.0 | V |
| $V_i$ | input voltage | referenced to $V_{SSA}$ | –0.3 | +7.0 | V |
| $V_{clk(p-p)}$ | AC input voltage for switching (peak-to peak-value) | referenced to $V_{SSD}$ | – | $V_{CCD}$ | V |
| $I_o$ | output current | | – | 10 | mA |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_{amb}$ | operating ambient temperature | | –20 | +75 | °C |
| $T_j$ | junction temperature | | – | 150 | °C |

**Note**

1. The supply voltages $V_{CCA}$, $V_{CCD}$ and $V_{CCO}$ may have any value between –0.3 and +7.0 V provided that the supply voltage difference $\Delta V_{CC}$ remains as indicated.

## HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---|---|---|---|
| $R_{th\ j-a}$ | thermal resistance from junction to ambient in free air | 76 (typ.) | K/W |

## CHARACTERISTICS

$V_{CCA}$ = $V_{CCD}$ = 4.75 V; $V_{CCO}$ = 2.6 V; $f_{CLK}$ = 18 Msps; $T_{amb}$ = 25 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{CCA}$ | analog supply voltage | | 4.5 | 4.75 | 5.5 | V |
| $V_{CCD}$ | digital supply voltage | | 4.5 | 4.75 | 5.5 | V |
| $V_{CCO}$ | supply voltage output | | 2.5 | 2.6 | 5.5 | V |
| $I_{CCA}$ | analog supply current | | – | 67 | – | mA |
| $I_{CCD}$ | digital supply current | | – | 15 | – | mA |
| $I_{CCO}$ | supply current output | $C_L$ = 20 pF on all data outputs; ramp input | – | 1 | – | mA |
| **Digital inputs** | | | | | | |
| CLOCK INPUT: CLK (REFERENCED TO DGND) | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | – | 0.6 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.2 | – | $V_{CCD}$ | V |
| $I_{IL}$ | LOW level input current | $V_{CLK}$ = 0.6 V | –1 | – | +1 | µA |
| $I_{IH}$ | HIGH level input current | $V_{CLK}$ = 2.2 V | – | – | 20 | µA |
| $Z_I$ | input impedance | $f_{CLK}$ = 18 MHz | – | 2 | – | kΩ |
| $C_I$ | input capacitance | $f_{CLK}$ = 18 MHz | – | 2 | – | pF |
| INPUTS: CDSP1 AND CDSP2 | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | – | 0.6 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.2 | – | $V_{CCD}$ | V |
| $I_{IL}$ | LOW level input current | $V_{IL}$ = 0.6 V | – | –100 | – | µA |
| $I_{IH}$ | HIGH level input current | $V_{IH}$ = 2.2 V | – | 0 | – | µA |
| INPUTS: SEN, STDBY, CLPCDS, CLPOPB, PBK AND CLPADC | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | – | 0.6 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.2 | – | $V_{CCD}$ | V |
| $I_i$ | input current | | –2 | – | +2 | µA |
| **Correlated double sampling; CDS** | | | | | | |
| $V_{iCDS(p-p)}$ | CDS input amplitude (peak-to-peak value) | | – | 400 | 1200 | mV |
| $I_{IN1,IN2}$ | input current pins 46 and 47 | | –2 | – | +2 | µA |
| $t_{CDS(min)}$ | CDS control pulses minimum active time (HIGH for TDA8786, LOW for TDA8786A) | $f_{iCDS1,2}$ = $f_{CLK(pix)}$ | 12 | – | – | ns |
| φ | CDSP1 phase with respect to CDSP2 phase | | – | 180 | – | deg |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Amplifier outputs** | | | | | | |
| $G_{AMPOUT}$ | output amplifier gain | | – | 6 | – | dB |
| $Z_{AMPOUT}$ | output amplifier impedance | | – | 300 | – | Ω |
| $V_{AGCOUT}$ | AGC output amplifier dynamic voltage level | | – | 1800 | – | mV |
| $Z_{AGCOUT}$ | AGC output amplifier output impedance | | – | – | 100 | Ω |
| $Z_{OPB}$ | optical black clamp and blanking block output impedance | | – | – | 100 | Ω |
| $I_{PBIN}$ | input current pin 8 | | –2 | – | +2 | μA |
| $G_{AGCmin}$ | minimum gain of AGC circuit | AGC DAC input code = 00 (9-bit control) | – | 3.5 | – | dB |
| $G_{AGCmax}$ | maximum gain of AGC circuit | AGC DAC input code = ≥319 (9-bit control) | – | 33.5 | – | dB |
| $V_{inflex(p-p)}$ | voltage at soft clipper inflexion point (peak-to-peak value) | soft clipper 4-bit control DAC input code = 00 | – | 0.9 | – | V |
| | | soft clipper 4-bit control DAC input code = 15 | – | 2.5 | – | V |
| $CR_{sc}$ | soft clipper compression ratio | $V_{i(sc)} < V_{inflex}$ | – | 1.0 | – | |
| | | $V_{i(sc)} > V_{inflex}$ | – | 0.66 | – | |
| **Analog-to-digital converter; ADC** | | | | | | |
| $f_{CLK(max)}$ | maximum clock frequency | | 18 | – | – | MHz |
| $t_{CPH}$ | clock pulse width HIGH | | 15 | – | – | ns |
| $t_{CPL}$ | clock pulse width LOW | | 15 | – | – | ns |
| $SR_{CLK}$ | clock input slew rate (rising and falling edge) | 10% to 90% | 0.5 | – | – | V/ns |
| $V_{iADC(p-p)}$ | ADC input voltage level (peak-to-peak value) | | – | 1.8 | – | V |
| $V_{RB}$ | ADC reference voltage output code 0 | | – | 1.4 | – | V |
| $V_{RT}$ | ADC reference voltage output code 1023 | | – | 3.2 | – | V |
| $I_{ADCIN}$ | input current pin 10 | | –2 | – | +2 | μA |
| ILE | integral linearity error | $f_{CLK}$ = 18 Msps; ramp input | – | ±1.3 | ±2.0 | LSB |
| DLE | differential linearity error | $f_{CLK}$ = 18 Msps; ramp input | – | ±0.5 | ±0.9 | LSB |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Digital-to-analog converters** | | | | | | |
| OFD DAC | | | | | | |
| $V_{OFD(p-p)}$ | additional 8-bit control DAC (OFD) output voltage (peak-to-peak value) | | – | 1.0 | – | V |
| $V_{OFD(0)}$ | DC output voltage for code 0 | | – | 2.4 | – | V |
| $V_{OFD(255)}$ | DC output voltage for code 255 | | – | 3.4 | – | V |
| $Z_{OFD}$ | additional 8-bit control DAC (OFD) output impedance | | – | 2000 | – | Ω |
| ADC CLAMP CONTROL DAC (see Fig.5) | | | | | | |
| $V_{DACOUT(p-p)}$ | ADC clamp 10-bit control DAC output voltage (peak-to-peak value) | | – | 0.9 | – | V |
| $V_{DACOUT}$ | DC output voltage | code 0 | – | 1.4 | – | V |
| | | code 1023 | – | 2.3 | – | V |
| $Z_{DACOUT}$ | ADC clamp control DAC output impedance | | – | – | 250 | Ω |
| **Digital outputs ($f_{clk}$ = 18 MHz; $C_L$ = 20 pF)** | | | | | | |
| $V_{OH}$ | HIGH level output voltage | $I_o$ = –1 mA | $V_{DDO}$ – 0.5 | – | $V_{DDO}$ | V |
| $V_{OL}$ | LOW level output voltage | $I_o$ = 1 mA | 0 | – | 0.5 | V |
| $I_{OZ}$ | output current in 3-state mode | 0.5 V < $V_o$ < $V_{DDO}$ | –20 | | +20 | μA |
| $t_h$ | output hold time | | 5 | – | – | ns |
| $t_d$ | output delay | $V_{DDO}$ = 4.75 V | – | 12 | 15 | ns |
| | | $V_{DDO}$ = 3.15 V | – | 17 | 20 | ns |
| | | $V_{DDO}$ = 2.7 V | – | 21 | 24 | ns |
| **Serial interface** | | | | | | |
| $f_{SCLK}$ | maximum frequency of serial interface | | 5 | – | – | MHz |

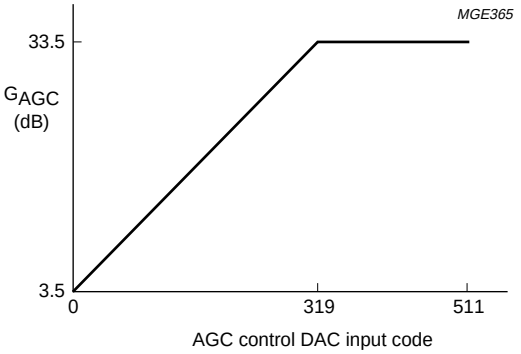
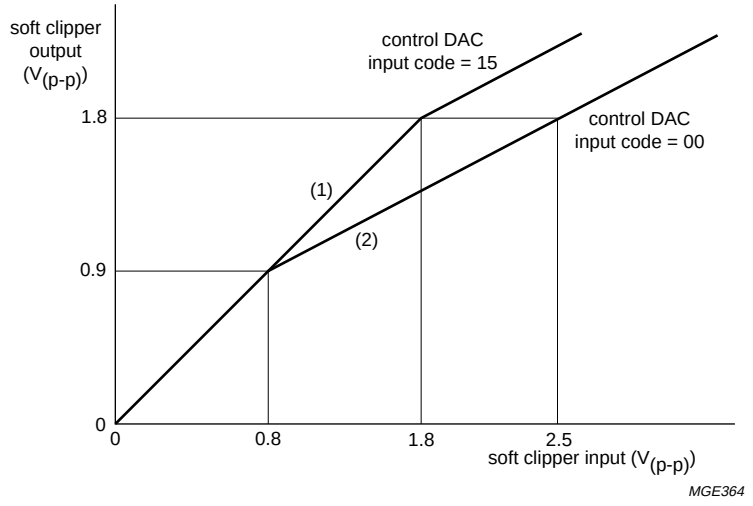



Fig.3 AGC gain as a function of DAC input code.




(1) $\frac{V_o}{V_i} = 1$

(2) $\frac{V_o}{V_i} = 0.66$

Fig.4 Soft clipper output voltage as a function of soft clipper input voltage.

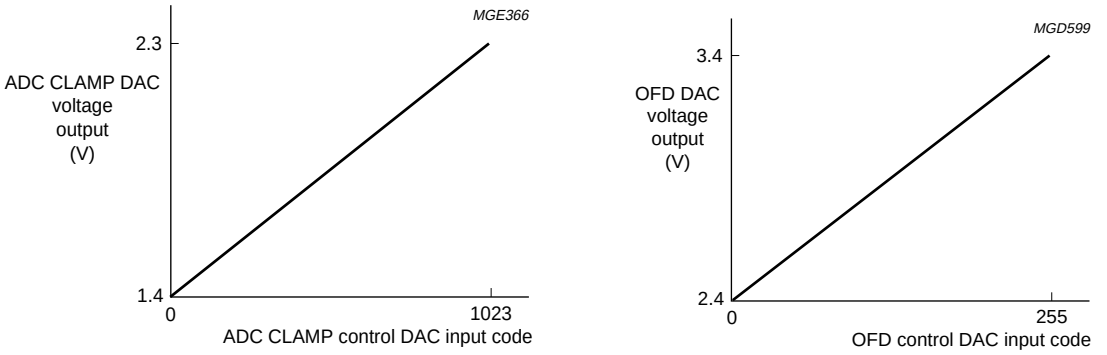



Fig.5 DAC voltage output as a function of DAC input code.

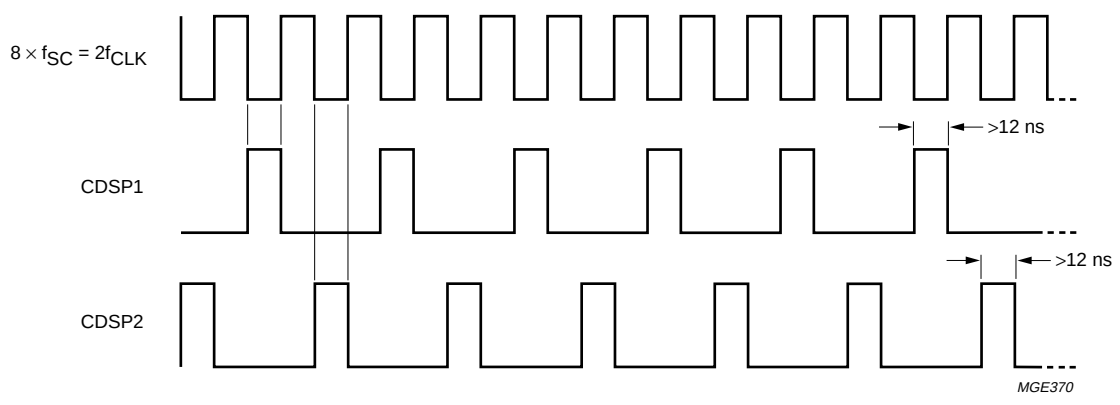



Fig.6 CCD high-band control signal timing (TDA8786).

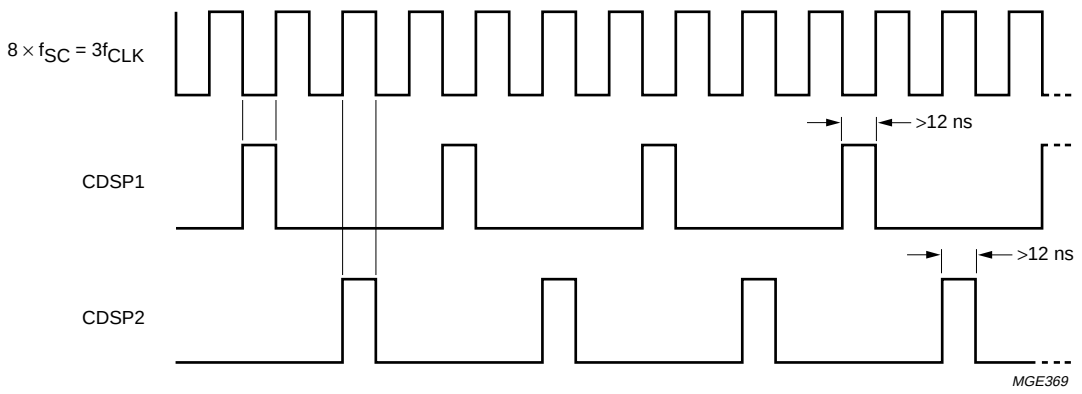



Fig.7 CCD normal-band control signal timing (TDA8786).

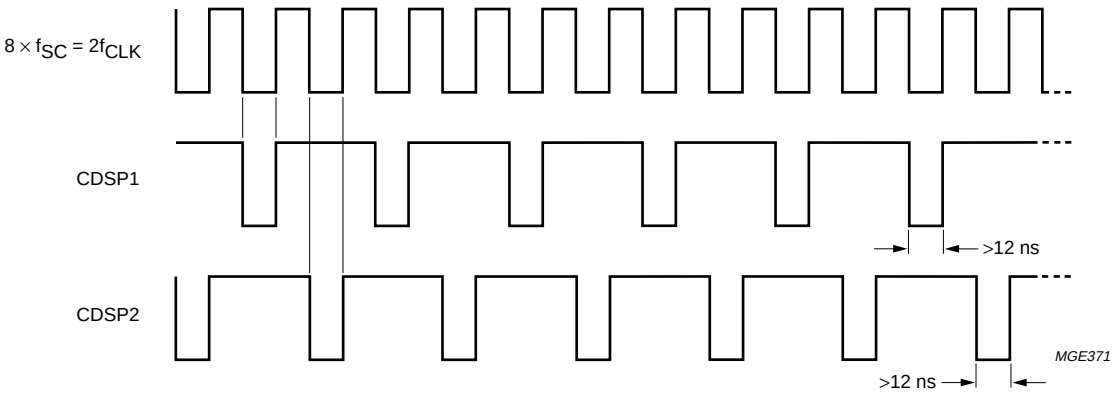



Fig.8 CCD high-band control signal timing (TDA8786A).

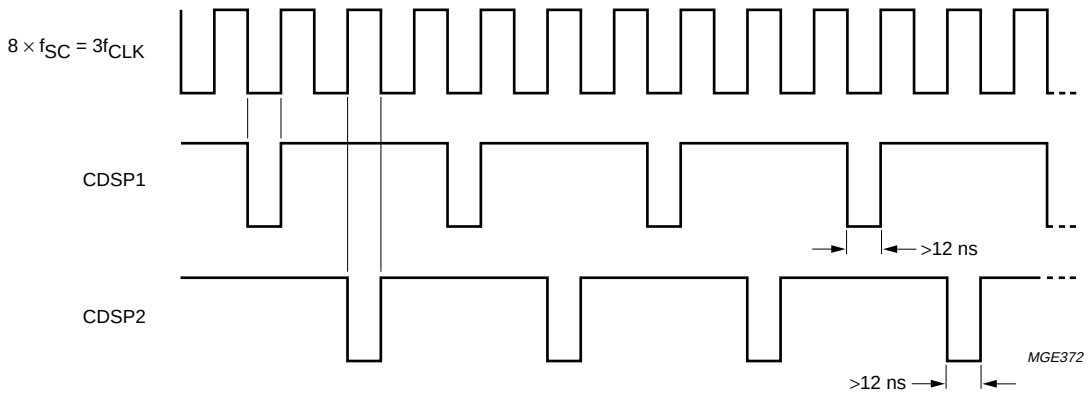



Fig.9 CCD normal-band control signal timing (TDA8786A).

**ADC clamping**

When CLPADC is HIGH (TDA8786); (LOW for TDA8786A) the ADC input is clamped to voltage level $V_{ref}$. $V_{ref}$ should normally be connected to $V_{RB}$ (ADC output code 0 pin) or to DACOUT (10-bit DAC output). The DAC is controlled via the serial interface, its output covers the lower half of the ADC input range.

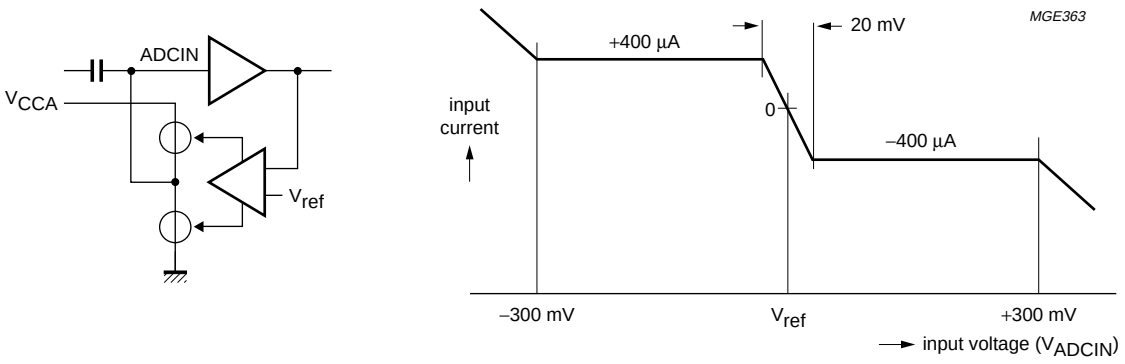



Fig.10 Clamping circuit and current waveform.

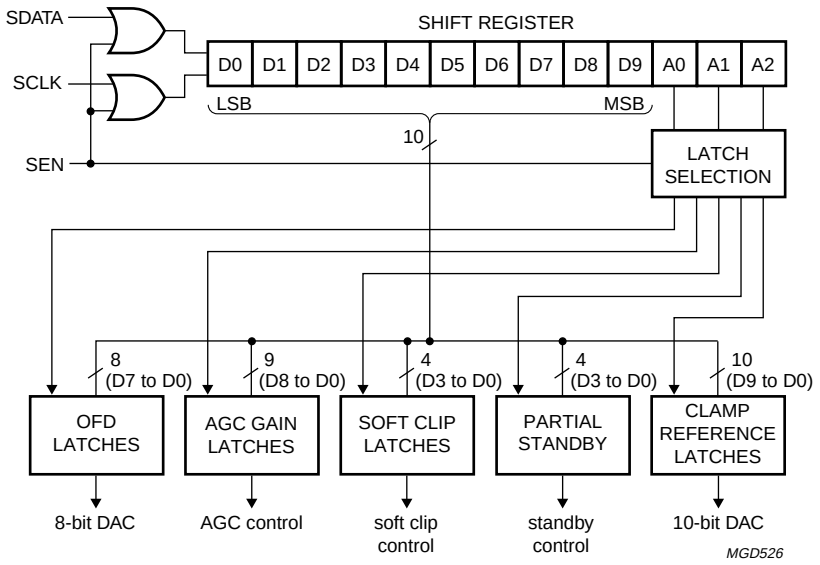
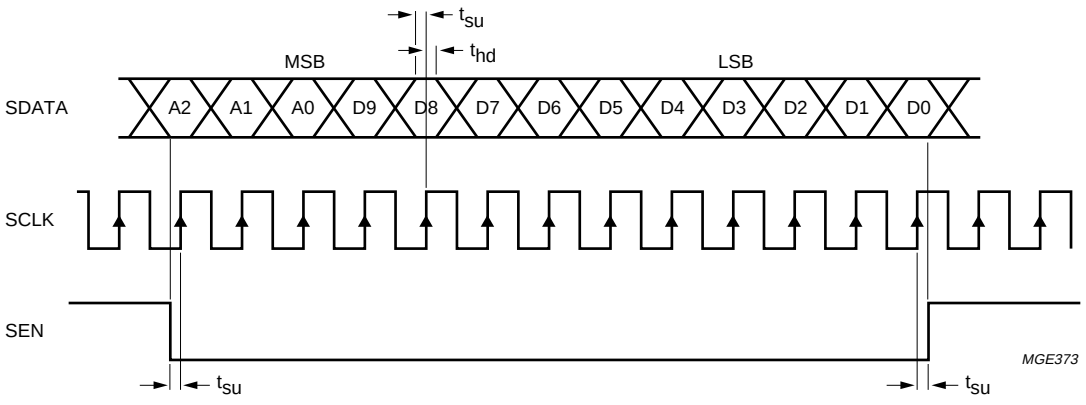



Fig.11 Serial interface block diagram.




$t_{su}$ = 4 ns (min.); $t_{hd}$ = 4 ns (min.).

Fig.12 Loading sequence of control DACs input data via the serial interface.

**Table 1** Serial interface programming

| ADDRESS BITS | | | DATA BITS D9 to D0 |
|---|---|---|---|
| **A2** | **A1** | **A0** | |
| 0 | 0 | 0 | OFD output control (D7 to D0). |
| 0 | 0 | 1 | Soft clipper control. Only the 4 LSBs (D3 to D0) are used. Bits D9 to D4 should be set to logic 0. |
| 0 | 1 | 0 | AGC gain control (D8 to D0). |
| 0 | 1 | 1 | Partial standby controls for power consumption optimization. Only the 4 LSBs (D3 to D0) are used. Bits D9 to D4 should be set to logic 0:<br>D0 = 1: CDS + AGC + soft clipper block in standby; $I_{CCA} + I_{CCD}$ = 38 mA<br>D1 = 1: optical black clamp + blanking block in standby; $I_{CCA} + I_{CCD}$ = 75 mA<br>D2 = 1: OFD DAC in standby; $I_{CCA} + I_{CCD}$ = 80.5 mA<br>D3 = 1: 6 dB amplifier (output on AMPOUT pin) in standby; $I_{CCA} + I_{CCD}$ = 81 mA. |
| 1 | 0 | 0 | Clamp reference DAC (D9 to D0). |

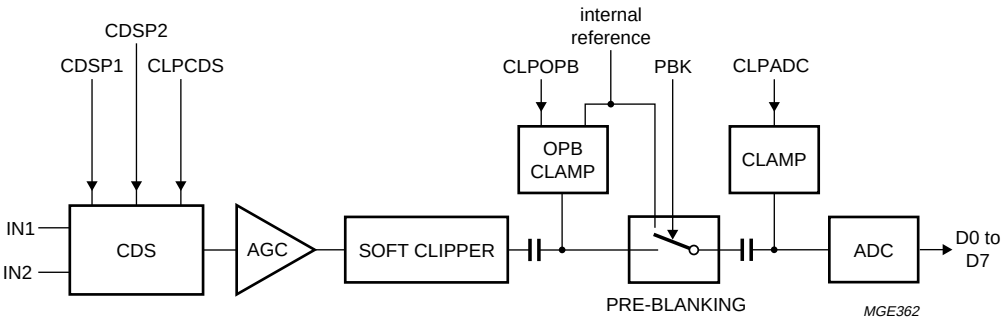
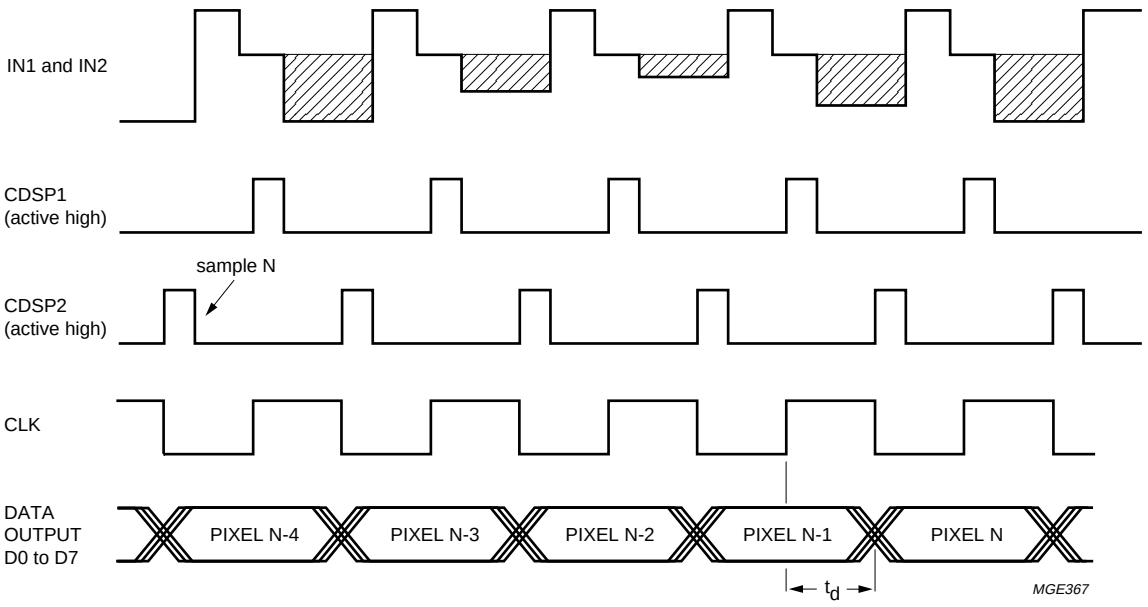



Fig.13 CDS, CLAMP and pre-blanking signal path for Figs 14. and 15




The hatched areas represent active video.

Fig.14 Pixel frequency timing diagram.

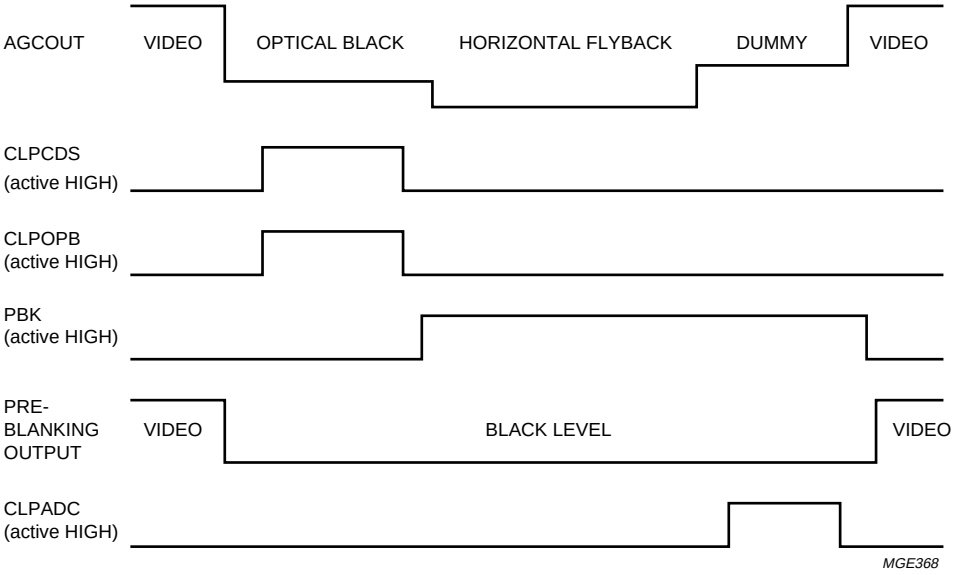
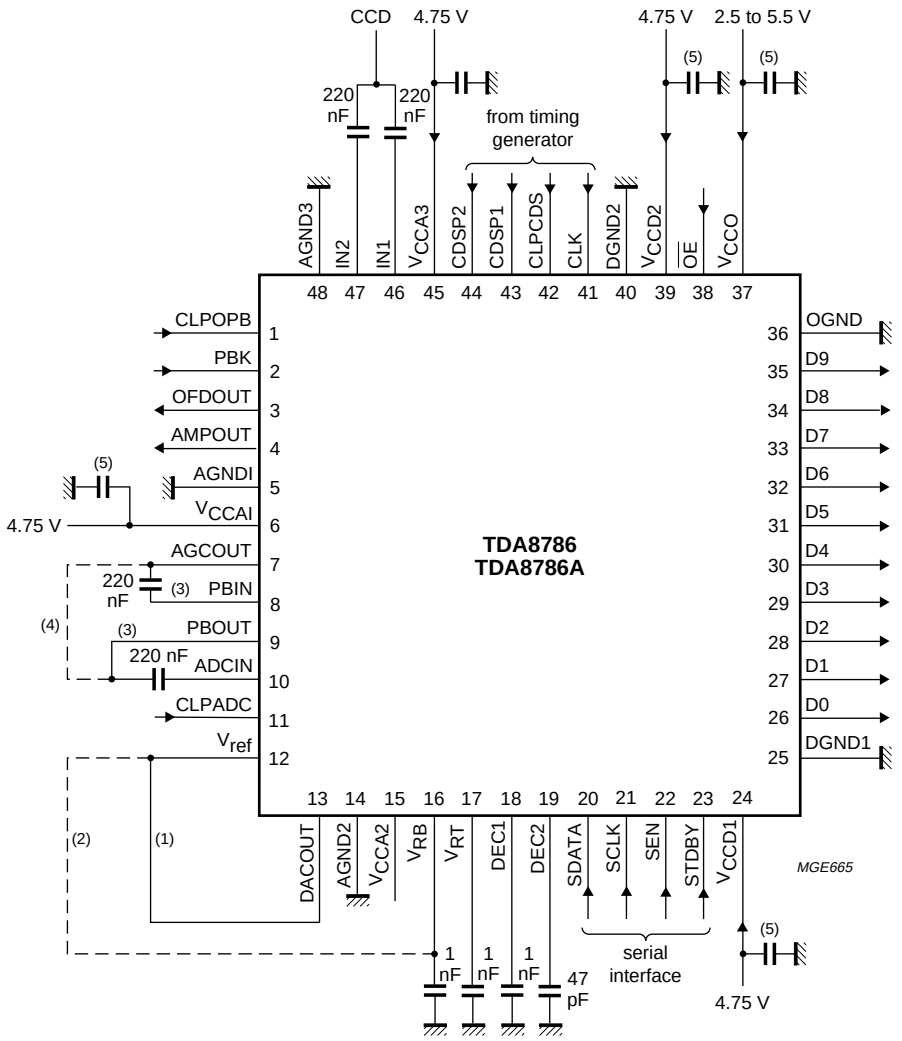



Fig.15 Line frequency timing diagram.

## APPLICATION INFORMATION




Depending on application [(1) or (2) and (3) or (4)] the following connections must be made;

(1) The clamp level of the signal input at ADCIN can be tuned from code 00 to code 511 in 0.5LSB step of ADC via the serial interface.

(2) The clamp level of the signal input at ADCIN is at code 00 of the ADC.

(3) The optical black clamp and preblanking blocks are used.

(4) The optical black clamp and preblanking blocks are not used.

(5) All supply pins must be decoupled with 100 nF capacitors as close as possible to the device.

Fig.16 Application diagram.

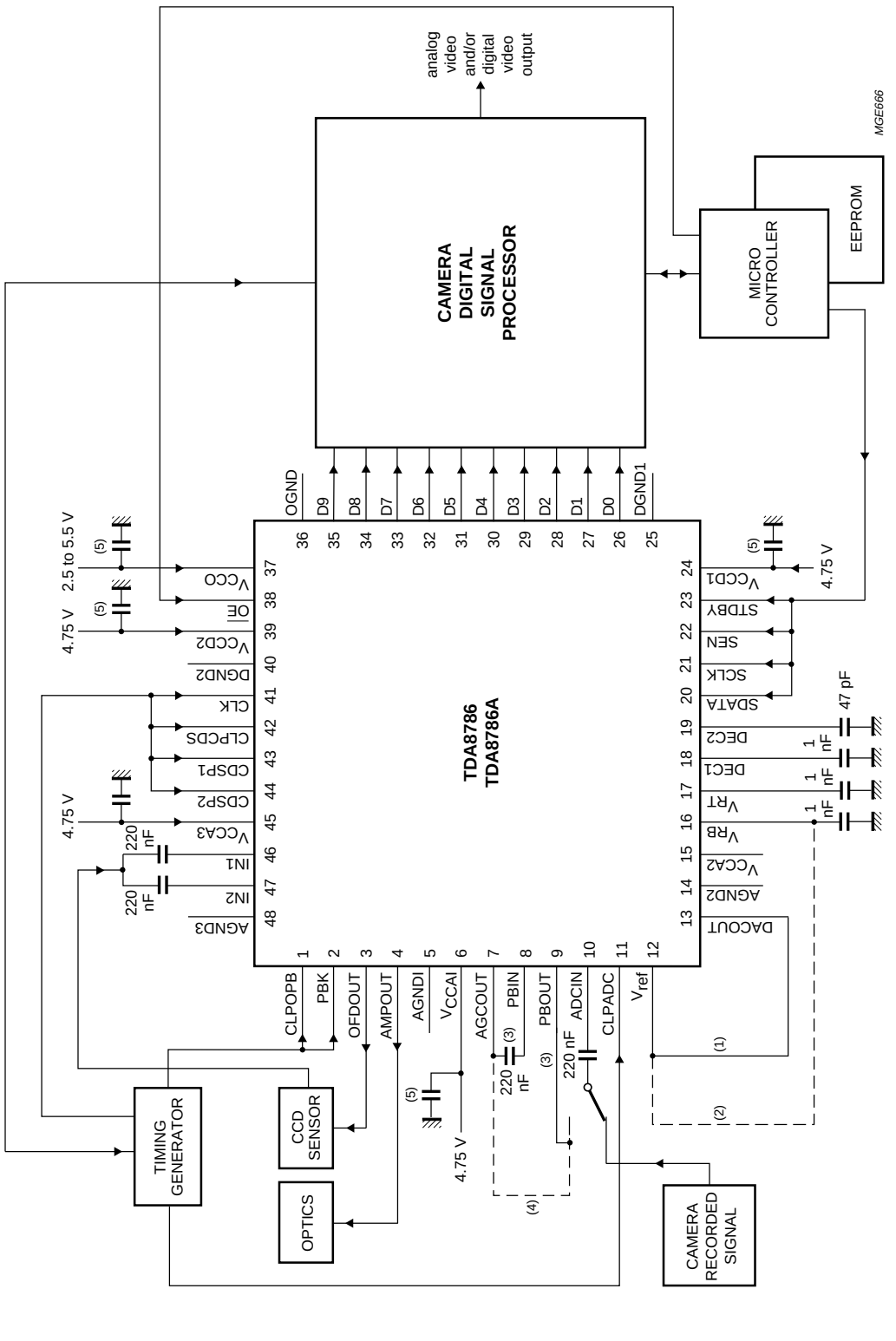
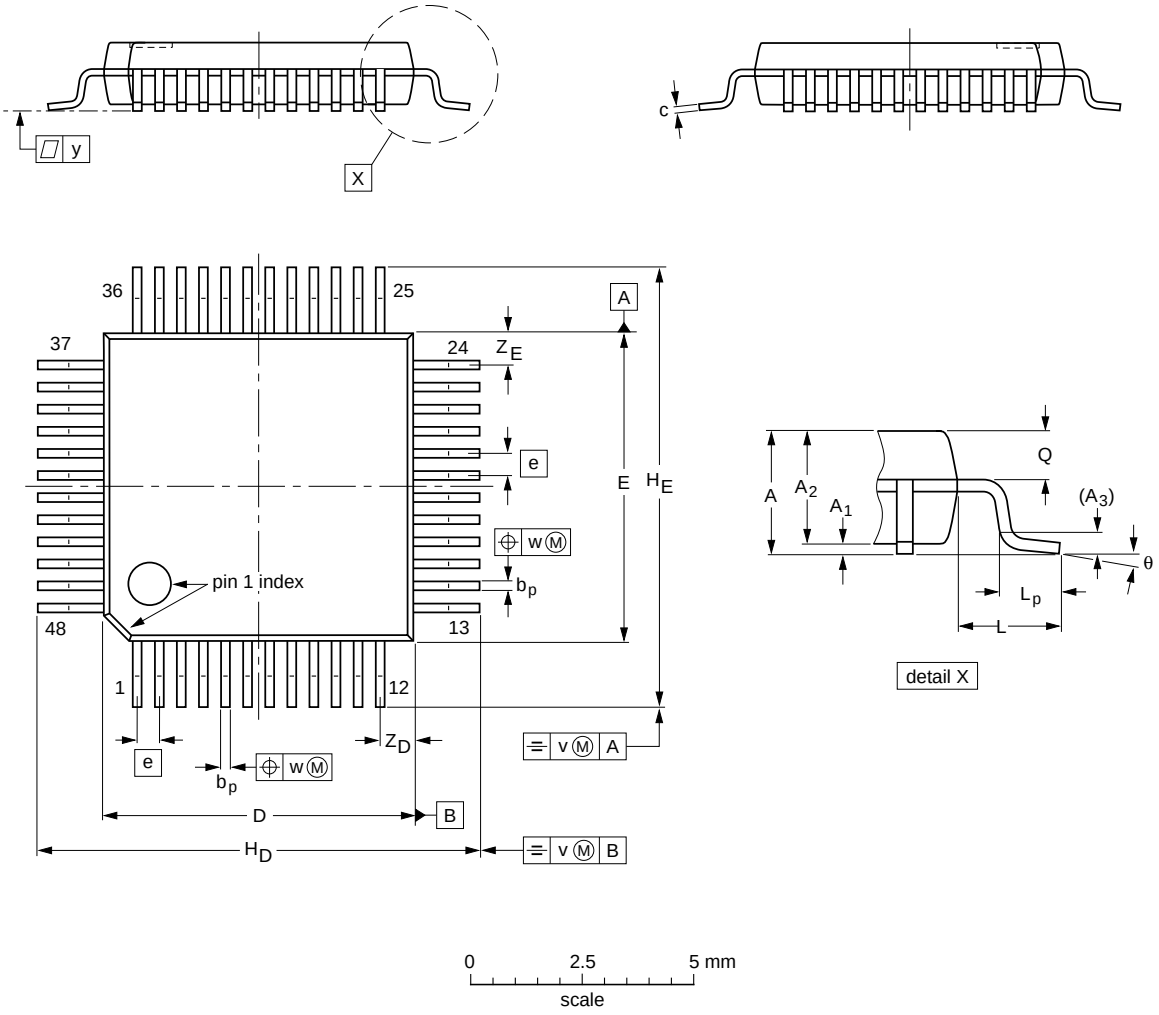



Fig.17 Application diagram.

See notes given in Fig.16

## PACKAGE OUTLINE

**LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm** **SOT313-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | Q | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.60 | 0.20<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 7.1<br>6.9 | 7.1<br>6.9 | 0.5 | 9.15<br>8.85 | 9.15<br>8.85 | 1.0 | 0.75<br>0.45 | 0.69<br>0.59 | 0.2 | 0.12 | 0.1 | 0.95<br>0.55 | 0.95<br>0.55 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT313-2 | | | | | | ~~93-06-15~~<br>94-12-19 |

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

### Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

### Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

**If wave soldering cannot be avoided, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

**Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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