DATA SHEET

TDA8712; TDF8712
8-bit digital-to-analog converters

Product specification
Supersedes data of April 1993
File under Integrated Circuits, IC02

June 1994

Philips Semiconductors

PHILIPS

8-bit digital-to-analog converters TDA8712; TDF8712

FEATURES

- 8-bit resolution
- Conversion rate up to 50 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required
- Temperature range
  - TDA8712: 0 to 70 °C
  - TDF8712: –40 to +85 °C.

APPLICATIONS

- High-speed digital-to-analog conversion
- Digital TV including:
  - field progressive scan
  - line progressive scan
- Subscriber TV decoders
- Satellite TV decoders
- Digital VCRs
- Industrial and automotive.

GENERAL DESCRIPTION

The TDA8712 and TDF8712 are 8-bit digital-to-analog converters (DACs) for video and other applications. They convert the digital input signal into an analog voltage output at a maximum conversion rate of 50 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8712	16	DIP	plastic	SOT38-1
TDF8712	16	DIP	plastic	SOT38-1
TDA8712T	16	SO16L	plastic	SOT162-1
TDF8712T	16	SO16L	plastic	SOT162-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage					
	TDA8712		4.5	5.0	5.5	V
	TDF8712		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage					
	TDA8712		4.5	5.0	5.5	V
	TDF8712		4.75	5.0	5.25	V
I_{CCA}	analog supply current	note 1	20	26	32	mA
I_{CCD}	digital supply current	note 1	16	23	30	mA
$\Delta V_{OUT(p-p)}$	full-scale analog output voltage differences between V_{OUT} and $\overline{V}_{OUT}$ (peak-to-peak value)	Z_L = 10 kΩ; note 2	–1.45	–1.60	–1.75	V
		Z_L = 75 Ω; note 2	–0.72	0.80	–0.88	V
ILE	DC integral linear error		–	±0.3	±0.5	LSB
DLE	DC differential linearity error		–	±0.3	±0.5	LSB
$f_{clk(max)}$	maximum conversion rate		50	–	–	MHz
B	–3 dB analog bandwidth	f_{clk} = 50 MHz; note 3	–	150	–	MHz
P_{tot}	total power dissipation					
	TDA8712		160	250	340	mW
	TDF8712		170	250	325	mW

Notes

1. D0 to D7 are connected to V_{CCD} and CLK is connected to DGND.
2. The analog output voltages (V_{OUT} and $\overline{V}_{OUT}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

BLOCK DIAGRAM

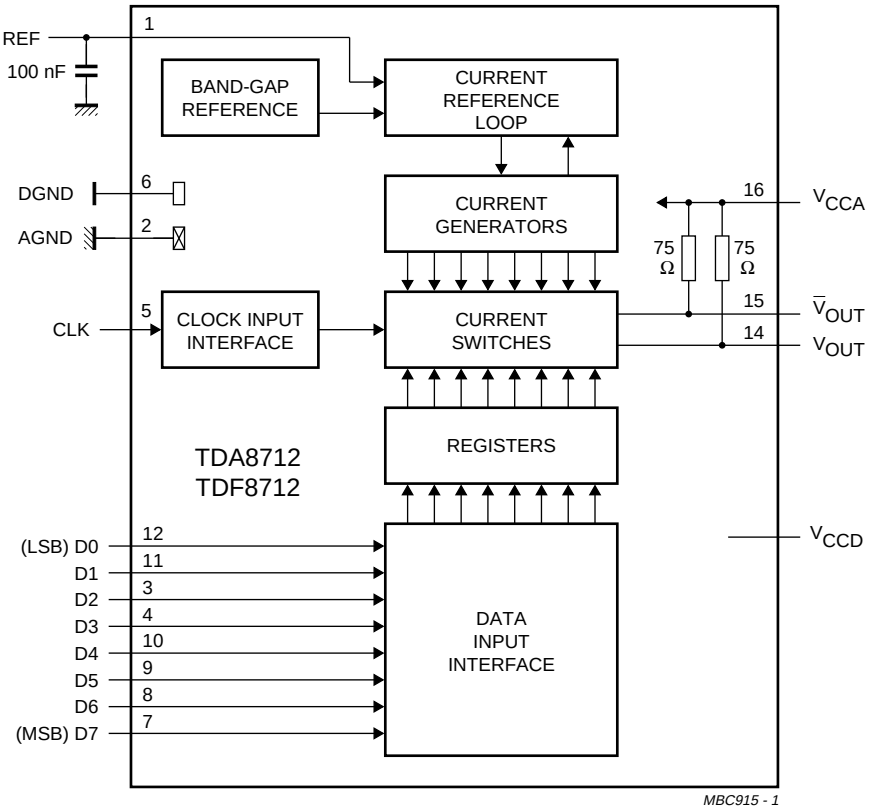


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input; bit 2
D3	4	data input; bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input; bit 7 (MSB)
D6	8	data input; bit 6
D5	9	data input; bit 5
D4	10	data input; bit 4
D1	11	data input; bit 1
D0	12	data input; bit 0 (LSB)
V_{CCD}	13	digital supply voltage (+5 V)
V_{OUT}	14	analog output voltage
$\overline{V}_{OUT}$	15	complimentary analog output voltage
V_{CCA}	16	analog supply voltage (+5 V)

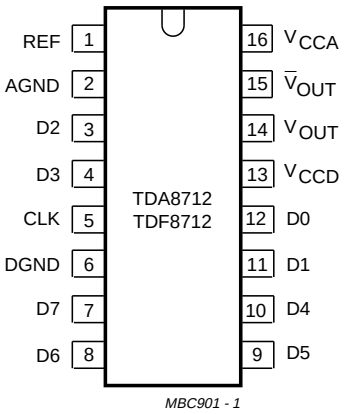


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	–0.3	+7.0	V
V_{CCD}	digital supply voltage	–0.3	+7.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCD}	–0.5	+0.5	V
ΔV_{GND}	ground voltage differences between V_{AGND} and V_{DGND}	–0.1	+0.1	V
V_I	input voltage (pins 3 to 5 and 7 to 12)	–0.3	V_{CCD}	V
I_{tot}	total output current (I_{OUT} + $\bar{I}_{OUT}$; pins 14 and 15)	–5	+26	mA
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature			
	TDA8712	0	+70	°C
	TDF8712	–40	+85	°C
T_j	junction temperature	–	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT38-1	70	K/W
	SOT162-1	90	K/W

CHARACTERISTICS

V_{CCA} = V_{16} to V_2 = 4.5 to 5.5 V (TDA8712) = 4.75 to 5.25 V (TDF8712); V_{CCD} = V_{13} to V_6 = 4.5 to 5.5 V (TDA8712) = 4.75 to 5.25 V (TDF8712); V_{CCA} to V_{CCD} = −0.5 to +0.5 V (TDA8712) = −0.25 to +0.25 V (TDF8712); REF decoupled to AGND via a 100 nF capacitor; T_{amb} = −40 to +85 °C; AGND and DGND shorted together; typical readings taken at V_{CCA} = V_{CCD} = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage					
	TDA8712		4.5	5.0	5.5	V
	TDF8712		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage					
	TDA8712		4.5	5.0	5.5	V
	TDF8712		4.75	5.0	5.25	V
I_{CCA}	analog supply current	note 1	20	26	32	mA
I_{CCD}	digital supply current	note 1	16	23	30	mA
ΔV_{GND}	ground voltage differences between V_{AGND} and V_{DGND}		−0.1	–	+0.1	V
Inputs						
DIGITAL INPUTS (D7 TO D0) AND CLOCK INPUT CLK						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	–	−0.3	−0.4	mA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	0.01	20	μA
$f_{clk(max)}$	maximum clock frequency		50	–	–	MHz
Outputs (referenced to V_{CCA})						
$\Delta V_{OUT(p-p)}$	full-scale analog output voltage differences between V_{OUT} and $\overline{V}_{OUT}$ (peak-to-peak value)	Z_L = 10 kΩ; note 2	−1.45	−1.60	−1.75	V
		Z_L = 75 Ω; note 2	−0.72	0.80	−0.88	V
V_{os}	analog offset output voltage	code = 0	–	−3	−25	mV
TC_{VOUT}	full-scale analog output voltage temperature coefficient		–	–	200	μV/K
TC_{Vos}	analog offset output voltage temperature coefficient		–	–	20	μV/K
B	−3 dB analog bandwidth	f_{clk} = 50 MHz; note 3	–	150	–	MHz
G_{diff}	differential gain		–	0.6	–	%
φ_{diff}	differential phase		–	1	–	deg
Z_o	output impedance		–	75	–	Ω
Transfer function (f_{clk} = 50 MHz)						
ILE	DC integral linear error		–	±0.3	±0.5	LSB
DLE	DC differential linearity error		–	±0.3	±0.5	LSB

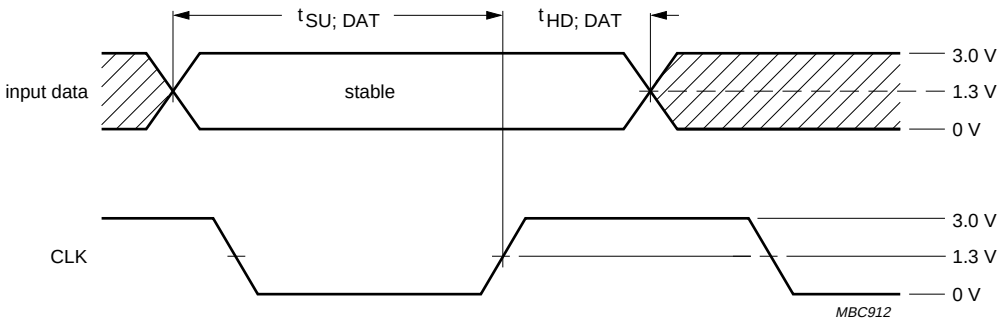
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics (f_{clk} = 50 MHz; notes 4 and 5; see Figs 3, 4 and 5)						
$t_{SU;DAT}$	data set-up time		–0.3	–	–	ns
$t_{HD;DAT}$	data hold time		2.0	–	–	ns
t_{PD}	propagation delay time		–	–	1.0	ns
t_{S1}	settling time 1	10% to 90% full-scale change to ±1 LSB	–	1.1	1.5	ns
t_{S2}	settling time 2	10% to 90% full-scale change to ±1 LSB	–	6.5	8.0	ns
t_d	input to 50% output delay time		–	3.0	5.0	ns
Output transients (glitches; f_{clk} = 50 MHz; note 6; see Fig.6)						
E_g	glitch energy from code	transition 127 to 128	–	–	30	LSB·ns

Notes

1. D0 to D7 are connected to V_{CCD} and CLK is connected to DGND.
2. The analog output voltages (V_{OUT} and $\overline{V}_{OUT}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).
4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $\overline{V}_{OUT}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data is latched at the rising edge of the clock. The output voltage remains stable (independent of input data variations) during the HIGH level of the clock (CLK = HIGH). During a LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages; see Fig.5.
5. The data set-up time ($t_{SU;DAT}$) is the minimum period preceding the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising edge of the clock and still be recognized. The data hold time ($t_{HD;DAT}$) is the minimum period following the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising edge of the clock and still be recognized.
6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 and 128 and on the falling edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of the offset voltage).

CODE	INPUT DATA (D7 to D0)	DAC OUTPUT VOLTAGES (V)			
		Z_L = 10 kΩ		Z_L = 75 Ω	
		V_{OUT}	$\overline{V}_{OUT}$	V_{OUT}	$\overline{V}_{OUT}$
0	000 00 00	0	–1.6	0	–0.8
1	000 000 01	–0.006	–1.594	–0.003	–0.797
.	.	.	.	.	.
128	100 000 00	–0.8	–0.8	–0.4	–0.4
.	.	.	.	.	.
254	111 111 10	–1.594	–0.006	–0.797	–0.003
255	111 111 11	–1.6	0	–0.8	0



The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns after the first rising edge of the clock ($t_{SU;DAT}$ is negative; –0.3 ns). Data must be held at least 2 ns after the rising edge ($t_{HD;DAT}$ = +2 ns).

Fig.3 Data set-up and hold times.

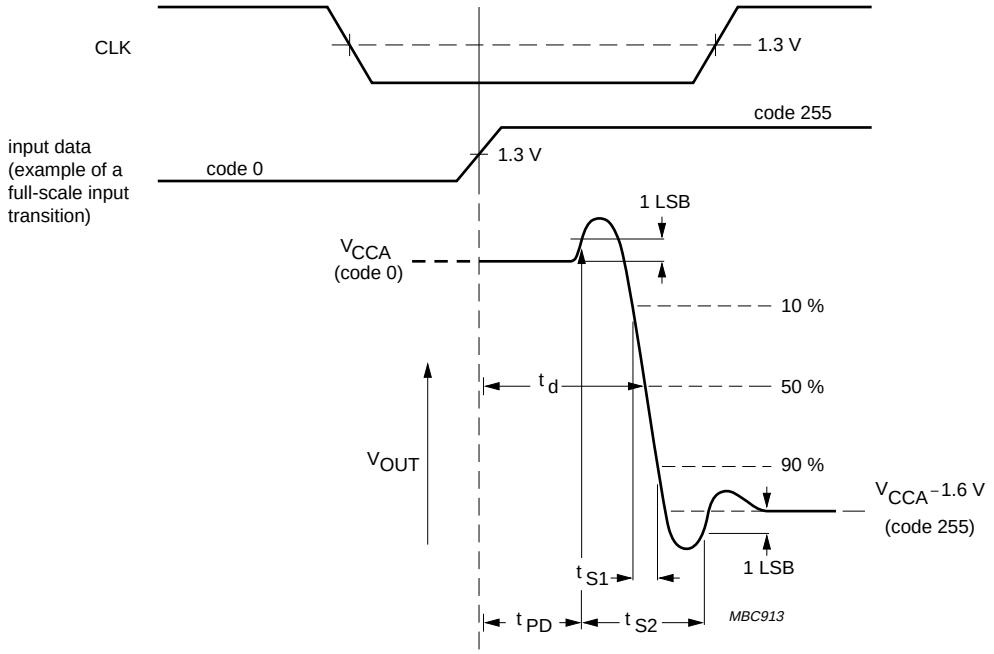
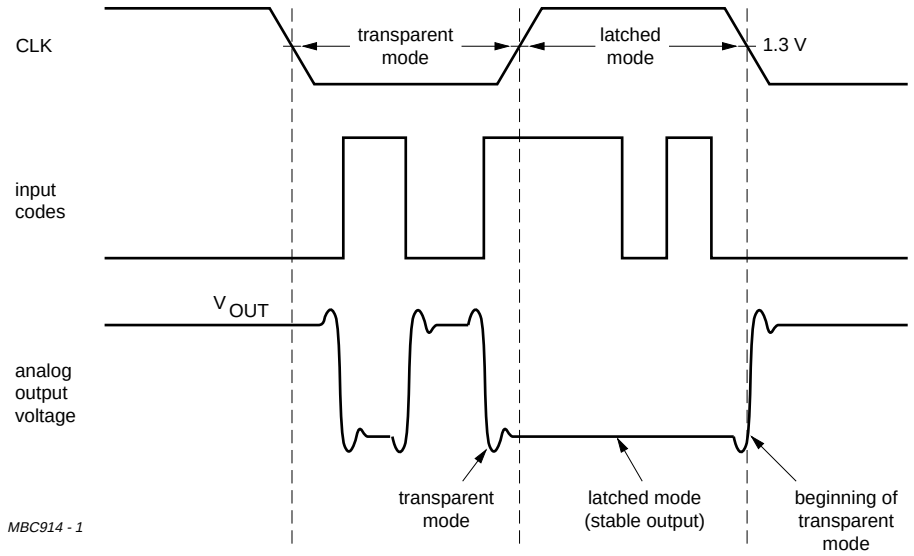
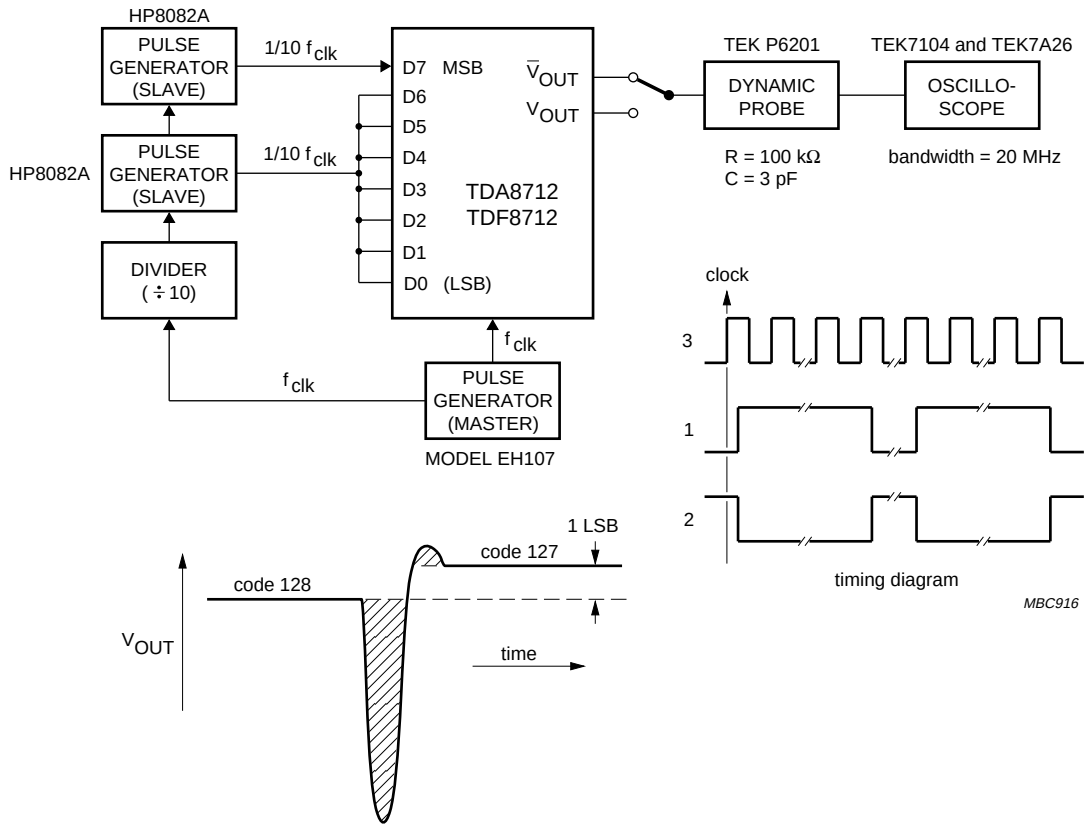


Fig.4 Switching characteristics.



During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable regardless of any change at the input. A change of input data during the latched mode will be seen on the falling edge of the clock (beginning of the transparent mode).

Fig.5 Latched and transparent mode.



The value of the glitch energy is the sum of the shaded area measured in LSB·ns.

Fig.6 Glitch energy measurement.

INTERNAL PIN CONFIGURATIONS

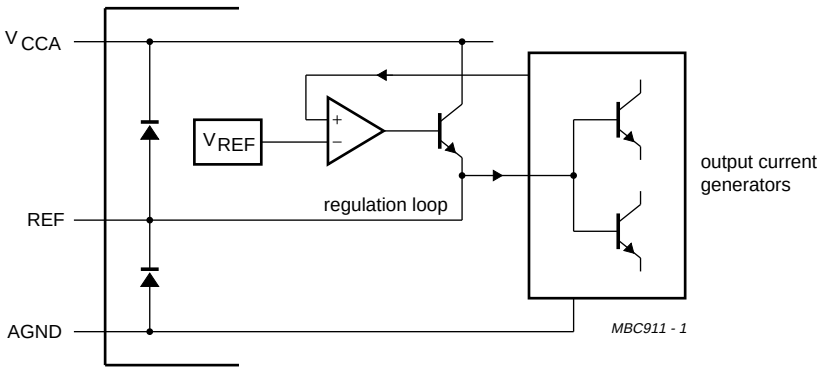


Fig.7 Reference voltage generator decoupling.

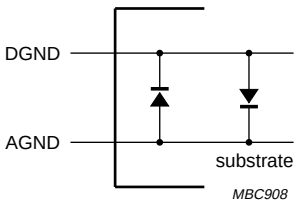


Fig.8 AGND and DGND.

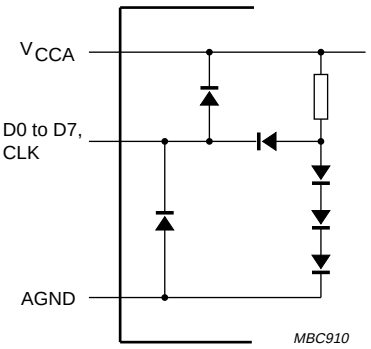


Fig.9 D7 to D0 and CLK.

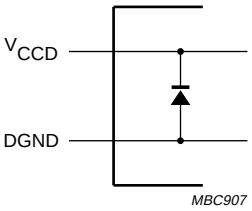


Fig.10 Digital supply.

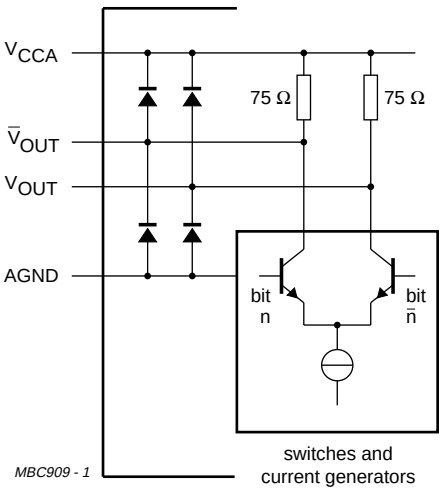


Fig.11 Analog outputs.

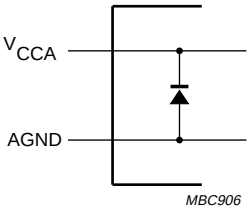
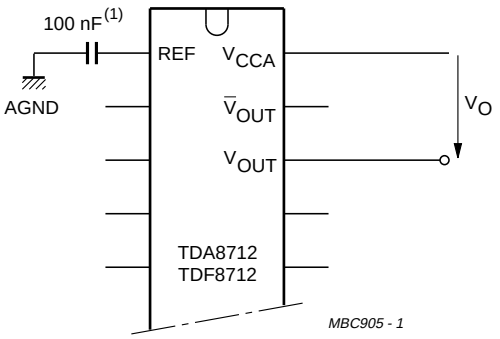


Fig.12 Analog supply.

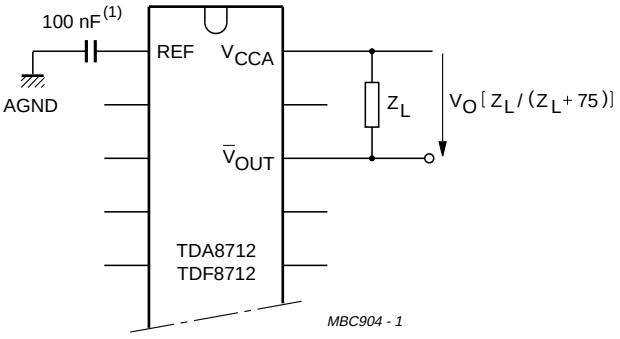
APPLICATION INFORMATION

Additional application information can be supplied on request (please quote *"FTV/8901").*



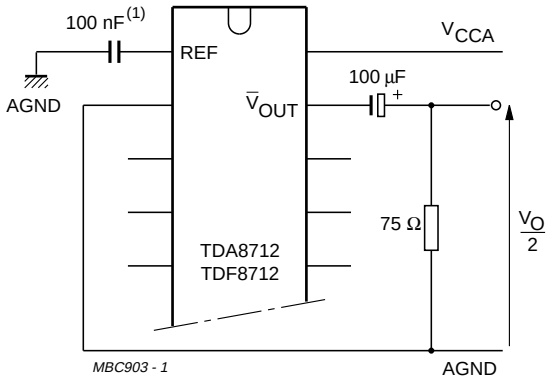
(1) This is a recommended value for decoupling pin 1.
$V_O = -\overline{V}_{OUT}$; see Table 1; Z_L = 10 kΩ.

Fig.13 Analog output voltage without external load.



(1) This is a recommended value for decoupling pin 1.
External load Z_L = 75 Ω to ∞.

Fig.14 Analog output voltage with external load.



(1) This is a recommended value for decoupling pin 1.

Fig.15 Analog output voltage with AGND as reference.

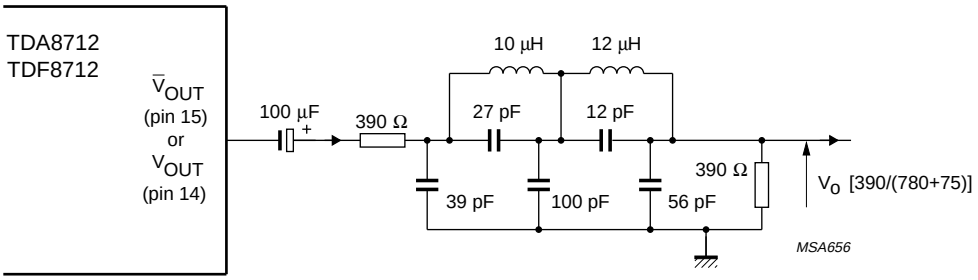


Fig.16 Example of anti-aliasing filter (analog output referenced to AGND).

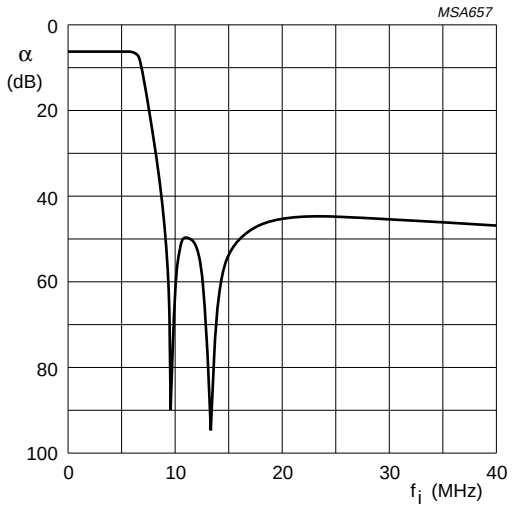
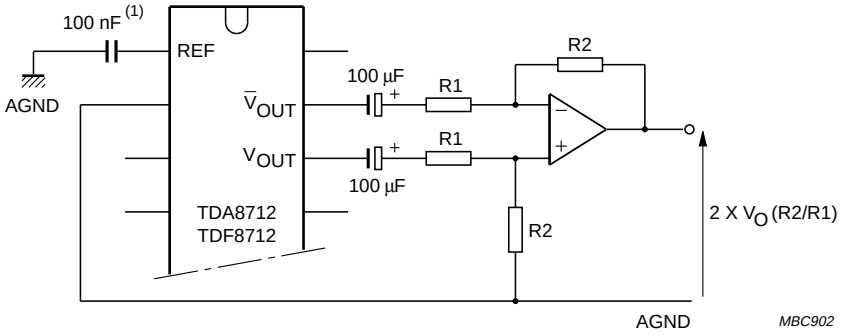


Fig.17 Frequency response for filter shown in Fig.16.

Characteristics of Fig. 17

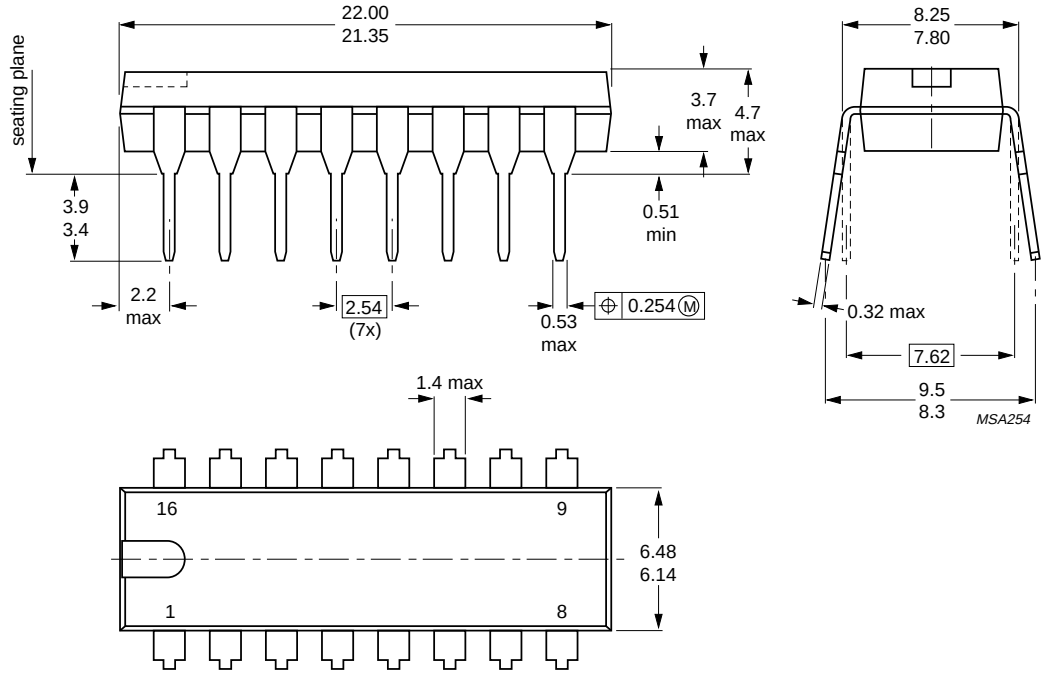
- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.1$ dB
- f = 6.7 MHz at −3 dB
- f_{notch} = 9.7 MHz and 13.3 MHz.



(1) This is a recommended value for decoupling pin 1.

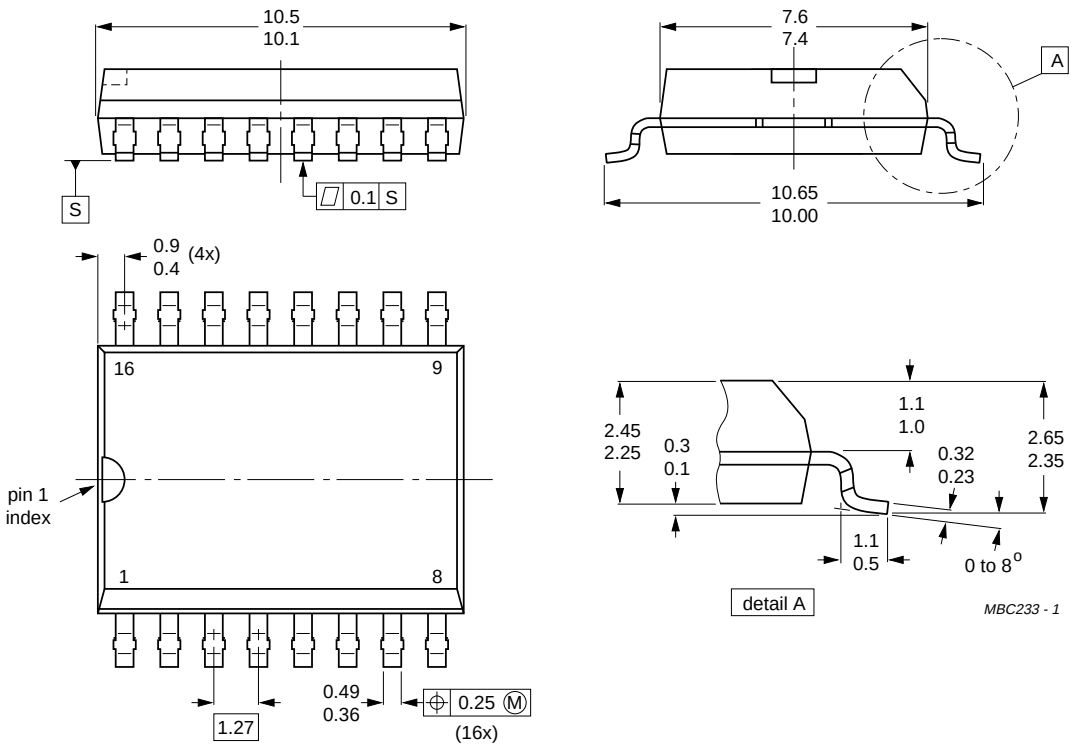
Fig.18 Differential mode (improved supply voltage ripple rejection).

PACKAGE OUTLINES



Dimensions in mm.

Fig.19 Plastic dual in-line package; 16 leads (300 mil) SOT38-1.



Dimensions in mm.

Fig.20 Plastic small outline package; 16 leads; large body (SOT162-1).

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic small-outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.