DATA SHEET

TDA8446
Fast RGB/YC switch for digital decoding

Product specification
Supersedes data of August 1992
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

Fast RGB/YC switch for digital decoding TDA8446

FEATURES

- R, G, B clamped inputs
- Luminance and chrominance difference matrix
- Y-clamped inputs
- Fast switching between internal and external Y
- Chrominance input
- Amplifier with selectable gain
- 3-state switch for chrominance output.

APPLICATIONS

- Digital TV systems
- Desktop video architecture.

DESCRIPTION

The TDA8446 is a video switch which has been designed for use in Digital Multistandard System Decoders (DMSD) in digital video system. The device is intended for matrixing incoming RGB signals and for switching between luminance signals. It generates a SYNC signal and TTL clamping pulses from any video signal with sync pulses.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	10.8	–	13.2	V
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8446	DIP20	plastic dual in-line package; 20 leads; (300 mil)	SOT146-1
TDA8446T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

BLOCK DIAGRAM

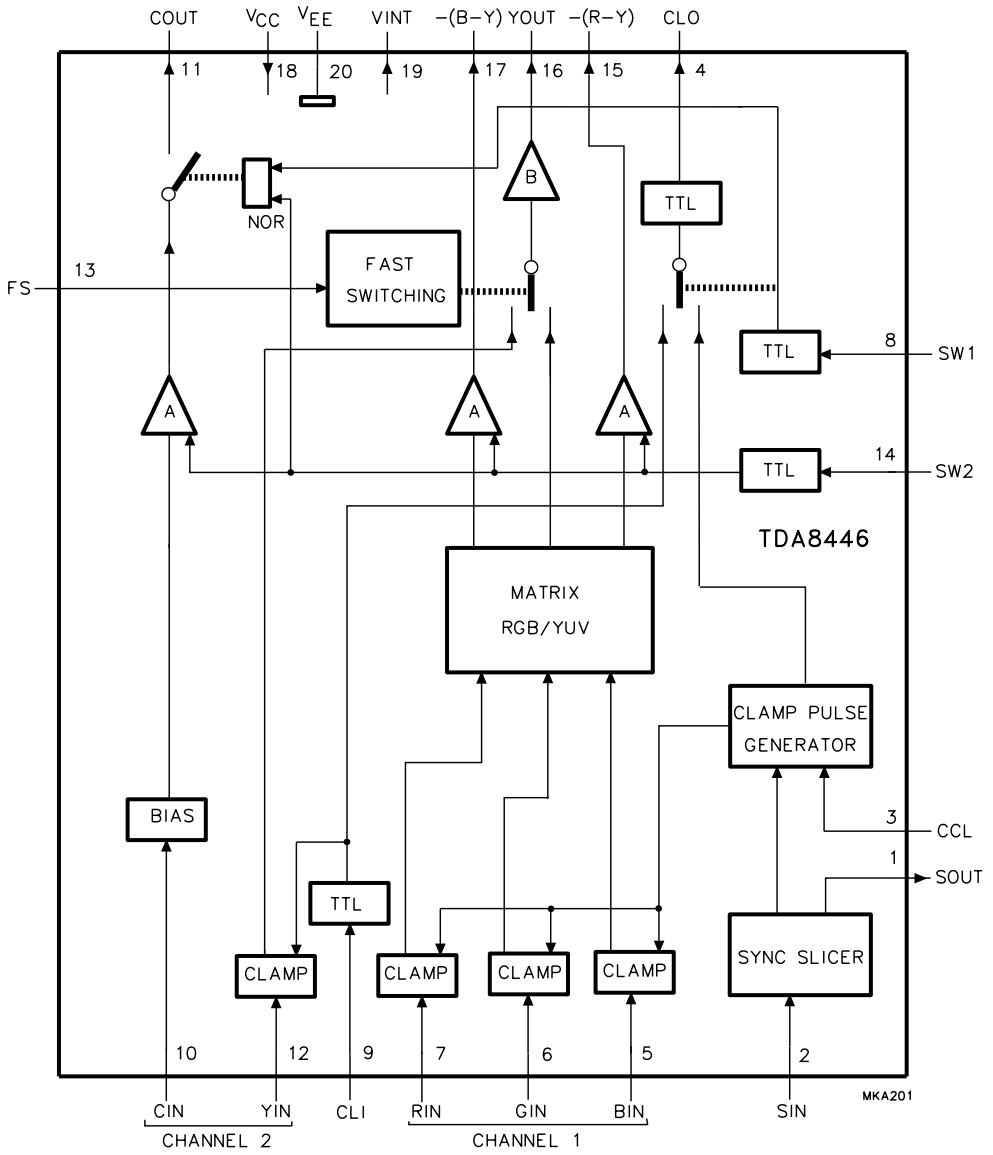


Fig.1 Block diagram (TDA8446).

PINNING

SYMBOL	PIN		DESCRIPTION
	DIP20	SO28	
SOUT	1	1	synchronization signal output; this output provides the synchronization information extracted from the incoming signal at pin 2 (SIN).
SIN	2	2	synchronization signal input; CSYNC or CVBS signal from the peri-connector
CCL	3	3	clamping capacitor connection; the clamping pulse is generated by external circuitry connected to this pin, the generated pulse clamps the RGB inputs.
n.c.	–	4	not connected
CLO	4	5	clamping pulse output
n.c.	–	6	not connected
BIN	5	7	B-signal input
GIN	6	8	G-signal input
RIN	7	9	R-signal input
SW1	8	10	clamping control signal input; this TTL signal is used to select the clamp signal, a LOW level at this input forces the circuit to output the generated clamping pulse.
n.c.	–	11	not connected
CLI	9	12	clamping pulse input; this TTL signal indicates the black level clamping period for the incoming Y signal (active-HIGH).
CIN	10	13	chrominance signal input
COUT	11	14	chrominance signal output
YIN	12	15	luminance signal input; this input also accepts the CVBS signal
FS	13	16	fast switching signal input; this signal is used to control fast switching of the luminance signals, a HIGH level at this input forces the circuit to output the internal Y signal.
n.c.	–	17	not connected
n.c.	–	18	not connected
SW2	14	19	gain control signal input; this TTL signal is used to set the gain of the chrominance amplifiers (A), a LOW level at this input forces the gain A to 6 dB (HIGH forces to 0 dB).
n.c.	–	20	not connected
–(R-Y)	15	21	–(R–Y) signal output
YOUT	16	22	luminance signal output
–(B–Y)	17	23	–(B–Y) signal output
n.c.	–	24	not connected
n.c.	–	25	not connected
V_{CC}	18	26	positive supply voltage (+12 V)
VINT	19	27	internal decoupling
V_{EE}	20	28	ground

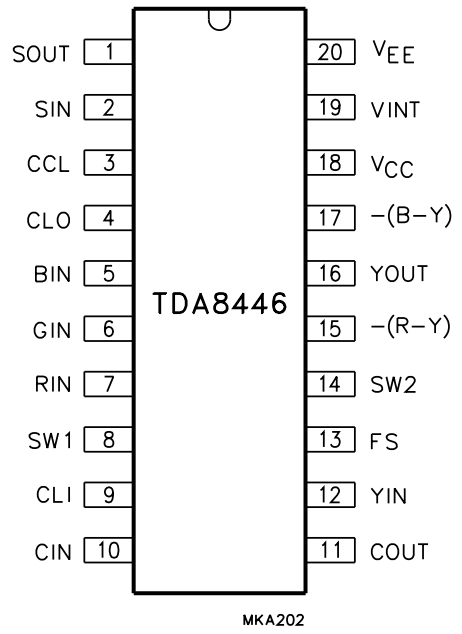


Fig.2 Pin configuration (DIP20).

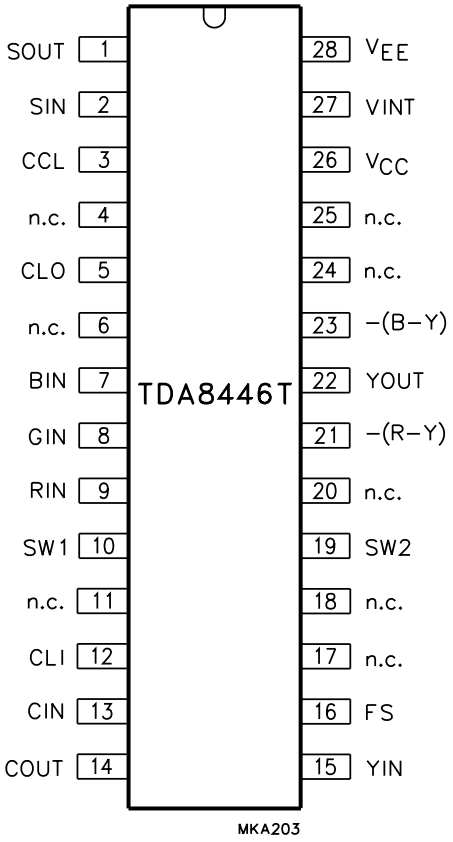


Fig.3 Pin configuration (SO28).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	+14	V
V_I	input voltage	–0.3	+12.3	V
T_{stg}	storage temperature	–55	+125	°C

HANDLING

Each pin will withstand the ESD test in accordance with MIL-STD-883C class 2 (2000 V to 2999 V). Method 3015 (Human body model: R = 1500 Ω; C = 100 pF) 3 pulses positive and 3 pulses negative on each pin as a function of ground. The IC will withstand 500 V in accordance with UZW-BO/FQ-B302 (Machine model: R = 0 Ω; C = 200 pF; L = 2.5 μH) 3 pulses positive and 3 pulses negative.

OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply/temperature					
V_{CC}	supply voltage	10.8	–	13.2	V
T_{amb}	operating ambient temperature	0	–	+70	°C
TTL inputs (SW1, SW2 and CLI)					
V_{IH}	HIGH level input voltage	2	–	V_{CC}	V
V_{IL}	LOW level input voltage	–0.3	–	+0.8	V
SYNC signal (SIN)					
$V_{S(p-p)}$	sync amplitude (peak-to-peak value)	0.2	–	2.5	V
Fast Switching input (FS)					
V_{IH}	HIGH level input voltage	1	–	3	V
V_{IL}	LOW level input voltage	0	–	0.4	V
Video inputs (RIN, GIN, BIN, CIN, YIN)					
$V_{i(p-p)}$	video amplitude on RIN, GIN and BIN inputs (peak-to-peak value)	–	0.7	1	V
C_I	input capacitance	–	100	–	nF
Clamping pulse generator (CCL)					
R_{clamp}	clamping resistance	–	4.7	–	kΩ
C_{clamp}	clamping capacitance	–	1	–	nF

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{CC}	supply current		–	–	75	mA
SVRR	supply voltage rejection ratio	note 1	30	–	–	dB
Y and R, G, B channels						
I_{CL}	input clamping current	V_{CC} = 6 V; V_I = 0 V	0.3	–	–	mA
I_I	input current	V_I = 9 V	–1.5	+0.5	+1.5	μA
G_A	gain of amplifier A	f_i = 1 MHz; V_{SW2} = 2 V	–1	0	+1	dB
		f_i = 1 MHz; V_{SW2} = 0.8 V	5	6	7	dB
G_B	gain of amplifier B	f_i = 1 MHz	–1	0	+1	dB
	RGB matrixed according to the following equations: Y = 0.30R + 0.59G + 0.11B R–Y = 0.70R – 0.59G – 0.11B B–Y = –0.30R – 0.59G + 0.89B					
ΔG_{diff}	relative gain difference	note 2	–	0	10	%
$\lvert\Delta G\rvert$	maximum gain variation	100 kHz < f_i < 8 MHz	–	3	–	dB
R_O	output resistance		–	15	–	Ω
Δt	time difference at output	f_i = 1 MHz; note 3	–	–	25	ns
V_O	DC output level	V_{CCL} = 6 V	–	4.2	–	V
t_{fsd}	fast switching delay	see Fig.4	–	20	–	ns
t_{fs}	fast switching time	see Fig.4	–	10	–	ns
I_{IFS}	input current on fast switching control (pin 13)	V_I = 0.4 V	–	0.7	–	μA
		V_I = 1 V	–	0.5	–	μA
Chrominance channel (CIN, COUT)						
R_i	internal input resistance		–	50	–	kΩ
V_O	DC output level	I_I = 0	–	5	–	V
G_A	gain of amplifier A	f_i = 1 MHz; V_{SW1} = V_{SW2} = 2 V	–1	0	+1	dB
		f_i = 1 MHz; V_{SW2} = 0.8 V	5	6	7	dB
$\lvert\Delta G\rvert$	maximum gain variation	100 kHz < f_i < 8 MHz	–	3	–	dB
α_{off}	isolation (off state)	f_i = 5 MHz; V_{SW1} = V_{SW2} = 0.8 V	–	60	–	dB
Z_o	output impedance	V_{SW1} = V_{SW2} = 0.8 V	100	–	–	kΩ
R_o	output resistance		–	7	–	Ω
TTL inputs (SW1, SW2, CLI)						
I_{IH}	HIGH level input current	V_{IH} = 2 V	–	–	10	μA
I_{IL}	LOW level input current	V_{IL} = 0.8 V	–	–	–600	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clamp output (CLO)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = 10 μA	2.4	–	–	V
Synchronization channel (SOUT)						
$V_{o(p-p)}$	output amplitude (peak-to-peak value)		0.2	–	1.5	V

Notes

1. Supply voltage rejection ratio = $20\log\frac{V_{R(CC)}}{V_{R(O)}}$
2. The relative gain difference is measured when only one input signal (R, G or B) is present.
3. The inputs RIN, GIN and BIN are interconnected; Δt is the maximum time coincidence error between the luminance and the chrominance signals.

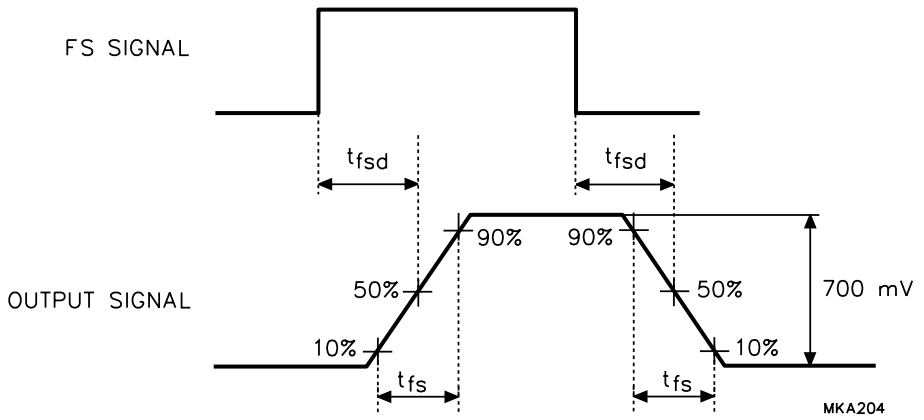


Fig.4 Fast switching times.

APPLICATION INFORMATION

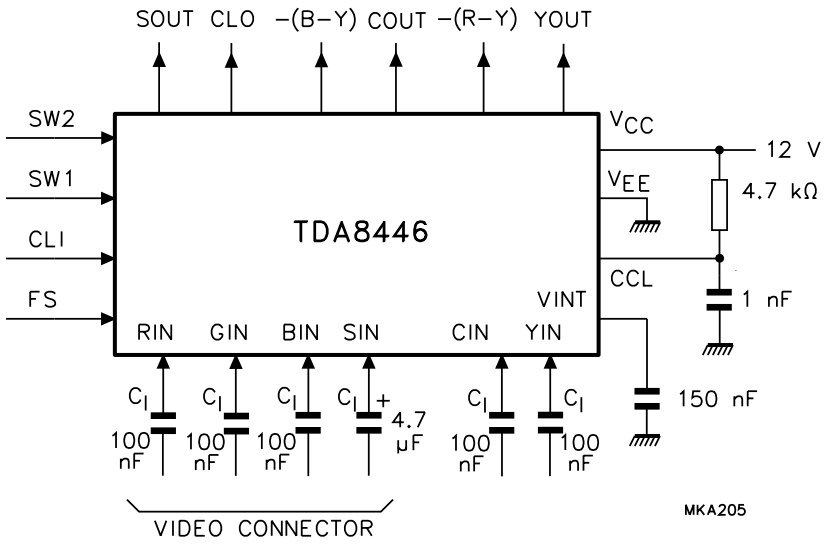
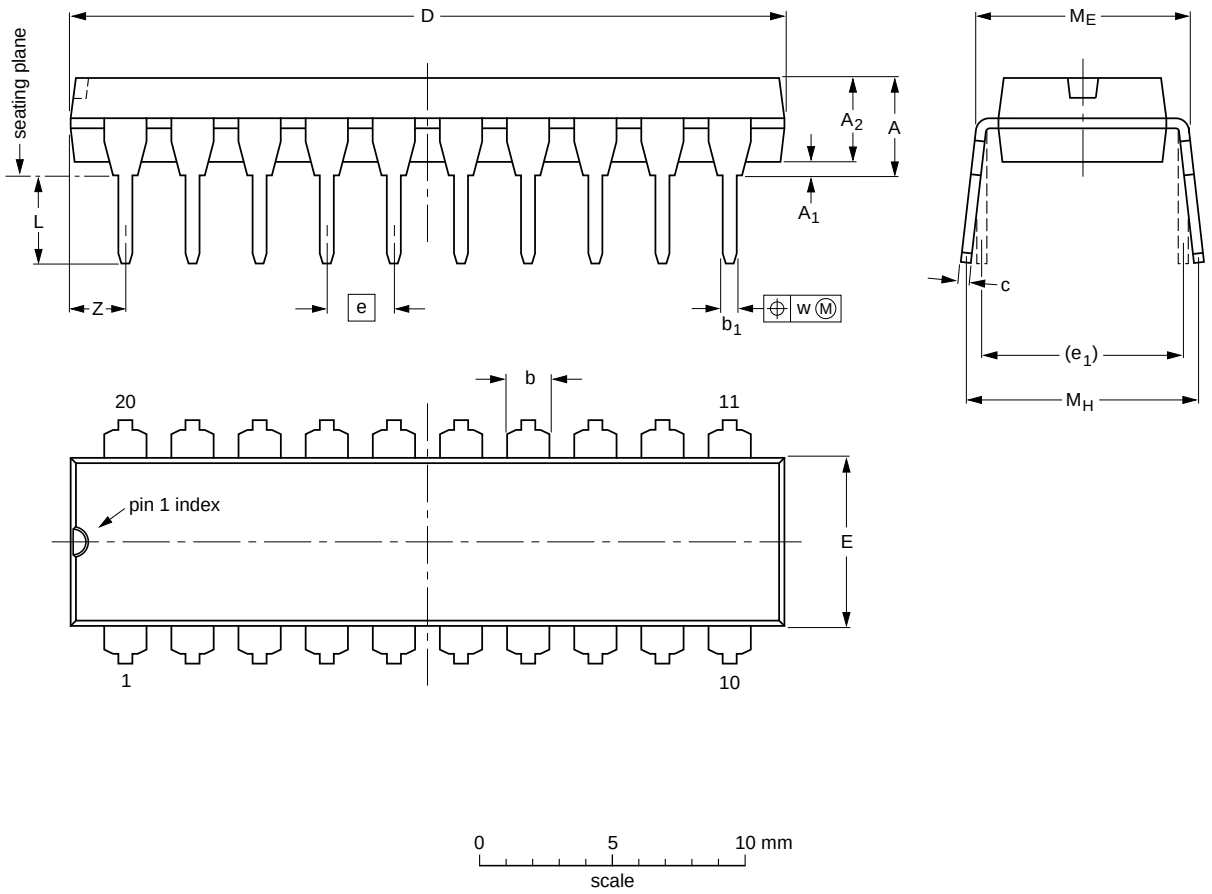


Fig.5 Typical application circuit.

PACKAGE OUTLINES

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

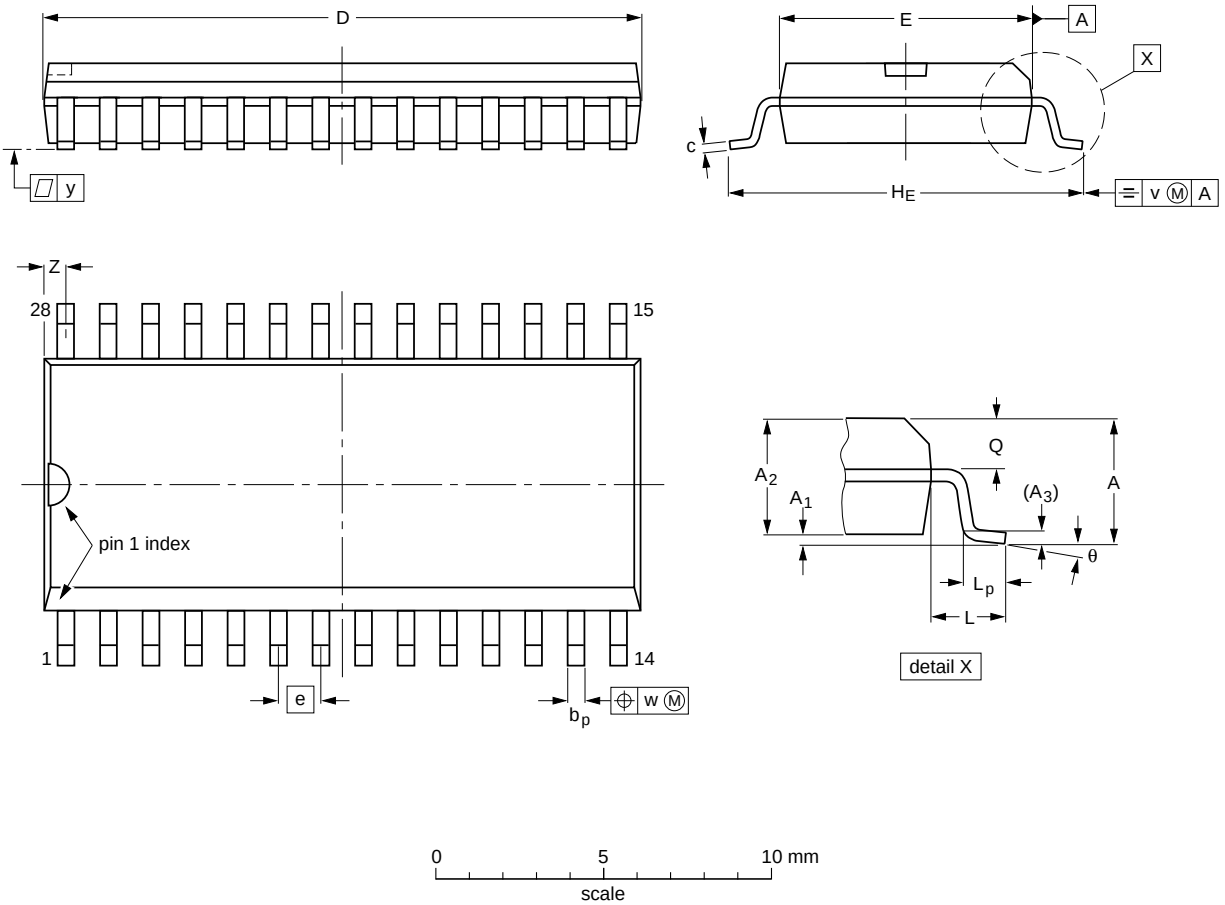
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic small outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.59+

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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