DATA SHEET

TDA8310A
PAL/NTSC colour processor for PIP applications

Product specification
Supersedes data of 1995 Nov 29
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Philips Semiconductors

PHILIPS

PAL/NTSC colour processor for PIP applications

TDA8310A

FEATURES

- Video switch with 2 CVBS inputs. One input can be switched between CVBS and Y/C and the circuit can automatically detect whether the incoming signal is CVBS or Y/C
- Integrated chrominance trap and bandpass filters (automatically calibrated)
- Integrated luminance delay line
- Automatic PAL/NTSC decoder which can decode all standards available in the world
- Easy interfacing with the TDA8395 (SECAM decoder) for multistandard applications
- Horizontal PLL with an alignment-free horizontal oscillator
- Vertical count-down circuit
- RGB/YUV and fast blanking switch with 3-state output and active clamping
- Low dissipation (560 mW)
- Small amount of peripheral components compared with competition ICs.

GENERAL DESCRIPTION

The TDA8310A is an alignment-free PAL/NTSC colour processor for Picture-in-Picture (PIP) applications. The main difference between the TDA8310 and the TDA8310A is that the vision IF amplifier has been omitted in the TDA8310A. Therefore, the circuit contains an input signal selector, a PAL/NTSC colour decoder, horizontal and vertical synchronization and an RGB/YUV switch.

The input signal selector has 2 CVBS inputs. One of the inputs can be switched between CVBS and Y/C and the circuit can automatically detect whether the incoming signal is CVBS or Y/C. The output signals for the PIP processor are;

Luminance signal

Colour difference signals (U and V)

Horizontal and vertical synchronization pulses.

The RGB/YUV switch can select between two RGB or YUV sources, e.g. between the PIP processor and the SCART input signal.

The supply voltage for the IC is 8 V. It is available in a 52-pin SDIP package.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8310A	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 19 and 41)	7.2	8.0	8.8	V
I_P	supply current	–	70	1.4	mA
Input voltages					
$V_{17,20(p-p)}$	CVBS/Y input voltage (peak-to-peak value)	–	1.0	–	V
$V_{16(p-p)}$	chrominance input voltage (peak-to-peak value)	–	0.3	–	V
$V_{i(p-p)}$	RGB/YUV input signal voltage amplitude (peak-to-peak value)	–	–	1.3	V
Output signals					
$V_{o(p-p)}$	luminance output voltage (peak-to-peak value)	–	1.4	–	V
$V_{50(p-p)}$	(B–Y) output voltage (peak-to-peak value)	1.06	1.33	1.6	V
$V_{51(p-p)}$	(R–Y) output voltage (peak-to-peak value)	0.84	1.05	1.26	V
V_{39}	horizontal sync pulse output voltage	–	4.0	–	V
V_{36}	vertical sync pulse output voltage	–	4.0	–	V
G_v	voltage gain of the RGB switches	–0.5	0	+0.5	dB
Control voltage					
$V_{control}$	control voltage for HUE	0	–	5.0	V

BLOCK DIAGRAM

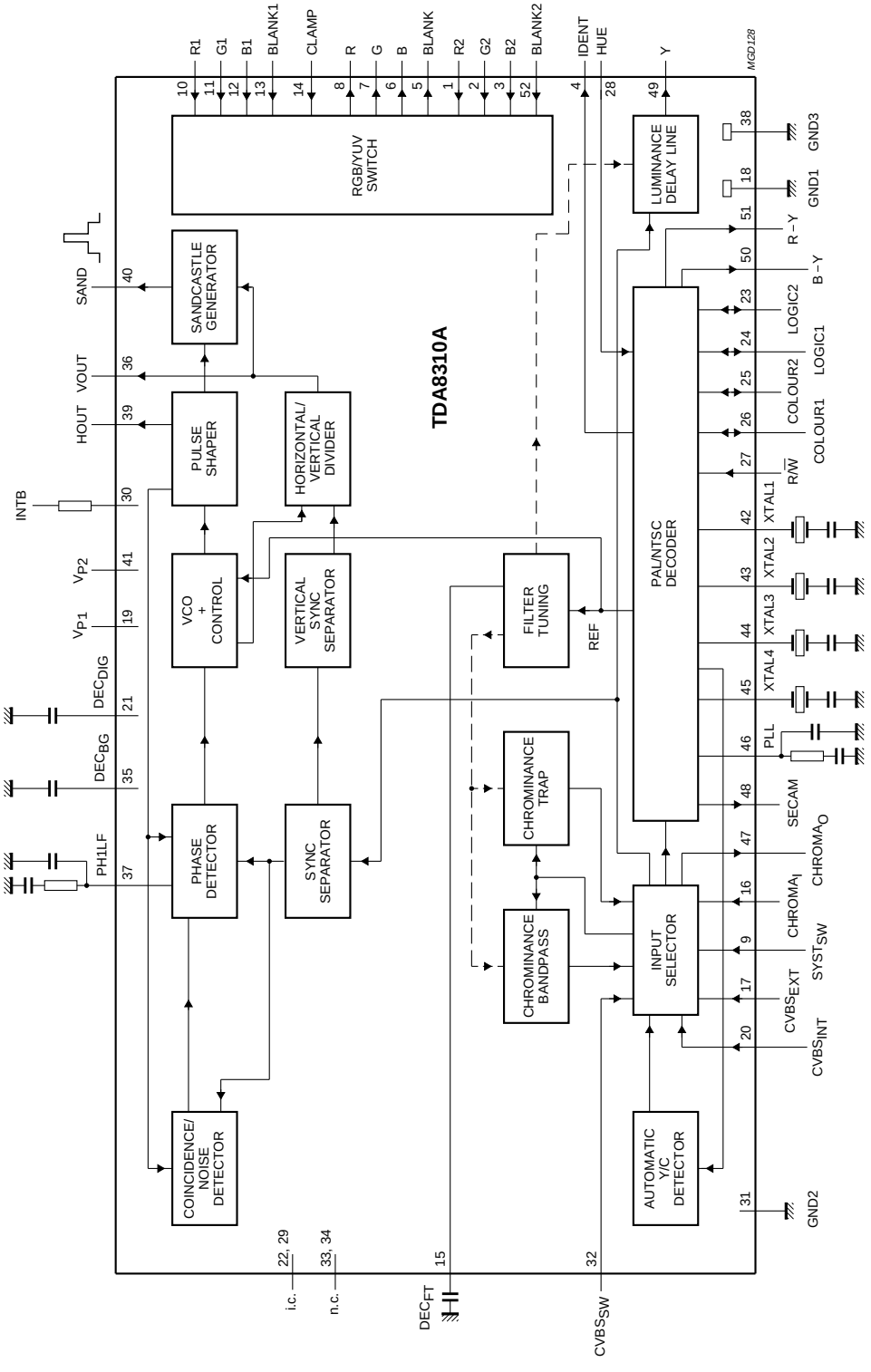


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
R2	1	RED input 2 (PIP)
G2	2	GREEN input 2 (PIP)
B2	3	BLUE input 2 (PIP)
IDENT	4	colour standard identification output
BLANK	5	blanking output
B	6	BLUE output
G	7	GREEN output
R	8	RED output
$SYST_{SW}$	9	CVBS/system switch
R1	10	RED input 1
G1	11	GREEN input 1
B1	12	BLUE input 1
BLANK1	13	blanking input 1
CLAMP	14	clamping pulse input
DEC_{FT}	15	decoupling filter tuning
$CHROMA_I$	16	chrominance input
$CVBS_{EXT}$	17	external CVBS/Y input
GND1	18	ground 1 (0 V)
V_{P1}	19	supply voltage 1 (+8 V)
$CVBS_{INT}$	20	internal CVBS input
DEC_{DIG}	21	decoupling digital supply rail
i.c.	22	internally connected (test purposes)
LOGIC2	23	crystal logic 2 input/output
LOGIC1	24	crystal logic 1 input/output
COLOUR2	25	colour system logic 2 input/output
COLOUR1	26	colour system logic 1 input/output
$R/\overline{W}$	27	read/write selection input

SYMBOL	PIN	DESCRIPTION
HUE	28	HUE control input
i.c.	29	internally connected (test purposes)
INTB	30	internal bias
GND2	31	ground 2 (0 V)
$CVBS_{SW}$	32	CVBS positive/negative modulation control switch input
n.c.	33	not connected
n.c.	34	not connected
DEC_{BG}	35	bandgap decoupling
VOUT	36	vertical sync output pulse
PH1LF	37	phase 1 loop filter
GND3	38	ground 3 (0 V)
HOUT	39	horizontal sync output pulse
SAND	40	sandcastle pulse output
V_{P2}	41	supply voltage 2 (+8 V)
XTAL1	42	4.4336 MHz crystal
XTAL2	43	3.5820 MHz crystal for PAL-N
XTAL3	44	3.5756 MHz crystal for PAL-M
XTAL4	45	3.5795 MHz crystal for NTSC
PLL	46	PLL colour filter
$CHROMA_O$	47	chrominance output for TDA8395
SECAM	48	SECAM reference output
Y	49	Y output
B–Y	50	B–Y output
R–Y	51	R–Y output
BLANK2	52	blanking/insertion input 2 (PIP)

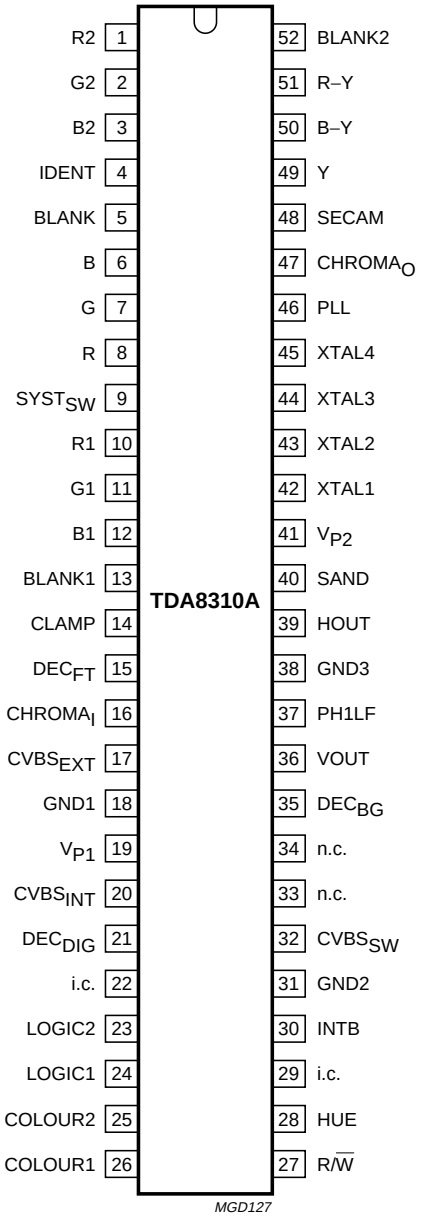


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

CVBS switch

The circuit contains a 2 input CVBS switch and one of the inputs can be switched between CVBS and Y/C. The circuit contains an identification circuit which can automatically switch between the CVBS and Y/C signals. It is also possible to force the switch to CVBS or Y/C.

Synchronization circuit

The sync separator is preceded by a voltage controlled amplifier which adjusts the sync pulse amplitude to a fixed level. The sync pulses are fed to the slicing stage (separator) which operates at 50% of the amplitude.

The separated sync pulses are fed to the first phase detector and to the coincidence detector. The coincidence detector is used to detect whether the line oscillator is synchronized and for transmitter identification. The first PLL has a very high static steepness this ensures that the phase of the picture is independent of the line frequency. The line oscillator operates at twice the line frequency.

The oscillator network is internal. Because of the spread of internal components an automatic adjustment circuit has been added to the IC.

The circuit compares the oscillator frequency with that of the crystal oscillator in the colour decoder. This results in a free-running frequency which deviates less than 2% from the typical value.

The horizontal output pulse is derived from the horizontal oscillator via a pulse shaper. The pulse width of the output pulse is 5.4 μs, the front edge of this pulse coincides with the front edge of the sync pulse at the input.

The vertical output pulse is generated by a count-down circuit. The pulse width is approximately 380 μs. Both the horizontal and vertical output pulses will always be available at the outputs even when no input signal is available.

In addition to the horizontal and vertical sync pulse outputs the IC has a sandcastle pulse output which contains burst key and blanking pulses.

Integrated video filters

The circuit contains a chrominance bandpass and trap circuit. The filters are realised by gyrator circuits that are automatically tuned by comparing the tuning frequency with the crystal frequency of the decoder. When a Y/C signal is supplied to the input the chrominance trap is automatically switched off by the Y/C detection circuit however, it is also possible to force the filters in the CVBS or Y/C position.

The luminance delay line is also realised by gyrator circuits.

Colour decoder

The colour decoder contains an alignment-free crystal oscillator, a colour killer circuit and colour difference demodulators. The 90° phase shift for the reference signal is achieved internally.

The colour decoder is very flexible. Together with the SECAM decoder (TDA8395) an automatic multistandard decoder can be designed but it is also possible to use it for one standard when only one crystal is connected to the IC. The decoder can be forced to one of the standards via the ‘forced mode’ pins. The crystal pins which are not used must be connected to the positive supply line via a 8.2 kΩ resistor. It is also possible to connect the non-used pins with one resistor to the positive supply line. In this event the resistor must have a value of 8.2 kΩ divided by the number of pins.

The chrominance output signal of the video switch is externally available and must be used as an input signal for the SECAM decoder.

RGB/YUV switch

The RGB/YUV switch is for switching between two RGB or YUV video sources. The outputs of the switch can be set to high-impedance state so that other switches can be used in parallel.

The switch is controlled via pins 13 and 52. The details of switch control are shown in Table 4.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	–	9.0	V
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	–25	+70	°C
T_{sld}	soldering temperature for 5 s	–	260	°C
T_j	maximum operating junction temperature	–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	≤40	K/W

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage (pins 19 and 41)		7.2	8.0	8.8	V
I_{P1}	supply current (pin 19)		45	65	80	mA
I_{P2}	supply current (pin 41)		3	5	10	mA
P_{tot}	total power dissipation		–	560	–	mW
R_{bias}	value of resistor to be connected between pin 30 and the positive supply line		–	10	–	kΩ
CVBS and Y/C switch						
INTERNAL CVBS AND EXTERNAL CVBS/Y INPUTS (PINS 20 AND 17)						
$V_{20,17(p\text{-}p)}$	CVBS/Y input voltage (peak-to-peak value)	notes 1 and 3	–	1	1.4	V
$I_{20,17}$	input current		–	4	6	µA
V_{clamp}	top sync clamping voltage level		–	3.3	–	V
I_{clamp}	clamping input current		80	100	–	µA
CHROMINANCE INPUT (PIN 16)						
$V_{16(p\text{-}p)}$	chrominance input voltage (peak-to-peak value)	notes 1, 4 and 11	–	0.3	–	V
$V_{16(p\text{-}p)}$	input signal amplitude before clipping occurs (peak-to-peak value)	note 2	1.0	–	–	V
R_I	chrominance input resistance		14	20	26	kΩ
C_I	chrominance input capacitance	note 1	–	–	5	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHROMINANCE OUTPUT (PIN 47)						
$V_{47(p-p)}$	output signal voltage amplitude (peak-to-peak value)		0.18	0.20	0.22	V
Z_O	output impedance		200	250	300	Ω
V_O	DC output voltage	open-circuit output	1.2	1.4	1.6	V
SWITCH CONTROL INPUT FOR INTERNAL/EXTERNAL POSITIVE/NEGATIVE MODULATION (PIN 32); note 5						
V_{32}	internal CVBS signal selected		–	–	1.0	V
V_{32}	external CVBS or Y/C signal selected		3.9	–	V_P	V
Z_I	input impedance		25	–	–	kΩ
ISS	suppression of non-selected video input signal	note 2	50	–	–	dB
SWITCH CONTROL INPUT FOR EXTERNAL CVBS OR Y/C SELECTION (PIN 9)						
V_9	filters switched to CVBS condition		–	–	1.0	V
V_9	filters switched to Y/C condition	note 6	2.0	–	3.0	V
V_9	automatic selection of CVBS or Y/C		3.9	–	V_P	V
Z_I	input impedance		25	–	–	kΩ
Chrominance filters, luminance delay line and luminance output						
CHROMINANCE TRAP CIRCUIT						
f_{trap}	trap frequency		–	f_{osc}	–	MHz
QF	trap quality factor	notes 2 and 7	–	2	–	
SR	colour subcarrier rejection		20	–	–	dB
CHROMINANCE BANDPASS CIRCUIT						
f_c	centre frequency		–	f_{osc}	–	MHz
QBP	bandpass quality factor	note 2	–	3	–	
Y DELAY LINE						
Δt_d	difference in delay time between the luminance and the demodulated chrominance signals	note 2	0	50	100	ns
B	bandwidth of internal delay line	note 2	8	–	–	MHz
Y OUTPUT (PIN 49)						
$V_{49(b-w)}$	output signal voltage amplitude (black-to-white value)	note 23	0.8	1.0	1.2	V
Z_O	output impedance		80	100	120	Ω
$V_{49(DC)}$	DC output voltage level (top sync)		2.7	2.9	3.1	V
I_{bias}	internal bias current of NPN emitter follower output transistor		0.4	0.5	–	mA
I_{source}	maximum source current		–	–	2	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal and vertical synchronization circuits						
SYNC VIDEO INPUT (PINS 17 AND 20)						
$V_{17,20}$	sync pulse voltage amplitude	note 1	50	300	–	mV
SL	slicing level	note 8	–	50	–	%
VERTICAL SYNC						
t_W	width of the vertical sync pulse without sync instability	note 9	22	–	–	µs
HORIZONTAL OSCILLATOR						
f_{fr}	free running frequency		–	15625	–	Hz
Δf_{fr}	spread on free running frequency		–	–	±2	%
$\Delta f_{osc}/\Delta V_P$	frequency variation with respect to the supply voltage	V_P = 8 V ±10%; note 2	–	0.2	0.5	%
Δf_{osc}	frequency variation with temperature	T_{amb} = 0 to 70 °C; note 2	–	–	80	Hz
$\Delta f_{osc(max)}$	maximum frequency deviation at the start of the horizontal output	no calibration	–	–	75	%
HORIZONTAL PLL (FILTER CONNECTED TO PIN 37); note 18						
f_{HR}	holding range PLL		–	±0.9	±1.2	kHz
f_{CR}	catching range PLL	note 2	±0.6	±0.9	–	kHz
S/N	signal-to-noise ratio of the video input signal at which the time constant is switched		14	20	26	dB
HYS	hysteresis at the switching point		1	3	6	dB
HORIZONTAL OUTPUT (PIN 39)						
V_{OH}	HIGH level output voltage	I_O = 2 mA	2.4	4.0	–	V
V_{OL}	LOW level output voltage	I_O = 2 mA	–	0.3	0.6	V
I_{sink}	sink current		–	–	2	mA
I_{source}	source current		–	–	2	mA
t_W	pulse width		–	5.4	–	µs
t_d	delay between the positive edge of the horizontal output pulse and the start of the horizontal sync pulse at the input		–	0	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VERTICAL OUTPUT (PIN 36); note 10						
f_{fr}	free running frequency		–	50/60	–	Hz
f_{lock}	locking range		45	–	64.5	Hz
	divider value not locked		–	625/525	–	lines
	locking range		488	–	722	lines/ frame
V_{OH}	HIGH level output voltage	I_{OL} = 2 mA	2.4	4.0	–	V
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	0.3	0.6	V
I_{sink}	sink current		–	–	2	mA
I_{source}	source current		–	–	2	mA
t_W	pulse width		–	380	–	µs
t_d	delay between the start of the vertical sync pulse at the input and the positive edge of the output pulse		–	37.5	–	µs
SANDCASTLE PULSE OUTPUT (PIN 40); note 16						
V_O	output voltage during scan	I_O = 1 mA; note 24	–	–	0.9	V
V_O	output voltage during burst key	I_O = 1 mA; note 24	4.1	–	5.2	V
Z_O	output impedance during blanking		1.0	–	–	MΩ
t_W	pulse width					
	burst key		3.3	3.5	3.7	µs
	line blanking		8.4	8.7	9.0	µs
	vertical blanking		–	14	–	lines
t_d	delay of start of burst key to start of sync		5.2	5.4	5.6	µs
Colour demodulation part						
CHROMINANCE AMPLIFIER						
ACC_{cr}	ACC control range	note 11	26	–	–	dB
ΔV	change in amplitude of the output signals over the ACC range		–	–	2	dB
THR_{on}	threshold colour killer ON		–38	–41	–44	dB
HYS_{off}	hysteresis colour killer OFF	note 2				
	strong input signal	S/N ≥ 40 dB	0	+3	+6	dB
	noisy input signal		0	+1	+8	dB
ACL CIRCUIT						
	chrominance burst ratio at which the ACL starts to operate		2.3	–	2.7	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REFERENCE PART						
Phase-locked loop; note 12						
f_{CR}	catching range		300	500	–	Hz
$\Delta\varphi$	phase shift for a ±300 Hz deviation of the oscillator frequency	note 2	–	–	2	deg
Oscillator						
TC_{osc}	temperature coefficient of f_{osc}	note 2	–	2.0	2.5	Hz/K
Δf_{osc}	f_{osc} deviation with respect to V_P	V_P = 8 V ±10%; note 2	–	–	250	Hz
R_I	input resistance (pins 43 to 45)	f_i = 3.58 MHz; note 1	–	1.5	–	kΩ
R_I	input resistance (pin 42)	f_i = 4.43 MHz; note 1	–	1	–	kΩ
C_I	input capacitance (pins 42 to 45)	note 1	–	–	10	pF
R	required resistance to V_P for a crystal pin which is not used	note 20	7.8	8.2	8.6	kΩ
HUE CONTROL INPUT (PIN 28); note 21						
HUE_{cr}	HUE control range	see also Fig.3	±35	±40	–	deg
$V_{control}$	control voltage to switch the colour PLL in the free-running mode	note 12	V_P – 1	–	–	V
R_I	input resistance		45	–	–	kΩ
DEMODULATOR OUTPUTS (PINS 50 AND 51)						
$V_{50(p-p)}$	−(B−Y) output signal voltage amplitude (peak-to-peak value)	note 25	1.06	1.33	1.60	V
$V_{51(p-p)}$	−(R−Y) output signal voltage amplitude (peak-to-peak value)	note 25	0.84	1.05	1.26	V
	spread of signal amplitude ratio PAL/NTSC	note 2	−1	–	+1	dB
Z_O	output impedance (R−Y)/(B−Y) output		–	–	500	Ω
B	bandwidth of demodulators	−3 dB; note 19	–	650	–	kHz
$V_{50(p-p)}$	(B−Y) residual carrier output voltage (peak-to-peak value)	f = f_{osc}	–	–	1	mV
		f = $2f_{osc}$	–	–	5	mV
$V_{51(p-p)}$	(R−Y) residual carrier output voltage (peak-to-peak value)	f = f_{osc}	–	–	1	mV
		f = $2f_{osc}$	–	–	5	mV
$V_{51(p-p)}$	H/2 ripple at (R−Y) output (peak-to-peak value)	only burst fed to input	–	–	25	mV
$\Delta V_O/\Delta T$	change of output signal amplitude with temperature	note 2	–	0.1	–	%/K
$\Delta V_O/\Delta V_P$	change of output signal amplitude with supply voltage	note 2	–	–	±0.1	dB
I_{bias}	internal bias current of NPN emitter follower output transistor		0.16	0.20	–	mA
I_{source}	maximum source current		–	–	1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DEMODULATION ANGLE AND GAIN RATIO						
	demodulation angle		85	90	95	deg
G	gain ratio of both demodulators G(B–Y) to G(R–Y)		1.60	1.78	1.96	
REFERENCE SIGNAL OUTPUT FOR TDA8395 (PIN 48)						
f_{ref}	reference frequency	note 13	–	4.43	–	MHz
$V_{48(p-p)}$	output signal amplitude (peak-to-peak value)		0.2	0.25	0.3	V
V_O	output voltage level	PAL/NTSC identified	1.5	1.6	1.7	V
V_O	output voltage level	no PAL/NTSC; SECAM (by TDA8395) identified	4.3	4.5	4.7	V
I_{48}	required current to force the decoder in SECAM mode		120	–	–	µA
STANDARD IDENTIFICATION AND FORCED SYSTEM SWITCHING (PINS 4 AND 23 TO 27); note 14						
$V_{I/O}$	input/output voltage					
	in ‘low’ condition		–	–	1.0	V
	in ‘high’ condition		4.0	–	5.3	V
$V_{I(max)}$	maximum input voltage	note 22	–	–	V_P	V
I_{load}	maximum load current (pins 23 to 26)		–	–	1	mA
I_I	input current (pins 23 to 26)					
	in ‘low’ or ‘high’ condition		–	–	1	µA
	when connected to V_P	note 22	–	–	10	µA
R_I	input resistance (pin 27)		80	–	–	kΩ
V_O	output voltage (pin 4)	I_O = 0.5 mA; notes 17 and 24				
	during PAL		–	–	0.9	V
	during SECAM		4.1	–	5.5	V
Z_O	output impedance (pin 4) during NTSC	note 17	1	–	–	MΩ
I_{load}	maximum load current (pin 4)		–	–	0.5	mA
RGB switch						
RGB INPUTS (PINS 1 TO 3 AND 10 TO 12)						
$V_{i(p-p)}$	signal voltage amplitude (peak-to-peak value)		–	–	1.3	V
Z_I	input impedance		100	–	–	kΩ
V_{clamp}	active clamping voltage level		2.6	2.8	3.0	V
I_{LI}	input leakage current	note 2	–	–	3	µA
I_{clamp}	active clamping current		–200	–	+200	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FAST BLANKING/SWITCH INPUTS (PINS 13 AND 52); note 15						
I_I	input current		–	–0.2	–0.3	mA
V_{IH}	HIGH level input voltage		0.9	–	3.0	V
V_{IL}	LOW level input voltage		0	–	0.5	V
t_d	delay between input and output pulse		–	–	50	ns
t_d	delay between switch input and RGB output		–	–	70	ns
V_{13}	input voltage on pin 13 to make RGB outputs and the fast blanking output high-ohmic		4	–	V_P	V
CLAMPING PULSE INPUT (PIN 14)						
V_{IH}	HIGH level input voltage		4.0	4.5	V_P	V
V_{IL}	LOW level input voltage		–	–	1	V
Z_I	input impedance		1	–	–	MΩ
RGB OUTPUTS (PINS 6 TO 8)						
G_v	voltage gain of the switches	f = 1 MHz	–0.5	0	+0.5	dB
G_{diff}	gain difference of the three channels		–	–	0.5	dB
Z_O	output impedance		–	–	150	Ω
$Z_{O(off)}$	output impedance in the ‘off’ state	f = 10 MHz	100	–	–	kΩ
V_O	output voltage during blanking	open-circuit output	1.2	1.4	1.6	V
V_{os}	blanking off-set voltage of the two sources		–	–	5	mV
$I_{source(max)}$	maximum source current		–	–	1	mA
I_{bias}	internal bias current of NPN emitter follower output transistor		0.16	0.2	–	mA
ISS	input signal suppression when RGB outputs are high-ohmic	f = 5 MHz; note 2	60	–	–	dB
		f = 10 MHz; note 2	50	–	–	dB
		f = 22 MHz; note 2	40	–	–	dB
α_{ct}	crosstalk between the two RGB channels	f = 5 MHz; note 2	–60	–	–	dB
		f = 10 MHz; note 2	–50	–	–	dB
		f = 22 MHz; note 2	–40	–	–	dB
B	bandwidth of the RGB channels	C_L = 20 pF; note 2				
	gain reduction –0.5 dB		5	–	–	MHz
	gain reduction –1 dB		10	–	–	MHz
	gain reduction –3 dB		22	–	–	MHz
t_d	delay from RGB input to output	note 2	–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FAST BLANKING OUTPUT (PIN 5)						
V_{OH}	HIGH level output voltage		2	–	3	V
V_{OL}	LOW level output voltage		0	–	0.3	V
Z_O	output impedance		–	–	300	Ω
$Z_{O(off)}$	output impedance in the 'off' state		100	–	–	kΩ
t_r	rise time of the output pulse		–	–	30	ns
t_f	fall time of the output pulse		–	–	30	ns
t_d	delay difference between fast blanking and RGB at the outputs		–	–	30	ns
I_{load}	maximum load current		–	–	1	mA

Notes

1. This parameter is not tested during production and is just given as application information for the designer of the television receiver.
2. This parameter is not tested during production but is guaranteed by the design and qualified by means of matrix batches which are made in the pilot production period.
3. Signal with negative-going sync. Amplitude includes sync pulse amplitude.
4. Burst amplitude; for a colour bar with 75% saturation the chrominance signal amplitude is 660 mV (p-p).
5. The IC has two 3-level switch control inputs for the selection of the video signal for the decoder and synchronization circuits. The video source for internal or external signal is selected via pin 32, also the polarity of the demodulation for the internal signal. When the video switch is in the external position the voltage level of pin 9 determines whether the video filters are switched to CVBS or Y/C. It is also possible via pin 9 to select an automatic detection of the Y/C signal.
6. This value is internally generated when the pin is left open-circuit (the minimum value of the series resistor is 25 kΩ).
7. The –3 dB bandwidth of the circuit can be calculated by means of the following equation:

$$f_{-3\ dB} = f_{osc}\left(1 - \frac{1}{2Q}\right)$$

8. The slicing level is independent of the sync pulse amplitude.
9. The horizontal and vertical sync are stable while processing Copy Guard signals and signals with phase shifted sync pulses (stretched tapes). Trick mode conditions of the VCR will also not disturb the synchronization. The value given is the delay caused by the vertical sync pulse integrator. The integrator has been designed such that the vertical sync is not disturbed for special anti-copy tapes with vertical sync pulses with an on/off time of 10/22 μs.
10. The timing pulses for the vertical ramp generator are obtained from the horizontal oscillator via a divider circuit. This divider circuit has 2 search modes of operation:
    a) The 'large window' mode is switched on when the circuit is not synchronized or, when a non-standard signal is received (the number of lines per frame in the 50 Hz mode is between 311 and 314 and in the 60 Hz mode between 261 and 264). In the search mode the divider can be triggered between line 244 and line 361 (approximately 45 to 64.5 Hz).
    b) The 'narrow window' mode is switched on when more than 15 successive vertical sync pulses are detected in the narrow window. When the circuit is in the standard mode and a vertical sync pulse is missing the retrace of the vertical ramp generator is started at the end of the window. Consequently, the disturbance of the picture is very small. The circuit will switch back to the search window when, for 6 successive vertical periods, no sync pulses are found within the window.

11. At a chrominance input voltage of 660 mV (p-p) (colour bar with 75% saturation i.e. burst signal amplitude 300 mV (p-p)) as given in Characteristics first parameter of Section “Chrominance input (pin 16)” the dynamic range of the ACC is +6 and −20 dB.
12. All frequency variations are referenced to 3.58/4.43 MHz carrier frequency. All oscillator specifications are measured with the Philips crystal series 9922 520. If the spurious response of the 4.43 MHz crystal is lower than −3 dB with respect to the fundamental frequency for a damping resistance of 1 kΩ, oscillation at the fundamental frequency is guaranteed. The spurious response of the 3.58 MHz crystal must be lower than −3 dB with respect to the fundamental frequency for a damping resistance of 1.5 kΩ. The catching and detuning range are measured for nominal crystal parameters. These are:
    a) Load resonance frequency f_0 (C_L = 20 pF) = 4.433619 or 3.579545 MHz
    b) Motional capacitance C_M = 20.6 fF (4.43 MHz crystal) or 14.7 fF (3.58 MHz crystal)
    c) Parallel capacitance C_0 = 5.5 pF (4.43 MHz crystal) or 4.5 pF (3.58 MHz crystal).

    The actual load capacitance in the application should be C_L = 18 pF to account for parasitic capacitances on and off chip.

    The free-running frequency of the oscillator can be checked by the HUE control pin to the positive supply rail. In that condition the colour killer is not active so that the frequency offset is visible on the screen. When two or more crystals are connected to the IC the circuit must be forced to one of the crystals during this test to prevent the oscillator continuously switching between the various frequencies.
13. The reference signal for the TDA8395 is available only when the crystal oscillator is operating at a frequency of 4.43 MHz. When a SECAM signal is identified this signal is only available during the vertical retrace period thus avoiding crosstalk with the incoming SECAM signal during scan.
14. The identified colour standard can be read from the IC in two ways:
    a) From the voltage level of pin 4. The voltage during the demodulation of the various standards is given in the last three parameters of this section.
    b) From the pins 23 to 26 when pin 27 is in the ‘read’ mode.

    When pin 27 is in the ‘write’ mode the colour decoder can be forced to one of the colour standards. The levels for the various standards are given in Tables 1, 2 and 3.
15. The control possibilities of the RGB switch via pins 13 and 52 are shown in Table 4.
16. To obtain a simple interface between the TDA8310A and the PIP processor the sandcastle output has been designed such that the output is pulled down during scan and pulled up during the burst key pulse. During blanking the output is high-ohmic and therefore the output voltage is determined by the load.
17. The output of pin 4 is designed similar to the sandcastle output. The output is pulled down during PAL and pulled up during SECAM. During NTSC the pin is floating so that the output level is determined by the load.
18. To obtain a good performance for both weak signal and VCR playback the time constant of the first control loop is switched depending on the input signal condition. Therefore the circuit contains a noise detector and the time constant is switched to ‘slow’ when excessive noise is present in the signal. This occurs when the internal video signal is selected or for an external CVBS signal when the chrominance input (pin 16) is left open-circuit. The time constant is always ‘fast’ when the chrominance input pin is connected to ground and the input is switched to the Y/C mode. In the ‘fast’ mode during the vertical retrace time the phase detector current is increased 50% so that phase errors due to head-switching of the VCR are corrected as soon as possible.

    During weak signal conditions (noise detector active) the phase detector is gated and the width of the gate pulse has a value of 5.7 µs so that the effect of the noise is reduced to a minimum.

    The output current of the phase detector for the various conditions is shown in Table 5.
19. This value indicates the bandwidth of the complete chrominance circuit including the chrominance bandpass filter. The bandwidth of the demodulator low-pass filter is approximately 1 MHz.

20. The crystal pins which are not used must be connected to the positive supply line via an 8.2 kΩ resistor. It is also possible to connect the non-used pins together and use a resistor with a value of 8.2 kΩ divided by the number of pins which are not used.
21. When this pin is left open-circuit the HUE control is set to the nominal value.
22. When one or more pins have to be connected to the positive supply line the **total** current must be limited to 40 μA. This can be achieved by connecting these pins together and connecting them to a positive supply line via a 100 kΩ resistor. When separate resistors are used a resistor with a higher value must be used so that the total current is limited to the required level.
23. This output signal value is obtained when the CVBS or Y input signal at pins 17 and/or 20 has an amplitude of 0.7 V (black-to-white value).
24. The output buffer consists of a combination of a PMOS and an NMOS. The maximum output impedance in the low state can be calculated by dividing the maximum output voltage (for this parameter 0.9 V) by the specified current. For the high state this resistance can be calculated by dividing the difference between the maximum and minimum output voltage by the specified current. The output impedance is independent of the value of the output current.
25. These output signal values are obtained for a colour bar input signal with 75% saturation.

Table 1 Read/write pin input (pin 27)

MODE	LEVEL
Decoder automatic	LOW
Forced decoder mode	HIGH

Table 2 Colour system logic (pins 25 and 26)

PIN 25	PIN 26	STANDARD
LOW	LOW	auto/no colour
LOW	HIGH	PAL
HIGH	LOW	NTSC
HIGH	HIGH	SECAM

Table 3 Crystal logic (pins 23 and 24)

PIN 23	PIN 24	SELECTED CRYSTAL (MHz)
LOW	LOW	4.43
LOW	HIGH	3.579 (NTSC)
HIGH	LOW	3.575 (PAL-M)
HIGH	HIGH	3.582 (PAL-N)

Table 4 Control logic RGB switch (pins 13 and 52)

PIN 13	PIN 52	RGB OUTPUT	FAST BLANKING OUTPUT
LOW	LOW	black	LOW
LOW	HIGH	RGB 2	HIGH
HIGH	LOW	RGB 1	HIGH
HIGH	HIGH	RGB 2	HIGH

Table 5 Output current of phase detector

CURRENT PHASE DETECTOR DURING	SCAN (μA)	VERTICAL RETRACE (μA)	GATED YES/NO
Weak signal and synchronized	30	30	YES (5.7 μs)
Strong signal and synchronized	180	270	NO
Not synchronized	180	270	NO

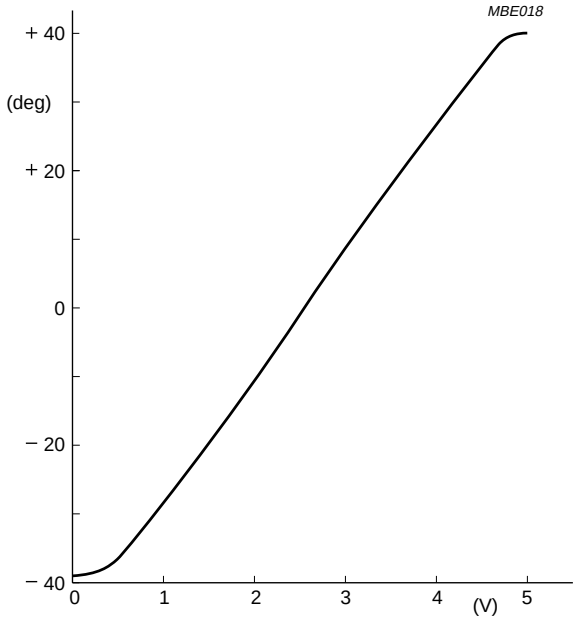
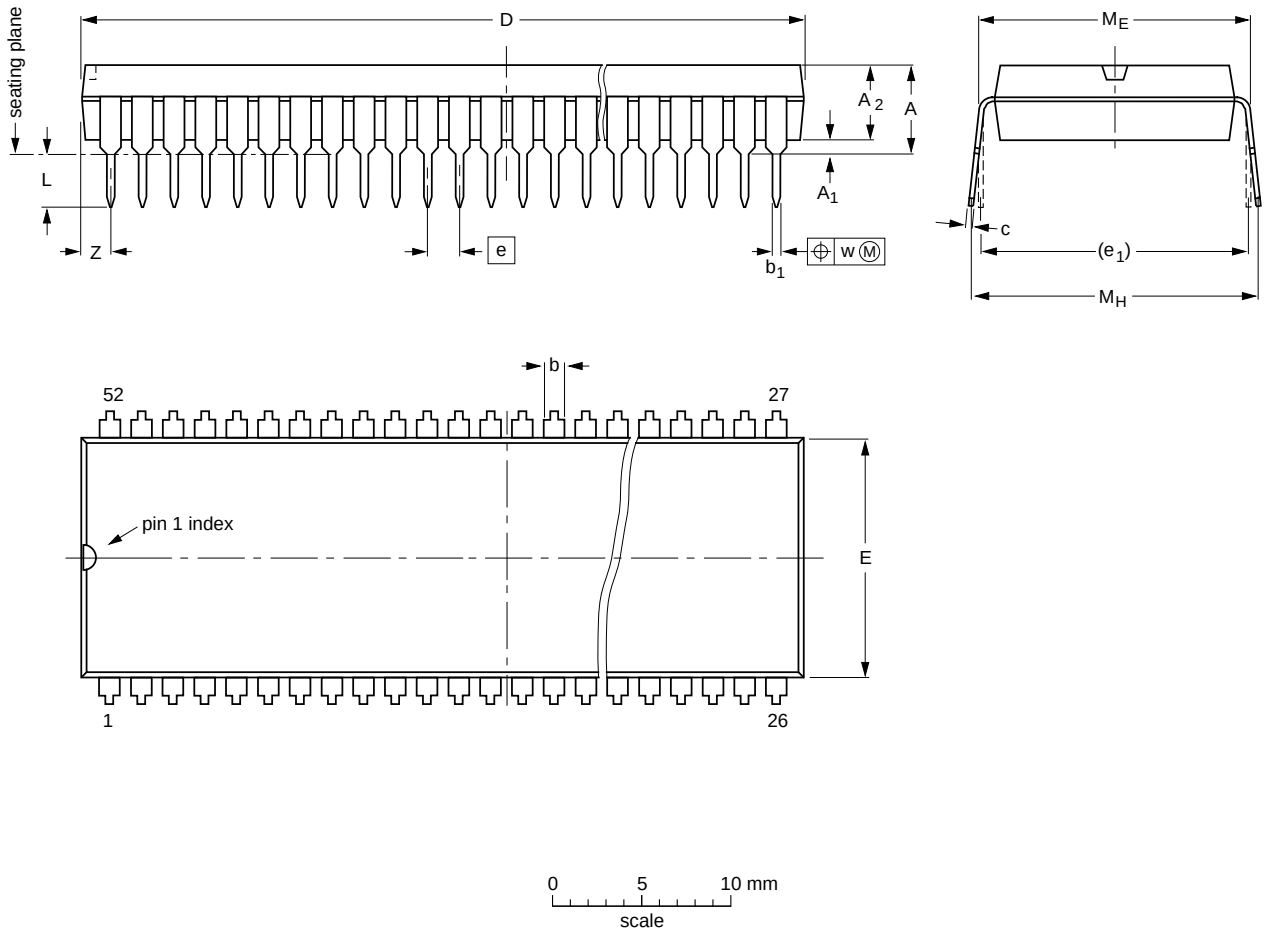


Fig.3 HUE control curve.

PACKAGE OUTLINE

SDIP52: plastic shrink dual in-line package; 52 leads (600 mil) **SOT247-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	47.9 47.1	14.0 13.7	1.778	15.24	3.2 2.8	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT247-1						~~90-01-22~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.