Low-power smart card coupler TDA8005

FEATURES

- V_{CC} generation (5 V ±5%, 20 mA maximum with controlled rise and fall times)
- Clock generation (up to 8 MHz), with two times synchronous frequency doubling
- Clock STOP HIGH, clock STOP LOW or 1.25 MHz (from internal oscillator) for cards power-down mode
- Specific UART on I/O for automatic direct/inverse convention settings and error management at character level
- Automatic activation and deactivation sequences through an independent sequencer
- Supports the protocol T = 0 in accordance with ISO 7816, GSM11.11 requirements (Global System for Mobile communication); and EMV banking specification approved for Final GSM11.11 Test Approval (FTA)
- Several analog options are available for different applications (doubler or tripler DC/DC converter, card presence, active HIGH or LOW, threshold voltage supervisor, etc.
- Overloads and take-off protections
- Current limitations in the event of short-circuit
- Special circuitry for killing spikes during power-on or off
- Supply supervisor
- Step-up converter (supply voltage from 2.5 to 6 V)
- Power-down and sleep mode for low-power consumption
- Enhanced ESD protections on card side (6 kV minimum)
- Control and communication through a standard RS232 full duplex interface
- Optional additional I/O ports for:
  - keyboard
  - LEDs
  - display
  - etc.
- 80CL51 microcontroller core with 4 kbytes ROM and 256-byte RAM.

APPLICATIONS

- Portable smart card readers for protocol T = 0
- GSM mobile phones.

GENERAL DESCRIPTION

The TDA8005 is a low cost card interface for portable smart card readers. Controlled through a standard serial interface, it takes care of all ISO 7816 and GSM11-11 requirements. It gives the card and the set a very high level of security, due to its special hardware against ESD, short-circuiting, power failure, etc. Its integrated step-up converter allows operation within a supply voltage range of 2.5 to 6 V.

The very low-power consumption in Power-down and sleep modes saves battery power. A special version where the internal connections to the controller are fed outside through pins allows easy development and evaluation, together with a standard 80CL51 microcontroller.

Development tools, application report and support (hardware and software) are available.

The device can be supplied either as a masked chip with standard software handling all communication between smart card and a master controller in order to make the application easier, or as a maskable device.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	doubler and tripler option	2.5	–	6.0	V
$I_{DD(pd)}$	supply current in power-down mode	V_{DD} = 5 V; card inactive	–	–	100	µA
$I_{DD(sm)}$	supply current in sleep mode	card powered but clock stopped	–	–	500	µA
$I_{DD(om)}$	supply current in operating mode	unloaded; f_{xtal} = 13 MHz; $f_{\mu C}$ = 6.5 MHz; f_{card} = 3.25 MHz	–	–	5.5	mA
V_{CC}	card supply voltage	including static and dynamic loads on 100 nF capacitor	4.75	5.0	5.25	V
I_{CC}	card supply current	operating	–	–	20	mA
		limitation	–	–	30	mA
SR	slew rate on V_{CC} (rise and fall)	maximum load capacitor 150 nF (including typical 100 nF decoupling)	0.05	0.1	0.15	V/µs
t_{de}	deactivation cycle duration		–	–	100	µs
t_{act}	activation cycle duration		–	–	100	µs
f_{xtal}	crystal frequency		2	–	16	MHz
T_{amb}	operating ambient temperature		–25	–	+85	°C

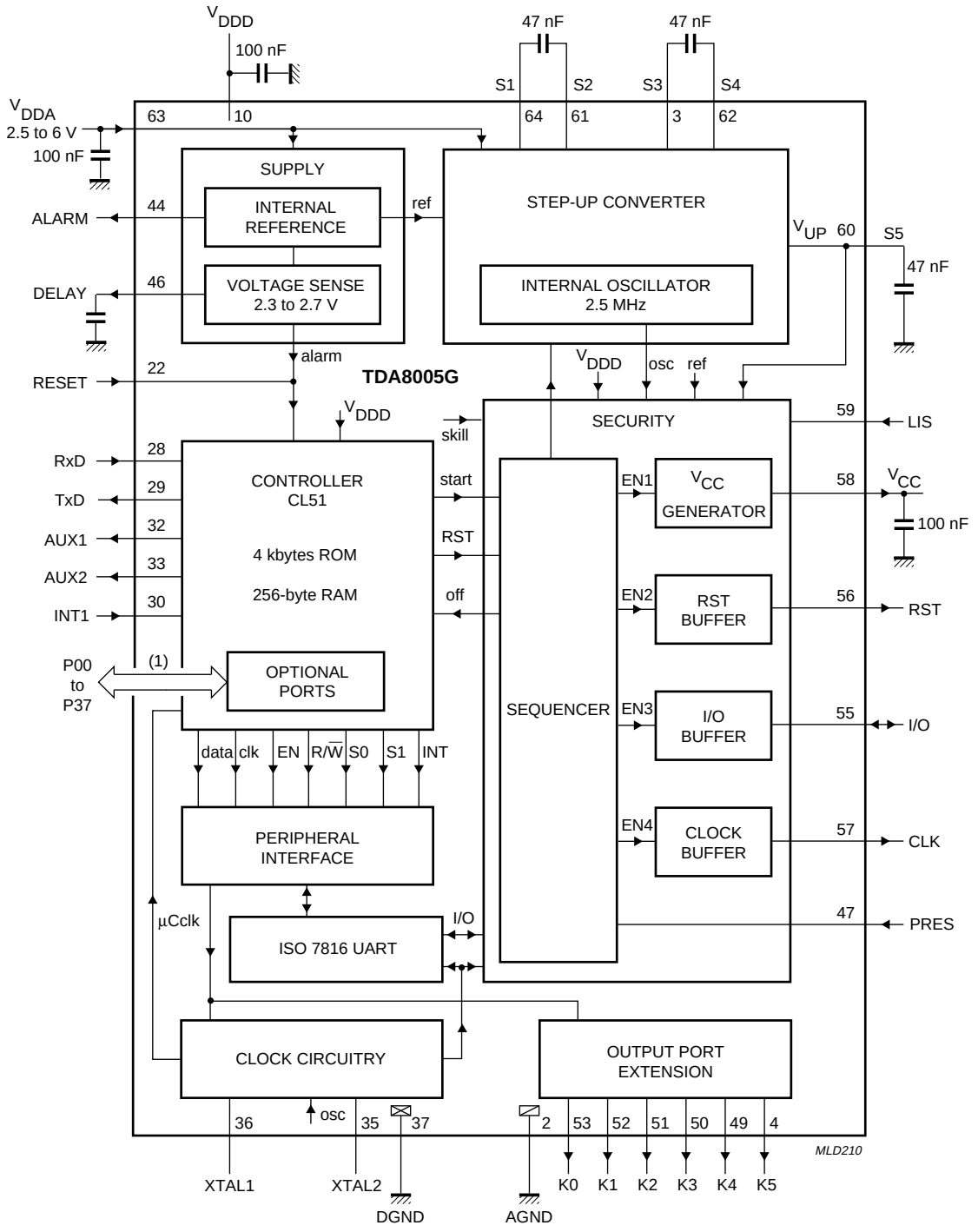
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8005G	LQFP64[1]	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
TDA8005H	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM



(1) For details see Chapter “Pinning”.

Fig.1 Block diagram (LQFP64; SOT314-2).

PINNING

SYMBOL	PIN		DESCRIPTION
	LQFP64 SOT314-2	QFP44 SOT307-2	
n.c.	1	–	not connected
AGND	2	1	analog ground
S3	3	2	contact 3 for the step-up converter
K5	4	–	output port from port extension
P03	5	3	general purpose I/O port (connected to P03)
P02	6	4	general purpose I/O port (connected to P02)
P01	7	5	general purpose I/O port (connected to P01)
n.c.	8	–	not connected
P00	9	6	general purpose I/O port (connected to P00)
V_{DDD}	10	7	digital supply voltage
n.c.	11	–	not connected
TEST1	12	8	test pin 1 (connected to P10; must be left open-circuit in the application)
P11	13	9	general purpose I/O port or interrupt (connected to P11)
P12	14	10	general purpose I/O port or interrupt (connected to P12)
P13	15	11	general purpose I/O port or interrupt (connected to P13)
P14	16	12	general purpose I/O port or interrupt (connected to P14)
n.c.	17	–	not connected
P15	18	13	general purpose I/O port or interrupt (connected to P15)
P16	19	14	general purpose I/O port or interrupt (connected to P16)
TEST2	20	15	test pin 2 (connected to PSEN; must be left open-circuit in the application)
P17	21	16	general purpose I/O port or interrupt (connected to P17)
RESET	22	17	input for resetting the microcontroller (active HIGH)
n.c.	23	–	not connected
n.c.	24	–	not connected
n.c.	25	–	not connected
n.c.	26	–	not connected
n.c.	27	–	not connected
RxD	28	18	serial interface receive line
TxD	29	19	serial interface transmit line
INT1	30	20	general purpose I/O port or interrupt (connected to P33)
T0	31	21	general purpose I/O port (connected to P34)
AUX1	32	22	push-pull auxiliary output (±5 mA; connected to timer T1 e.g. P35)
AUX2	33	23	push-pull auxiliary output (±5 mA; connected to timer P36)
P37	34	24	general purpose I/O port (connected to P37)
XTAL2	35	25	crystal connection
XTAL1	36	26	crystal connection or external clock input
DGND	37	27	digital ground
n.c.	38	–	not connected

SYMBOL	PIN		DESCRIPTION
	LQFP64 SOT314-2	QFP44 SOT307-2	
n.c.	39	–	not connected
P20	40	28	general purpose I/O port (connected to P20)
P21	41	–	general purpose I/O port (connected to P21)
P22	42	29	general purpose I/O port (connected to P22)
P23	43	30	general purpose I/O port (connected to P23)
ALARM	44	–	open-drain output for Power-On Reset (active HIGH or LOW by mask option)
n.c.	45	–	not connected
DELAY	46	31	external capacitor connection for delayed reset signal
PRES	47	32	card presence contact input (active HIGH or LOW by mask option)
TEST3	48	33	test pin 3 (must be left open-circuit in the application)
K4	49	–	output port from port extension
K3	50	–	output port from port extension
K2	51	–	output port from port extension
K1	52	–	output port from port extension
K0	53	–	output port from port extension
TEST4	54	34	test pin 4 (must be left open-circuit in the application)
I/O	55	35	data line to/from the card (ISO C7 contact)
RST	56	36	card reset output (ISO C2 contact)
CLK	57	37	clock output to the card (ISO C3 contact)
V_{CC}	58	38	card supply output voltage (ISO C1 contact)
LIS	59	39	supply for low-impedance on cards contacts
S5	60	40	contact 5 for the step-up converter
S2	61	41	contact 2 for the step-up converter
S4	62	42	contact 4 for the step-up converter
V_{DDA}	63	43	analog supply voltage
S1	64	44	contact 1 for the step-up converter

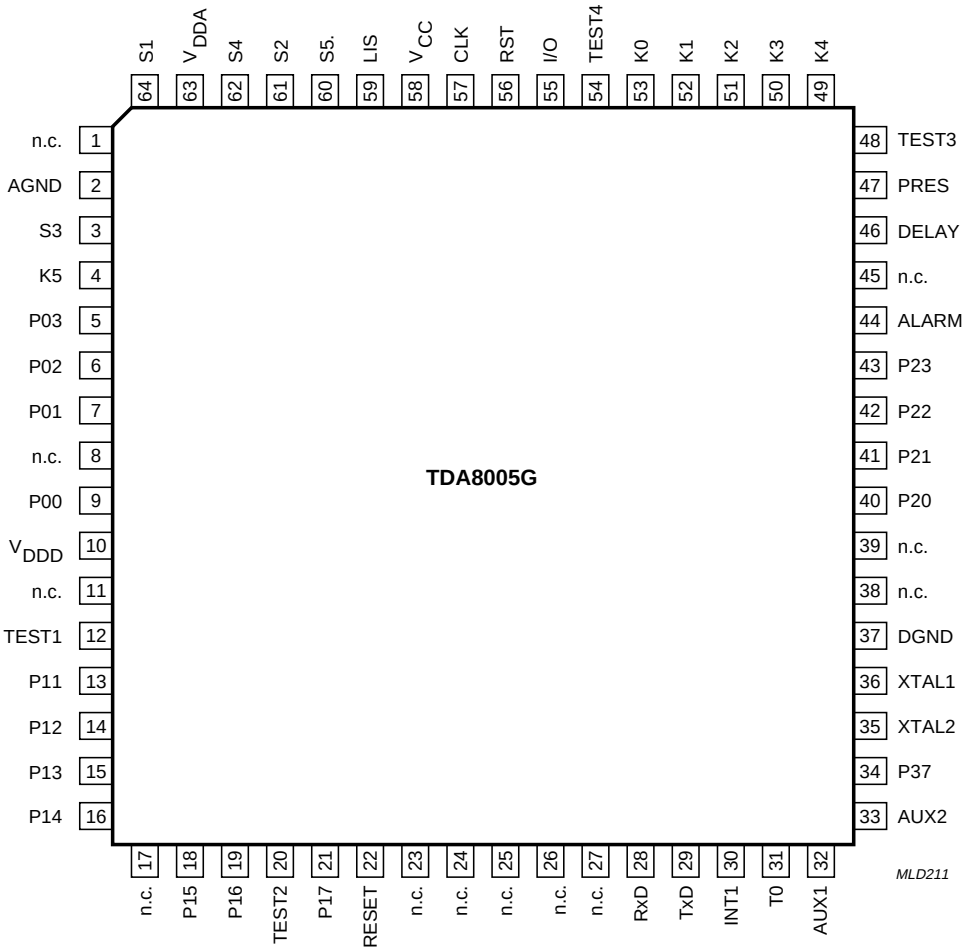


Fig.2 Pin configuration (LQFP64; SOT314-2).

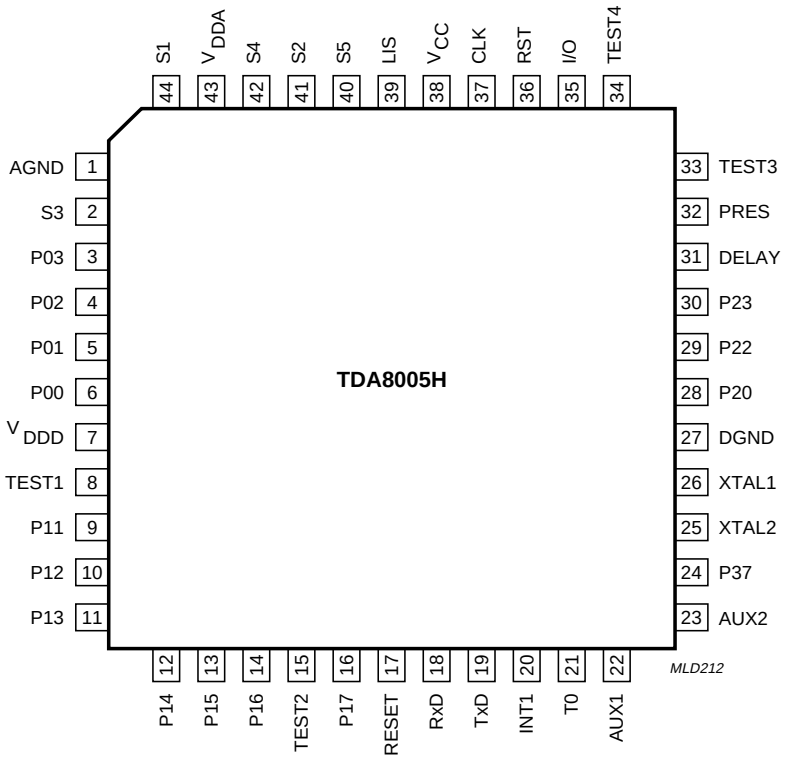


Fig.3 Pin configuration (QFP44; SOT307-2).

FUNCTIONAL DESCRIPTION

Microcontroller

The microcontroller is an 80CL51 with 256 bytes of RAM instead of 128. The baud rate of the UART has been multiplied by four in modes 1, 2 and 3 (which means that the division factor of 32 in the formula is replaced by 8 in both reception and transmission, and that in the reception modes, only four samples per bit are taken with decision on the majority of samples 2, 3 and 4) and the delay counter has been reduced from 1536 to 24. All the other functions remain unchanged. Please, refer to the published specification of the 80CL51 for any further information. Pins INT0, P10, P04 to P07 and P24 to P27 are used internally for controlling the smart card interface.

Mode 0 is unchanged. The baud rate for modes 1 and 3 is $\frac{2^{SMOD}}{8} \times \frac{f_{clk}}{12 \times (256 - TH1)}$

The baud rate for mode 2 is $\frac{2^{SMOD}}{16} \times f_{clk}$

Table 1 Mode 3 timing

BAUD RATE	f_{clk} = 6.5 MHz; V_{DD} = 5 V		f_{clk} = 3.25 MHz; V_{DD} = 5 or 3 V	
	SMOD	TH1	SMOD	TH1
135416	1	255	–	–
67708	0	255	1	255
45139	1	253	–	–
33854	0	254	0	255
27083	1	251	–	–
22569	0	253	1	253
16927	–	–	0	254
13542	–	–	1	251
11285	0	250	0	253

Supply

The circuit operates within a supply voltage range of 2.5 to 6 V. The supply pins are V_{DDD}, V_{DDA}, DGND and AGND. Pins V_{DDA} and AGND supply the analog drivers to the card and have to be externally decoupled because of the large current spikes that the card and the step-up converter can create. An integrated spike killer ensures the contacts to the card remain inactive during power-up or power-down. An internal voltage reference is generated which is used within the step-up converter, the voltage supervisor, and the V_{CC} generator.

The voltage supervisor generates an alarm pulse, whose length is defined by an external capacitor tied to the DELAY pin, when V_{DDD} is too low to ensure proper operation (1 ms per 1 nF typical). This pulse is used as a RESET pulse by the controller, in parallel with an external RESET input, which can be tied to the system controller. It is also used in order to either block any spurious card contacts during controllers reset, or to force an automatic deactivation of the contacts in the event of supply drop-out (see Sections “Activation sequence” and “Deactivation sequence”).

In the 64 pin version, this reset pulse is output to the open drain ALARM pin, which may be selected active HIGH or active LOW by mask option and may be used as a reset pulse for other devices within the application.

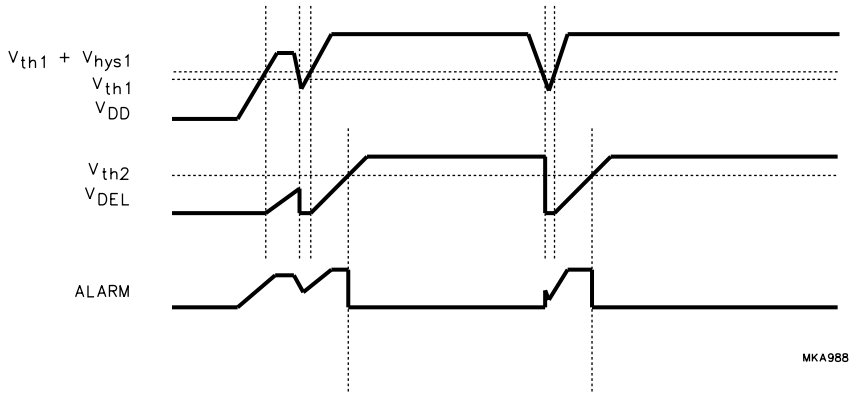


Fig.4 Supply supervisor.

Low impedance supply (pin LIS)

For some applications, it is mandatory that the contacts to the card (V_{CC}, RST, CLK and I/O) are low impedance while the card is inactive and also when the coupler is not powered. An auxiliary supply voltage on pin LIS ensures this condition where I_{LIS} = <5 µA for V_{LIS} = 5 V. This low impedance situation is disabled when V_{CC} starts rising during activation, and re-enabled when the step-up converter is stopped during deactivation. If this feature is not required, the LIS pin must be tied to V_{DD}.

Step-up converter

Except for the V_{CC} generator, and the other cards contacts buffers, the whole circuit is powered by V_{DDD} and V_{DDA}. If the supply voltage is 3 V or 5 V, then a higher voltage is needed for the ISO contacts supply. When a card session is requested by the controller, the sequencer first starts the step-up converter, which is a switched capacitors type, clocked by an internal oscillator at a frequency approximately 2.5 MHz. The output voltage, V_{UP}, is regulated at approximately 6 V and then fed to the V_{CC} generator. V_{CC} and GND are used as a reference for all other cards contacts. The step-up converter may be chosen as a doubler or a tripler by mask option, depending on the voltage and the current needed on the card.

ISO 7816 security

The correct sequence during activation and deactivation of the card is ensured through a specific sequencer, clocked by a division ratio of the internal oscillator.

Activation (START signal P05) is only possible if the card is present (PRES HIGH or LOW according to mask option), and if the supply voltage is correct (ALARM signal inactive), CLK and RST are controlled by RSTIN (P04), allowing the correct count of CLK pulses during Answer-to-Reset from the card.

The presence of the card is signalled to the controller by the OFF signal (P10).

During a session, the sequencer performs an automatic emergency deactivation in the event of card take-off, supply voltage drop, or hardware problems. The OFF signal falls thereby warning the controller

Clock circuitry

The clock to the microcontroller and the clock to the card are derived from the main clock signal (XTAL from 2 to 16 MHz, or an external clock signal).

Microcontroller clock (f_{clk}) after reset, and during power reduction modes, the microcontroller is clocked with $f_{INT}/8$, which is always present because it is derived from the internal oscillator and gives the lowest power consumption. When required, (for card session, serial communication or anything else) the microcontroller may choose to clock itself with $\frac{1}{2}f_{xtal}$, $\frac{1}{4}f_{xtal}$ or $\frac{1}{2}f_{INT}$. All frequency changes are synchronous, thereby ensuring no hang-up due to short spikes etc.

Cards clock: the microcontroller may select to send the card $\frac{1}{2}f_{xtal}$, $\frac{1}{4}f_{xtal}$, $\frac{1}{8}f_{xtal}$ or $\frac{1}{2}f_{INT}$ (~1.25 MHz), or to stop the clock HIGH or LOW. All transition are synchronous, ensuring correct pulse length during start or change in accordance with ISO 7816.

After power on, CLK is set at STOP LOW, and f_{clk} is set at $\frac{1}{8}f_{INT}$.

Power-down and sleep modes

The TDA8005 offers a large flexibility for defining power reduction modes by software. Some configurations are described below.

In the power-down mode, the microcontroller is in power-down and the supply and the internal oscillator are active. The card is not active; this is the smallest power consumption mode. Any change on P1 ports or on PRES will wake-up the circuit (for example, a key pressed on the keyboard, the card inserted or taken off).

In the sleep mode, the card is powered, but configured in the Idle or sleep mode. The step-up converter will only be active when it is necessary to reactivate V_{UP}. When the microcontroller is in Power-down mode any change on P1 ports or on PRES will wake up the circuit.

In both power reduction modes the sequencer is active, allowing automatic emergency deactivation in the event of card take-off, hardware problems, or supply drop-out.

The TDA8005 is set into Power-down or Sleep mode by software. There are several ways to return to normal mode, Introduction or extraction of the card, detection of a change on P1 (which can be a key pressed) or a command from the system microcontroller. For example, if the system monitors the clock on XTAL1, it may stop this clock after setting the device into power-down mode and then wake it up when sending the clock again. In this situation, the internal clock should have been chosen before the f_{clk}.

Peripheral interface

This block allows synchronous serial communication with the three peripherals (ISO UART, CLOCK CIRCUITRY and OUTPUT PORTS EXTENSION).

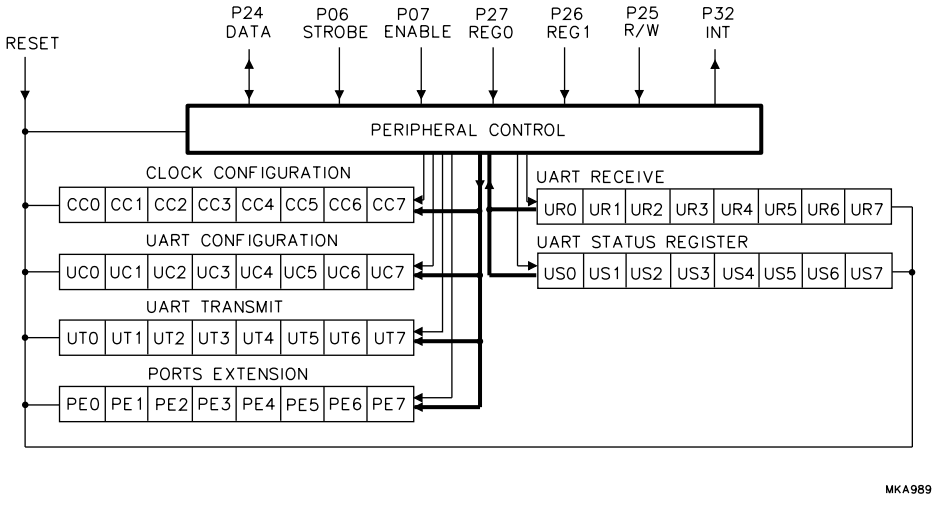


Fig.5 Peripheral interface diagram.

Table 2 Description of Figure 5

BIT NAME	DESCRIPTION
REG0 = 0, REG1 = 0, R/W = 0; CLOCK CONFIGURATION (Configuration after reset is cards clock STOP LOW, $f_{clk} = \frac{1}{8}f_{INT}$)	
CC0	cards clock = $\frac{1}{2}f_{xtal}$
CC1	cards clock = $\frac{1}{4}f_{xtal}$
CC2	cards clock = $\frac{1}{8}f_{xtal}$
CC3	cards clock = $\frac{1}{2}f_{INT}$
CC4	cards clock = STOP HIGH
CC5	$f_{clk} = \frac{1}{2}f_{xtal}$
CC6	$f_{clk} = \frac{1}{4}f_{xtal}$
CC7	$f_{clk} = \frac{1}{2}f_{INT}$
REG0 = 1, REG1 = 0, R/W = 0; UART CONFIGURATION (after reset all bits are cleared)	
UC0	ISO UART RESET
UC1	START SESSION
UC2	LCT (Last Character to Transmit)
UC3	TRANSMIT/RECEIVE
UC4 to UC7	not used
REG0 = 0, REG1 = 1, R/W = 0; UART TRANSMIT	
UT0 to UT7	LSB to MSB of the character to be transmitted to the card
REG0 = 1, REG1 = 1, R/W = 0; PORTS EXTENSION (after reset all bits are cleared)	
PE0 to PE5	PE0 to PE5 is the inverse of the value to be written on K0 to K5
PE6, PE7	not used
REG0 = 0, REG1 = 0, R/W = 1; UART RECEIVE	
UR0 to UR7	LSB to MSB of the character received from the card
REG0 = 1, REG1 = 0, R/W = 1; UART STATUS REGISTER (after reset all bits are cleared)	
US0	UART TRANSMIT buffer empty
US1	UART RECEIVE buffer full
US2	first start bit detected
US3	parity error detected during reception of a character (the UART has asked the card to repeat the character)
US4	parity error detected during transmission of a character. The controller must write the previous character in UART TRANSMIT, or abort the session.
US5 to US7	not used

USE OF PERIPHERAL INTERFACE

Write operation

Select the correct register with R/W, REG0, REG1.

Write the word in the peripheral shift register (PSR) with DATA and STROBE. DATA is shifted on the rising edge of STROBE. 8 shifts are necessary.

Give a negative pulse on ENABLE. The data is parallel loaded in the register on the falling edge of ENABLE.

Read operation

Select the correct register with R/W, REG0 and REG1.

Give a first negative pulse on ENABLE. The word is parallel loaded in the peripheral shift register on the rising edge of ENABLE.

Give a second negative pulse on ENABLE for configuring the PSR in shift right mode.

Read the word from PSR with DATA and STROBE. DATA is shifted on the rising edge of STROBE. 7 shifts are necessary.

Table 3 Example of peripheral interface

CHANGE OF CLOCK CONFIGURATION(1)		**READ CHARACTER ARRIVED IN UART RECEIVE**(2)	
	CLR REG0		CLR REG0
	CLR REG1		CLR REG1
	CLR R/W		SET R/W
	MOV R2, #8		CLR ENABLE
LOOP	RRC A		SET ENABLE
	MOV DATA C		CLR ENABLE
	CLR STROBE		SET ENABLE
	SET STROBE		MOV R2, #8
	DJNZ R2, LOOP	LOOP	MOV C, DATA
	CLR ENABLE		RRC A
	SET ENABLE		CLR STROBE
	SET DATA		SET STROBE
	RET		DJNZ R2, LOOP
			SET DATA
			RET

Notes

1. The new configuration is supposed to be in the accumulator.
2. The character will be in the accumulator.

ISO UART

The ISO UART handles all the specific requirements defined in ISO T = 0 protocol type. It is clocked with the cards clock, which gives the $f_{clk}/31$ sampling rate for start bit detection (the start bit is detected at the first LOW level on I/O) and the $f_{clk}/372$ frequency for ETU timing (in the reception mode the bit is sampled at $\frac{1}{2}$ETU). It also allows the cards clock frequency changes without interfering with the baud rate.

This hardware UART allows operating of the microcontroller at low frequency, thus lowering EM radiations and power consumption. It also frees the microcontroller of fastidious conversions and real time jobs thereby allowing the control of higher level tasks.

The following occurs in the reception mode (see Fig.6):

- Detection of the inverse or direct convention at the begin of ATR.
- Automatic convention setting, so the microcontroller only receives characters in direct convention.
- Parity checking and automatic request for character repetition in case of error (reception is possible at 12 ETU).

In the transmission mode (see Fig.7):

- Transmission according to the convention detected during ATR, consequently the microcontroller only has to send characters in direct convention. Transmission of the next character may start at 12 ETU in the event of no error or 13 ETU in case of error.
- Parity calculation and detection of repetition request from the card in the event of error.
- The bit LCT (Last Character to Transmit) allows fast reconfiguration for receiving the answer 12 ETU after the start bit of the last transmitted character.

The ISO UART status register can inform which event has caused an interrupt. (Buffer full, buffer empty, parity error detected etc.) cf Peripheral Interface.

This register is reset when the microcontroller reads the status out of it.

The ISO UART configuration register enables the microcontroller to configure the ISO UART. cf Peripheral Interface.

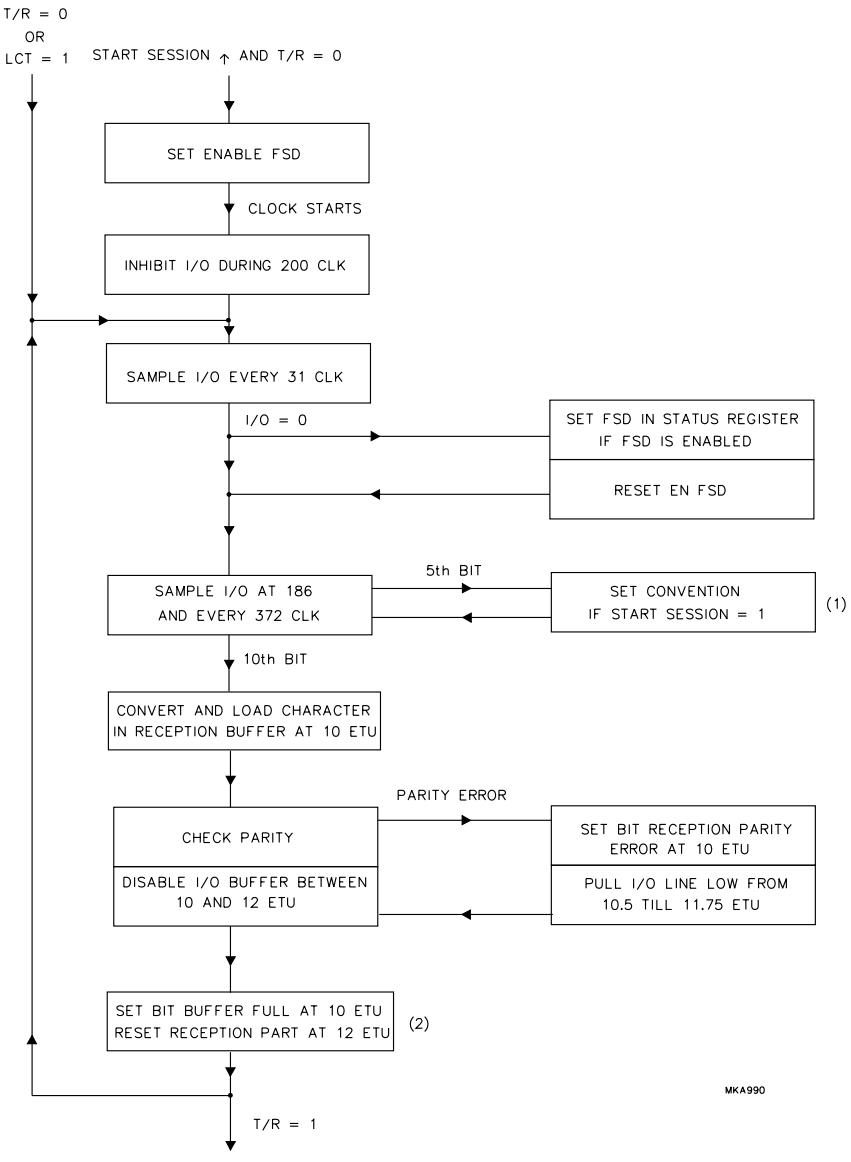
After power-on, all ISO UART registers are reset.

The ISO UART is configured in the reception mode. When the microcontroller wants to start a session, it sets the bits START SESSION and RESET ISO UART in UART CONFIGURATION and then sets START LOW. When the first start bit on I/O is detected (sampling rate $f_{clk}/31$), the UART sets the bit US2 (First Start Detect) in the status register which gives an interrupt on INT0 one CLK pulse later.

The convention is recognized on the first character of the ATR and the UART configures itself in order to exchange direct data without parity processing with the microcontroller whatever the convention of the card is. The bit START SESSION must be reset by software. At the end of every character, the UART tests the parity and resets what is necessary for receiving another character.

If no parity error is detected, the UART sets the bit US1 (BUFFER FULL) in the STATUS REGISTER which warns the microcontroller it has to read the character before the reception of the next one has been completed. The STATUS REGISTER is reset when read from the controller.

If a parity error has been detected, the UART pulls the I/O line LOW between 10.5 and 12 ETU. It also sets the bits BUFFER FULL and US3 (parity error during reception) in the STATUS REGISTER which warns the microcontroller that an error has occurred. The card is supposed to repeat the previous character.



(1) The start session is reset by software.

(2) The software may load the received character in the peripheral control at any time without any action on the ISO UART.

Fig.6 ISO UART reception flow chart.

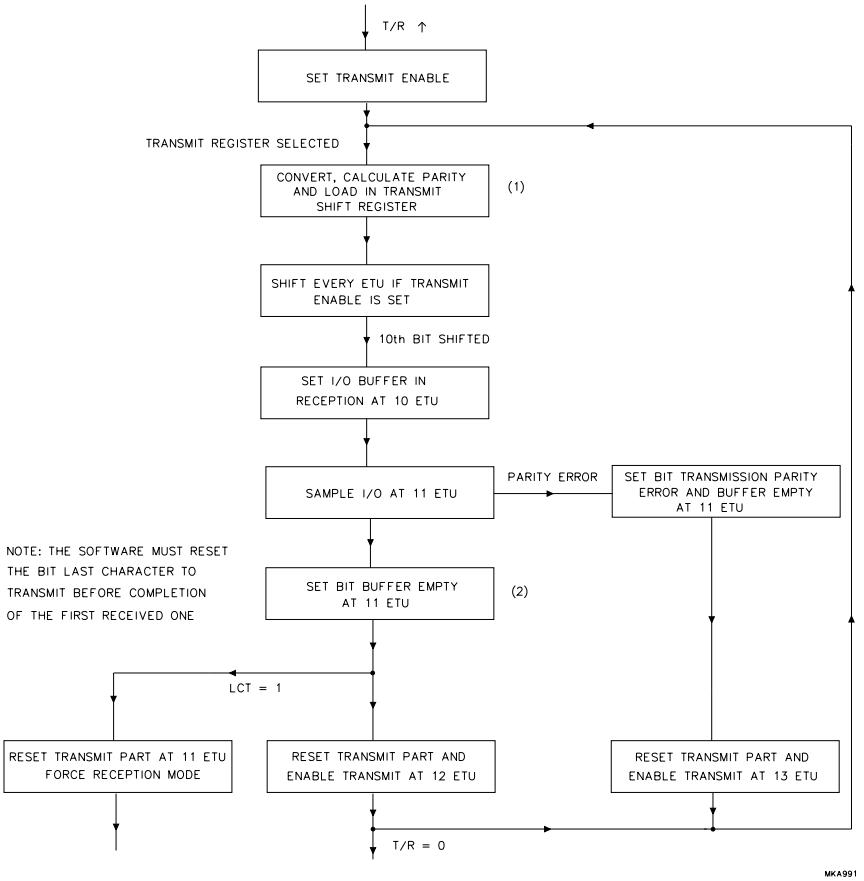
When the controller needs to transmit data to the card, it first sets the bit UC3 in the UART CONFIGURATION which configures the UART in the transmission mode. As soon as a character has been written in the UART TRANSMIT register, the UART makes the conversion, calculates the parity and starts the transmission on the rising edge of ENABLE. When the character has been transmitted, it surveys the I/O line at 11 ETU in order to know if an error has been detected by the card.

If no error has occurred, the UART sets the bit US0 (BUFFER EMPTY) in the STATUS REGISTER and waits for the next character. If the next character has been written before 12 ETU, the transmission will start at 12 ETU. If it was written after 12 ETU it will start on the rising edge of ENABLE.

If an error has occurred, it sets the bits BUFFER EMPTY and US4 (parity error during transmission) which warns the microcontroller to rewrite the previous character in the UART TRANSMIT register. If the character has been rewritten before 13 ETU, the transmission will start at 13 ETU. If it has been written after 13 ETU it will start on the rising edge of ENABLE.

When the transmission is completed, the microcontroller may set the bit LCT (Last Character to Transmit) so that the UART will force the reception mode into ready to get the reply from the card at 12 ETU. This bit must be reset before the end of the first reception. The bit T/R must be reset to enable the reception of the following characters.

When the session is completed, the microcontroller reinitializes the whole UART by resetting the bit RESET ISO UART.



(1) The transmit register may be loaded just after reading from the status register.

(2) The software must reset the last character but before completion of the first received character.

Fig.7 ISO UART transmission flow chart.

I/O buffer modes (see Fig.8)

The following are the I/O buffer modes:

1. I/O buffer disabled by ENIO.
2. I/O buffer in input, 20 kΩ pull-up resister connected between I/O and V_{CC}, I/O masked till 200 clock pulses.
3. I/O buffer in input, 20 kΩ pull-up resister connected between I/O and V_{CC}, I/O is sampled every 31 clock pulses.
4. I/O buffer in output, 20 kΩ pull-up resister connected between I/O and V_{CC}.
5. I/O buffer in output, I/O is pulled LOW by the N transistor of the buffer.
6. I/O buffer in output, I/O is strongly HIGH or LOW by the P or N transistor.

Output ports extension

In the LQFP64 version, 6 auxiliary output ports may be used for low frequency tasks (for example, keyboard scanning). These ports are push-pull output types (cf use in software document).

Activation sequence

When the card is inactive, V_{CC}, CLK, RST and I/O are LOW, with low impedance with respect to GND. The step-up converter is stopped. The I/O is configured in the reception mode with a high impedance path to the ISO UART, subsequently no spurious pulse from the card during power-up will be taken into account until I/O is enabled. When everything is satisfactory (voltage supply, card present, no hardware problems), the microcontroller may initiate an activation sequence by setting START LOW (t_0):

- The step-up converter is started (t_1)
- LIS signal is disabled by ENLI, and V_{CC} starts rising from 0 to 5 V with a controlled rise time of 0.1 V/µs typically (t_2)
- I/O buffer is enabled (t_3)
- Clock is sent to the card (t_4)
- RST buffer is enabled (t_5).

In order to allow a precise count of clock pulses during ATR, a defined time window (t_3; t_5) is opened where the clock may be sent to the card by means of RSTIN. Beyond this window, RSTIN has no more action on clock, and only monitors the cards RST contact (RST is the inverse of RSTIN).

The sequencer is clocked by $f_{INT}/64$ which leads to a time interval T of 25 µs typical. Thus $t_1 = 0$ to $\frac{1}{64}T$, $t_2 = t_1 + \frac{1}{2}3T$, $t_3 = t_1 + 4T$, $t_4 = t_3$ to t_5 and $t_5 = t_1 + 7T$ (see Fig.9).

Deactivation sequence (see Fig.10)

When the session is completed, the microcontroller sets START HIGH. The circuit then executes an automatic deactivation sequence:

- Card reset (RST falls LOW) at t_{10}
- Clock is stopped at t_{11}
- I/O becomes high impedance to the ISO UART (t_{12})
- V_{CC} falls to 0 V with typical 0.1 V/µs slew rate (t_{13})
- The step-up converter is stopped and CLK, RST, V_{CC} and I/O become low impedance to GND (t_{14}).
- $t_{10} < \frac{1}{64}T$; $t_{11} = t_{10} + \frac{1}{2}T$; $t_{12} = t_{10} + T$; $t_{13} = t_{10} + \frac{1}{2}3T$; $t_{14} = t_{10} + 5T$.

Protections

Main hardware fault conditions are monitored by the circuit

- Overcurrent on V_{CC}
- Short circuits between V_{CC} and other contacts
- Card take-off during transaction.

When one of these problems is detected, the security logic block pulls the interrupt line OFF LOW, in order to warn the microcontroller, and initiates an automatic deactivation of the contacts. When the deactivation has been completed, the OFF line returns HIGH, except if the problem was due to a card extraction in which case it remains LOW till a card is inserted.

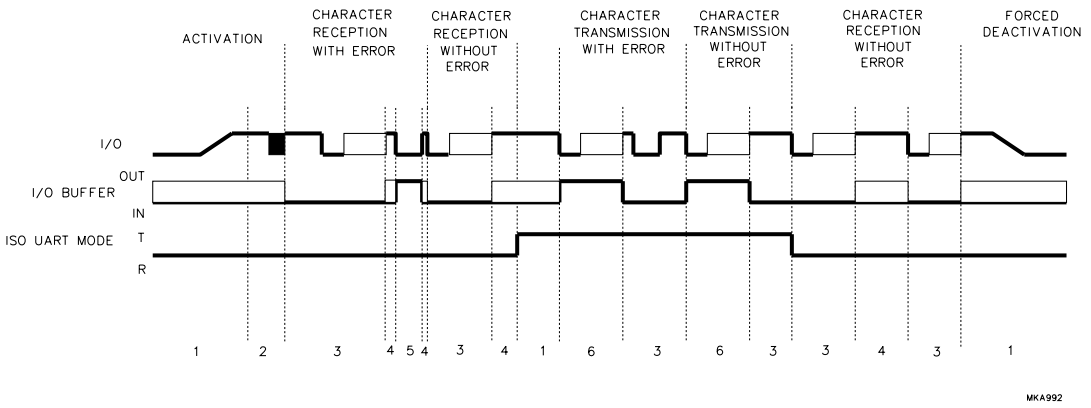


Fig.8 I/O buffer modes.

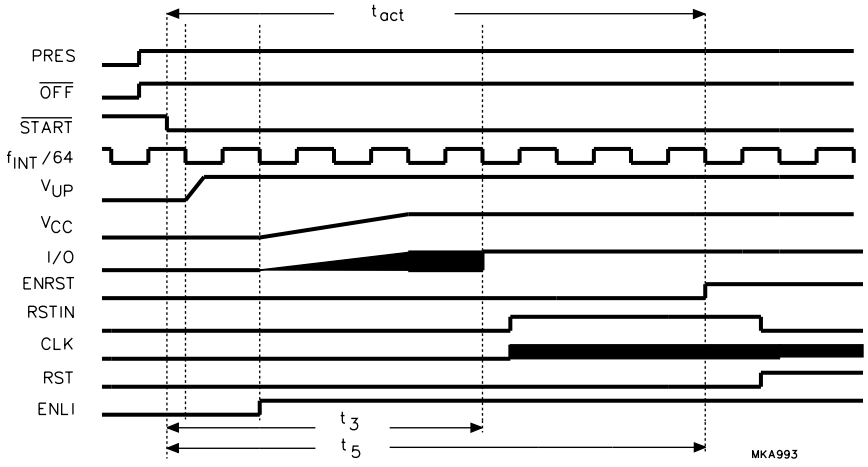


Fig.9 Activation sequence.

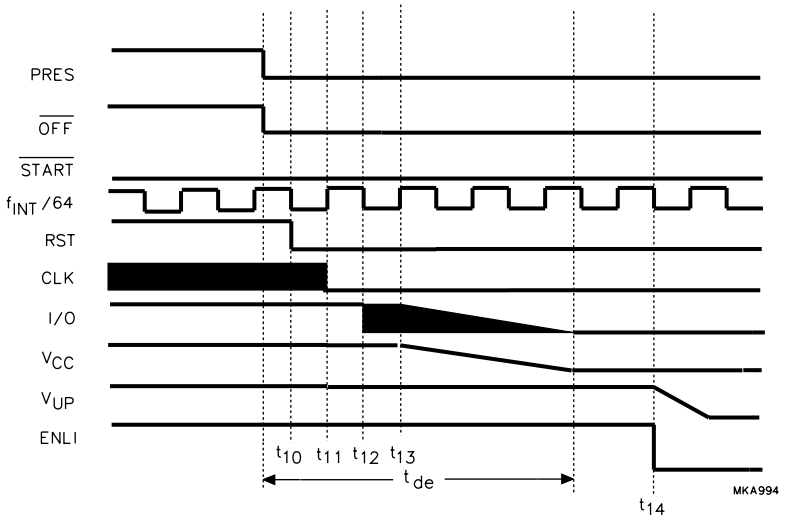


Fig.10 Emergency deactivation sequence after a card take-off.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage		–0.5	6.5	V
V_{DDD}	digital supply voltage		–0.5	6.5	V
V_n	all input voltages		–0.5	V_{DD} + 0.5	V
I_{n1}	DC current into XTAL1, XTAL2, RX, TX, RESET, INT1, P34, P37, P00 to P03, P11 to P17, P20 to P23 and TEST1 to TEST4		–	5	mA
I_{n2}	DC current from or to AUX1, AUX2		–10	+10	mA
I_{n3}	DC current from or to S1 to S5		tbf	tbf	mA
I_{n4}	DC current into DELAY		–	tbf	mA
I_{n5}	DC current from or to PRES		tbf	tbf	mA
I_{n6}	DC current from and to K0 to K5		–5	+5	mA
I_{n7}	DC current from or into ALARM (according to option choice)		–5	+5	mA
P_{tot}	continuous total power dissipation	T_{amb} = –20 to +85°C	–	500	mW
T_{stg}	IC storage temperature		–55	+150	°C
V_{es}	electrostatic discharge	on pins I/O, V_{CC}, RST, CLK and PRES	–6	+6	kV
		on other pins	–2	+2	kV

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air		
	LQFP64	70	K/W
	QFP44	60	K/W

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; for general purpose I/O ports see 80CL51 data sheet; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5	–	6.0	V
$I_{DD(pd)}$	supply current power-down mode	V_{DD} = 5 V; card inactive	tbf	90	tbf	µA
$I_{DD(sm)}$	supply current sleep mode	card powered, but with clock stopped	tbf	500	tbf	µA
$I_{DD(om)}$	supply current operating mode	unloaded; f_{xtal} = 13 MHz; f_{clk} = 6.5 MHz; f_{card} = 3.25 MHz	tbf	5.5	tbf	mA
		V_{DD} = 3 V; f_{xtal} = 13 MHz; f_{clk} = 3.25 MHz; f_{card} = 3.25 MHz	tbf	3	tbf	mA
V_{th1}	threshold voltage on V_{DD} (falling)		2	–	2.3	V
V_{hys1}	hysteresis on V_{th1}		50	–	200	mV
V_{th2}	threshold voltage on DELAY		–	1.38	–	V
V_{DEL}	voltage on pin DELAY		–	–	V_{DD}	V
I_{DEL}	output current at DELAY	pin grounded (charge)	–	–1	–	µA
		V_{DEL} = V_{DD} (discharge)	–	2	–	mA
t_W	ALARM pulse width	C_{DEL} = 10 nF	–	10	–	ms
ALARM (open drain active HIGH or LOW output)						
I_{OH}	HIGH level output current	active LOW option; V_{OH} = 5 V	–	–	10	µA
V_{OL}	LOW level output voltage	active LOW option; I_{OL} = 2 mA	–	–	0.4	V
I_{OL}	LOW level output current	active HIGH option, V_{OL} = 0 V	–	–	–10	µA
V_{OH}	HIGH level output voltage	active HIGH option, I_{OH} = –2 mA	V_{DD} – 1	–	–	V
Crystal oscillator (note 1)						
f_{xtal}	crystal frequency		2	–	16	MHz
f_{EXT}	external frequency applied on XTAL1		0	–	16	MHz
Step-up converter						
f_{INT}	oscillation frequency		2	–	3	MHz
V_{UP}	voltage on S5		–	6.0	–	V
Low impedance supply (LIS)						
V_{LIS}	voltage on LIS		0	–	V_{DD}	V
I_{LIS}	current at LIS		–	–	5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset output to the card (RST)						
$V_{inactive}$	output voltage	when inactive	–0.3	–	0.4	V
		when LIS is used; $I_{inactive}$ = 1 mA	–0.3	–	0.4	V
$I_{inactive}$	current from RST when inactive and pin grounded		–	–	–1	mA
V_{OL}	LOW level output voltage	I_{OL} = 200 μA	–0.3	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} <–200 μA	4	–	V_{CC} + 0.3	V
		I_{OH} = –20 μA	V_{CC} – 0.7	–	V_{CC} + 0.3	V
t_r	rise time	C_L = 30 pF	–	–	1	μs
t_f	fall time	C_L = 30 pF	–	–	1	μs
Clock output to the card (CLK)						
$V_{inactive}$	output voltage	when inactive	–0.3	–	0.4	V
		when LIS is used; $I_{inactive}$ = 1 mA	–0.3	–	0.4	V
$I_{inactive}$	current from RST when inactive and pin grounded		–	–	–1	mA
V_{OL}	LOW level output voltage	I_{OL} = 200 μA	–0.3	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –200 μA	2.4	–	V_{CC} + 0.3	V
		I_{OH} = –20 μA	0.7V_{CC}	–	V_{CC} + 0.3	V
		I_{OH} = –10 μA	V_{CC} – 0.7	–	V_{CC} + 0.3	V
t_r	rise time	C_L = 30 pF	–	–	10	ns
t_f	fall time	C_L = 30 pF	–	–	10	ns
f_{clk}	clock frequency	1 MHz Idle configuration	1	–	1.5	MHz
		low operating speed	–	–	2	MHz
		middle operating speed	–	–	4	MHz
		high operating speed	–	–	8	MHz
δ	duty cycle	C_L = 30 pF	45	–	55	%
Card supply voltage (V_{CC})						
$V_{inactive}$	output voltage	when inactive	–	–	0.4	V
		when LIS is used; $I_{inactive}$ = 1 mA	–	–	0.4	V
$I_{inactive}$	current from RST when inactive and pin grounded		–	–	–1	mA
V_o	output voltage in active mode with 100 nF capacitor; including static load (up to 20 mA) and dynamic current of 40 nA	I_{max} = 200 mA, f_{max} = 5 MHz, and duration <400 ns	4.75	–	5.25	V
I_{CC}	output current	V_{CC} = 5V	–	–	–20	mA
		V_{CC} shorted to GND	–	–	–40	mA
SR	slew rate	up or down (max capacitance is 150 nF)	–	0.1	–	V/μs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data line (I/O)						
$V_{inactive}$	output voltage	when inactive	–	–	0.4	V
		when LIS is used; $I_{inactive}$ = 1 mA	–	–	0.4	V
$I_{inactive}$	current from RST when inactive and pin grounded		–	–	–1	mA
V_{OL}	LOW level output voltage (I/O configured as an output)	I_{OL} = 1 mA	–0.3	–	0.4	V
V_{OH}	HIGH level output voltage (I/O configured as an output)	I_{OH} <–100 μA	3.8	–	V_{CC} + 0.3	V
V_{IL}	input voltage LOW (I/O configured as an input)	I_{IL} = 1 mA	–0.3	–	0.8	V
V_{IH}	input voltage HIGH (I/O configured as an input)	I_{IL} = 100 μA	2	–	V_{CC}	V
t_r	rise time	C_L = 30 pF	–	–	1	μs
t_f	fall time	C_L = 30 pF	–	–	1	μs
R_{pu}	pull-up resistor connected to V_{CC} when I/O is input	see Table 4 for options	–	–	–	
Protections						
$I_{CC(sd)}$	shutdown current at V_{CC}		–	–30	–	mA
Timing						
t_{act}	activation sequence duration		–	–	225	μs
t_{de}	deactivation sequence duration		–	–	150	μs
$t_{3(start)}$	start of the window for sending clock to the card		–	–	130	μs
$t_{3(end)}$	end of the window for sending clock to the card		140	–	–	μs
Auxiliary outputs (AUX1, AUX2)						
V_{OL}	LOW level output voltage	I_{OL} = 5 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –5 mA	V_{DD} – 1	–	–	V
Output ports from extension (K0 to Kn)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –2 mA	V_{DD} – 1	–	–	V
Card presence input (PRES)						
V_{IL}	LOW level input voltage	I_{IL} = –1 mA	–	–	0.6	V
V_{IH}	HIGH level input voltage	I_{IH} = 100 μA	$0.7V_{DD}$	–	–	V

Note

1. The crystal oscillator is the same as OPTION 3 of the 80CL51.

APPLICATION INFORMATION

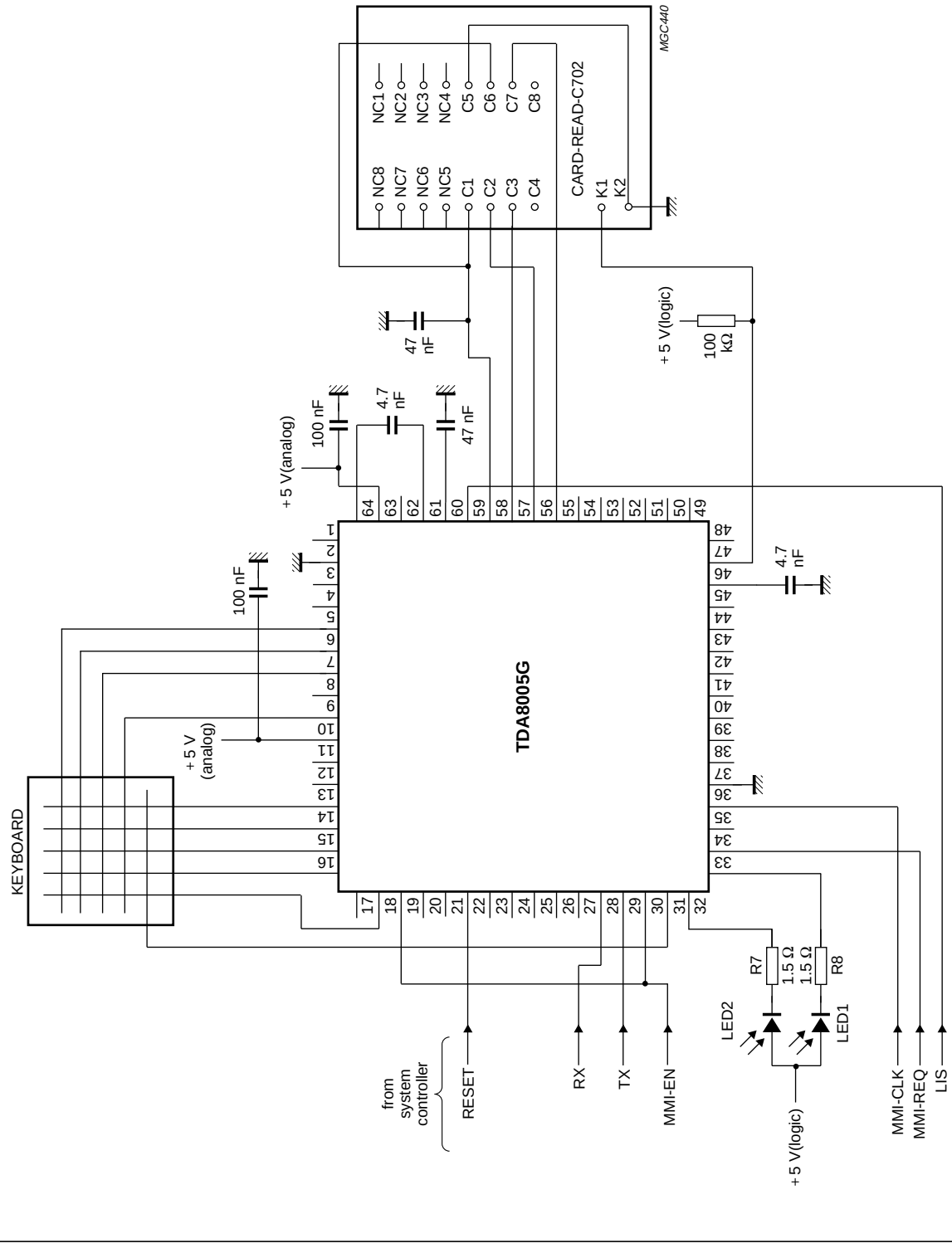


Fig.11 Possible GSM application.

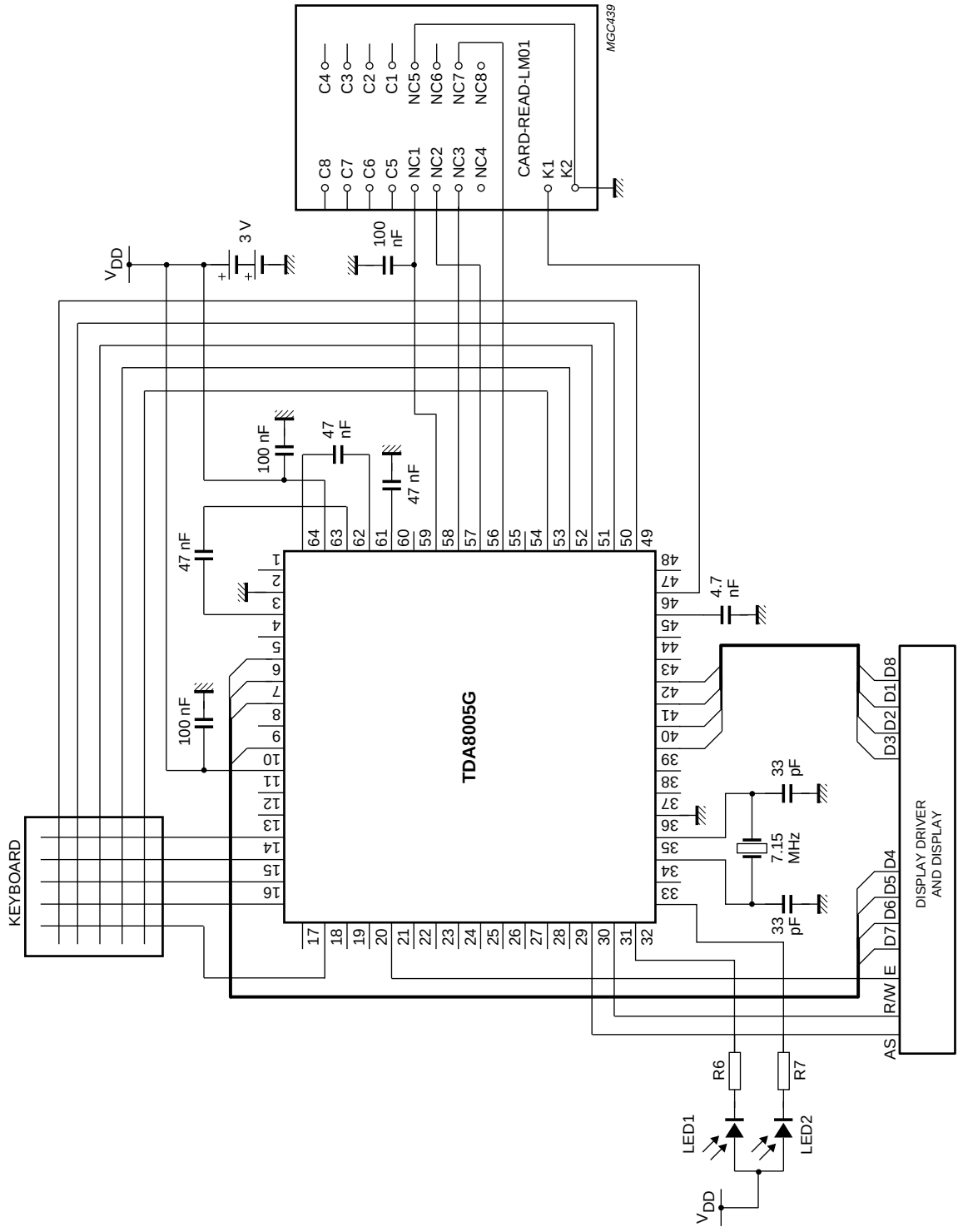


Fig.12 Possible stand-alone application.

Table 4 TDA8005 option choice form

FUNCTION	DESCRIPTION	OPTION
Ports		
P00		
P01		
P02		
P03		
P04	RSTIN (fixed)	3 S
P05	START (fixed)	3 S
P06	STR (fixed)	3 S
P07	EN (fixed)	3 S
P10	OFF (fixed)	2 S
P11		
P12		
P13		
P14		
P15		
P16		
P17		
P20		
P21		
P22		
P23		
P24	DATA (fixed)	1 S
P25	R/W (fixed)	3 S
P26	REG1 (fixed)	3 S
P27	REG0 (fixed)	3 S
P30		
P31		
P32	INT (fixed)	1 S
P33		
P34		
P35	AUXI (fixed)	3 S
P36	AUX2 (fixed)	3 S
P37		

FUNCTION	DESCRIPTION	OPTION
Analog options		
Step-up	doubler (updo) or tripler (uptri)	
Supervisor	2.3 (supervb, 3 (supervtr) or 4.5 (supercl)	
I/O	low impedance (UARTl) or high impedance (UARTh)	
I/O pull-up	10, 20 or 30 kΩ	
R_CLK	0, 100, 150 or 200 Ω	
R_RST	0, 80, 130 or 180 Ω	
ALARM	active HIGH (alarmbufp) or active LOW (alarmbufn)	
PRES	active HIGH (prestopp) or active LOW (prestopn)	