DATA SHEET

TDA6402; TDA6403

5 V mixer/oscillator and synthesizer for cable TV and VCR 2-band tuners

Preliminary specification
File under Integrated Circuits, IC02

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Semiconductors

PHILIPS

5 V mixer/oscillator and synthesizer for cable TV and VCR 2-band tuners

TDA6402; TDA6403

FEATURES

- Single-chip 5 V mixer/oscillator and synthesizer for cable TV and VCR tuners
- Synthesizer function compatible with existing TSA5526
- Universal bus protocol (I^2C-bus or 3-wire bus)
  - bus protocol for 18 or 19-bit transmission (3-wire bus)
  - extra protocol for 27-bit transmission (test modes and features for 3-wire bus)
  - address + 4 data bytes transmission (I^2C-bus WRITE mode)
  - address + 1 status byte (I^2C-bus READ mode)
  - 4 independent I^2C-bus addresses
- 1 PNP buffer for UHF band selection (25 mA)
- 3 PNP buffers for general purpose, e.g. 2 VHF sub-bands, FM sound trap (25 mA)
- 33 V tuning voltage output
- In-lock detector
- 5-step A/D converter (3 bits in I^2C-bus mode)
- 15-bit programmable divider
- Programmable reference divider ratio (512, 640 or 1024)
- Programmable charge pump current (60 or 280 μA)
- Programmable automatic charge pump current switch
- Varicap drive disable
- Mixer/oscillator function compatible with existing TDA5732
- Balanced mixer with a common emitter input for VHF (single input)
- Balanced mixer with a common base input for UHF (balanced input)
- 2-pin common emitter oscillator for VHF
- 4-pin common emitter oscillator for UHF
- IF preamplifier with asymmetrical 75 Ω output impedance to drive a low-ohmic impedance (75 Ω)
- Low power
- Low radiation
- Small size.

APPLICATIONS

- Cable tuners for TV and VCR (switched concept for VHF)
- Recommended RF bands for the USA: 55.25 to 133.25 MHz, 139.25 to 361.25 MHz and 367.25 to 801.25 MHz.

GENERAL DESCRIPTION

The TDA6402 and TDA6403 are programmable 2-band mixer/oscillators and synthesizers intended for VHF/UHF cable tuners (see Fig.1).

The devices include two double balanced mixers and two oscillators for the VHF and UHF band respectively, an IF amplifier and a PLL synthesizer. The VHF band can be split-up into two sub-bands using a proper oscillator application and a switchable inductor. Two pins are available between the mixer output and the IF amplifier input to enable IF filtering for improved signal handling. Four PNP ports are provided. Band selection is provided by using pin PUHF. When PUHF is ‘ON’, the UHF mixer-oscillator is active and the VHF band is switched off. When PUHF is ‘OFF’, the VHF mixer-oscillator is active and the UHF band is ‘OFF’. PVHFL and PVHFH are used to select the VHF sub-bands. FMST is a general purpose port, that can be used to switch an FM sound trap. When it is used, the sum of the collector currents has to be limited to 30 mA.

The synthesizer consists of a divide-by-eight prescaler, a 15-bit programmable divider, a crystal oscillator and its programmable reference divider and a phase/frequency detector combined with a charge-pump which drives the tuning amplifier, including 33 V output.

Depending on the reference divider ratio (512, 640 or 1024), the phase comparator operates at 7.8125 kHz, 6.25 kHz or 3.90625 kHz with a 4 MHz crystal.

The device can be controlled according to the I²C-bus format or 3-wire bus format depending on the voltage applied to pin SW (see Table 2). In the 3-wire bus mode (SW = HIGH), pin LOCK/ADC is the lock output.
The LOCK output is LOW when the PLL loop is locked. In the I²C-bus mode (SW = LOW), the lock detector bit FL is set to logic 1 when the loop is locked and is read on the SDA line (Status Byte) during a READ operation in I²C-bus mode only. The Analog-to-Digital Converter (ADC) input is available on pin LOCK/ADC for digital AFC control in the I²C-bus mode only. The ADC code is read during a READ operation on the I²C-bus (see Table 10). In test mode, pin LOCK/ADC is used as a TEST output for f_{REF} and $\frac{1}{2}f_{DIV}$, in both I²C-bus mode and 3-wire bus mode (see Table 6).

When the automatic charge-pump current switch mode is activated and when the loop is phase-locked, the charge-pump current value is automatically switched to LOW. This action is taken to improve the carrier-to-noise ratio. The status of this feature can be read in the ACPS flag during a read operation on the I²C-bus (see Table 8).

I²C-bus format (SW = GND)

Five serial bytes (including address byte) are required to address the device, select the VCO frequency, program the four ports, set the charge-pump current and set the reference divider ratio. The device has four independent I²C-bus addresses which can be selected by applying a specific voltage on input CE (see Table 5).

3-wire bus format (SW = V_{CC} or OPEN)

Data is transmitted to the devices during a HIGH-level on input CE (enable line). The device is compatible with 18-bit and 19-bit data formats, as shown in Figs 4 and 5. The first four bits are used to program the PNP ports and the remaining bits control the programmable divider. A 27-bit data format may also be used to set the charge-pump current, the reference divider ratio and for test purposes (see Fig.6).

It is not allowed to address the devices with words whose length is different from 18, 19 or 27 bits.

Table 1 Data word length for 3-wire bus

TYPE NUMBER	DATA WORD	REFERENCE DIVIDER(1)	FREQUENCY STEP
TDA6402; TDA6403	18-bit	512	62.50 kHz
TDA6402; TDA6403	19-bit	1024	31.25 kHz
TDA6402; TDA6403	27-bit	programmable	programmable

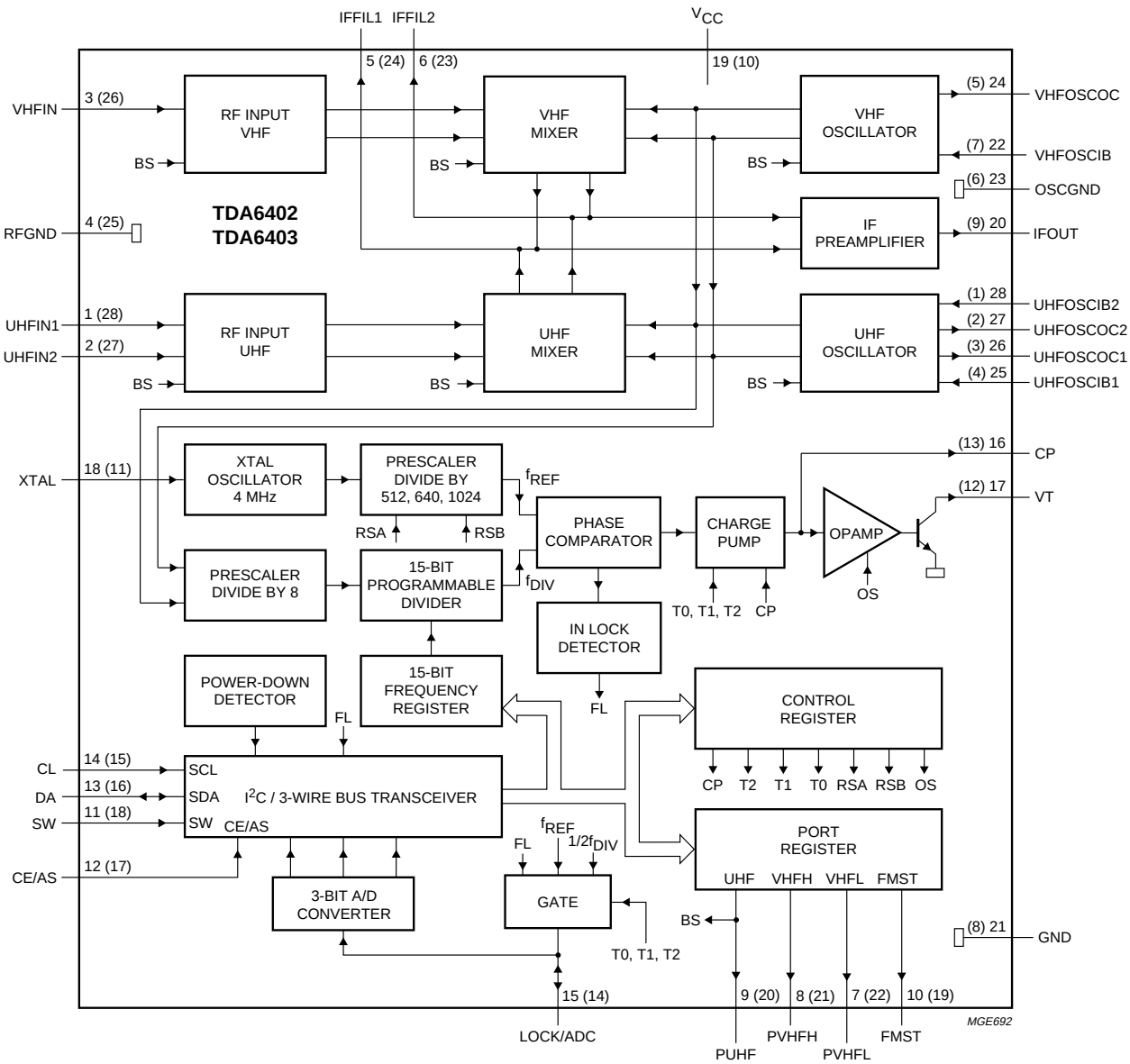
Note

1. The selection of the reference divider is given by an automatic identification of the data word length. When the 27-bit format is used, the reference divider is controlled by RSA and RSB bits (see Table 7). More details are given in Chapter “PLL functional description”, Section “3-wire bus mode (SW = OPEN or V_{CC})”.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6402M	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1
TDA6403M	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

BLOCK DIAGRAM



The pin numbers in parenthesis represent the TDA6403.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	TDA6402	TDA6403	
UHFIN1	1	28	UHF RF input 1
UHFIN2	2	27	UHF RF input 2
VHFIN	3	26	VHF RF input
RFGND	4	25	RF ground
IFFIL1	5	24	IF filter output 1
IFFIL2	6	23	IF filter output 2
PVHFL	7	22	PNP port output, general purpose (e.g. VHF low sub-band)
PVHFH	8	21	PNP port output, general purpose (e.g. VHF high sub-band)
PUHF	9	20	PNP port output, UHF band
FMST	10	19	PNP port output, general purpose (e.g. FM sound trap)
SW	11	18	bus format selection input (I^2C-bus/3-wire bus)
CE/AS	12	17	chip Enable/Address Selection input
DA	13	16	serial data input/output
CL	14	15	serial clock input
LOCK/ADC	15	14	lock detector output (3-wire bus)/ADC input (I^2C-bus)
CP	16	13	charge pump output
VT	17	12	tuning voltage output
XTAL	18	11	crystal oscillator input
V_{CC}	19	10	supply voltage
IFOUT	20	9	IF output
GND	21	8	digital ground
VHFOSCIB	22	7	VHF oscillator input base
OSCGND	23	6	oscillator ground
VHFOSCOC	24	5	VHF oscillator output collector
UHFOSCIB1	25	4	UHF oscillator input base 1
UHFOSCOC1	26	3	UHF oscillator output collector 1
UHFOSCOC2	27	2	UHF oscillator output collector 2
UHFOSCIB2	28	1	UHF oscillator input base 2

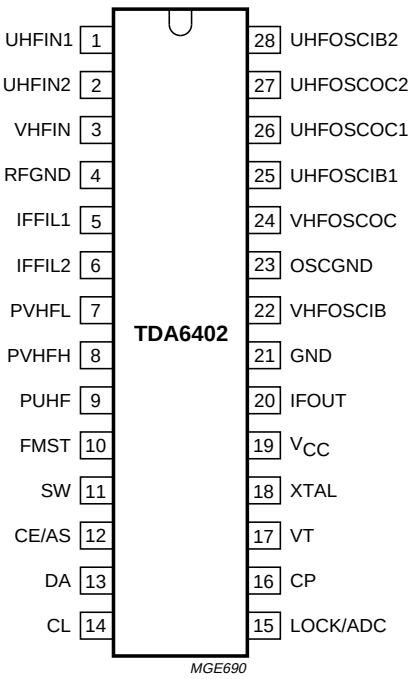


Fig.2 Pin configuration for TDA6402.

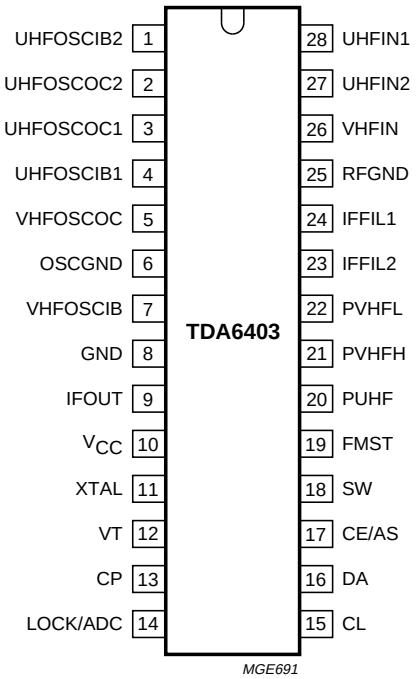


Fig.3 Pin configuration for TDA6403.

PLL FUNCTIONAL DESCRIPTION

The device is controlled via the I²C-bus or the 3-wire bus, depending on the voltage applied on the SW input. A HIGH level on the SW input enables the 3-wire bus; CE/AS, DA and CL inputs are used as ENABLE (CE), DATA and CLOCK inputs respectively. A LOW level on SW input enables the I²C-bus; the CE/AS, DA and CL inputs are used as address selection (AS), SDA and SCL input respectively (see Table 2).

Table 2 Bus format selection

SYMBOL	PIN		3-WIRE BUS MODE	I²C-BUS MODE
	TDA6402	TDA6403		
SW	11	18	HIGH level or OPEN	LOW level or GND
CE/AS	12	17	ENABLE input	Address selection input
DA	13	16	DATA input	SDA input
CL	14	15	CLOCK input	SCL input
LOCK/ADC	15	14	LOCK/TEST output	ADC input/TEST output

I²C-bus mode (SW = GND)

WRITE MODE; R/W = 0 (see Table 3)

Data bytes can be sent to the device after the address transmission (first byte). Four data bytes are needed to fully program the device. The bus transceiver has an auto-increment facility which permits the programming of the device within one single transmission (address + 4 data bytes).

The device can also be partially programmed providing that the first data byte following the address is divider byte 1 (DB1) or control byte (CB). The bits in the data bytes are defined in Table 3. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or control and band-switch data (first bit = 1) will follow. Until an I²C-bus STOP command is sent by the controller, additional data bytes can be entered without the need to re-address the device. The frequency register is loaded after the 8th clock pulse of the second divider byte (DB2), the control register is loaded after the 8th clock pulse of the control byte (CB) and the band-switch register is loaded after the 8th clock pulse of the band switch byte (BB).

I²C-BUS ADDRESS SELECTION

The module address contains programmable address bits (MA1 and MA0) which offer the possibility of having several synthesizers (up to 4) in one system by applying a specific voltage on the CE input. The relationship between MA1 and MA0 and the input voltage applied to the CE input is given in Table 5.

Table 3 I²C-bus data format, write mode

NAME	BYTE	BITS								ACK
		MSB							LSB	
Address byte	ADB	1	1	0	0	0	MA1	MA0	R/W = 0	A
Divider byte 1	DB1	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2	DB2	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte	CB	1	CP	T2	T1	T0	RSA	RSB	OS	A
Band-switch byte	BB	X	X	X	X	FMST	PUHF	PVHFH	PVHFL	A

Table 4 Description of symbols used in Table 3

SYMBOL	DESCRIPTION
A	acknowledge
MA1, MA0	programmable address bits (see Table 5)
N14 to N0	programmable divider bits; $N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2^{1} + N0$
CP	charge pump current CP = 0 = 60 μA CP = 1 = 280 μA (default)
T2, T1, T0	test bits (see Table 6)
RSA, RSB	reference divider ratio select bits (see Table 7)
OS	tuning amplifier control bit: OS = 0; normal operation; tuning voltage is ‘ON’ (default) OS = 1; tuning voltage is ‘OFF’ (high impedance)
PVHFL, PVHFH, PUHF, FMST	PNP ports control bits: bit = 0; buffer n is ‘OFF’ (default) bit = 1; buffer n is ‘ON’
X	don’t care; may be a ‘0’ or a ‘1’

Table 5 Address selection (I^2C-bus mode)

MA1	MA0	VOLTAGE APPLIED ON CE INPUT (SW = GND)
0	0	0 V to $0.1 \times V_{CC}$
0	1	open or $0.2 \times V_{CC}$ to $0.3 \times V_{CC}$
1	0	$0.4 \times V_{CC}$ to $0.6 \times V_{CC}$
1	1	$0.9 \times V_{CC}$ to $1.0 \times V_{CC}$

Table 6 Test modes

T2	T1	T0	TEST MODES
0	0	0	automatic charge-pump switched off
0	0	1	automatic charge-pump switched on (note 1)
0	1	X	charge-pump is 'OFF'
1	1	0	charge-pump is sinking current
1	1	1	charge-pump is sourcing current
1	0	0	f_{REF} is available on pin LOCK/ADC (note 2)
1	0	1	$\frac{1}{2}f_{DIV}$ is available on pin LOCK/ADC (note 2)

Notes

1. This is the default mode at power-on reset.
2. The ADC input cannot be used when these test modes are active; see Section "Read mode; R/W = 1 (see Table 8)" for more information.

Table 7 Reference divider ratio select bits

RSA	RSB	REFERENCE DIVIDER RATIO
X	0	640
0	1	1024
1	1	512

Note

1. X = don't care; may be a '0' or a '1'.

READ MODE; R/W = 1 (see Table 8)

Data can be read from the device by setting the R/W bit to 1. After the slave address has been recognized, the device generates an acknowledge pulse and the first data byte (status byte) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a HIGH-level of the SCL clock signal. A second data byte can be read from the device if the microcontroller generates an acknowledge on the SDA line (master acknowledge). End of transmission will occur if no master acknowledge occurs. The device will then release the data line to allow the microcontroller to generate a STOP condition.
The POR flag is set to 1 at power-on. The flag is reset when an end-of-data is detected by the device (end of a READ sequence). Control of the loop is made possible with the in-lock flag FL which indicates when the loop is locked (FL = 1).

The automatic charge-pump switch flag (ACPS) is LOW when the automatic charge-pump switch mode is 'ON' and the loop is locked. In other conditions, ACPS = 1.
When ACPS = 0, the charge-pump current is forced to the LOW value.

A built-in ADC is available on LOCK/ADC pin (I^2C-bus mode only). This converter can be used to apply AFC information to the microcontroller from the IF section of the television. The relationship between the bits A2, A1 and A0 is given in Table 10.

Table 8 Read data format

NAME	BYTE	BITS								ACK
		MSB(1)							LSB	
Address byte	ADB	1	1	0	0	0	MA1	MA0	R/W = 1	A
Status byte	SB	POR	FL	ACPS	1	1	A2	A1	A0	–

Note

1. MSB is transmitted first.

Table 9 Description of symbols used in Table 8

SYMBOL	DESCRIPTION
A	acknowledge
POR	power-on reset flag (POR = 1 at power-on)
FL	in-lock flag (FL = 1 when the loop is locked)
ACPS	automatic charge-pump switch flag: ACPS = 0; active ACPS = 1; not active
A2, A1, A0	digital outputs of the 5-level ADC

Table 10 A to D converter levels (note 1)

A2	A1	A0	VOLTAGE APPLIED ON ADC INPUT
1	0	0	$0.60 \times V_{CC}$ to $1.00 \times V_{CC}$
0	1	1	$0.45 \times V_{CC}$ to $0.60 \times V_{CC}$
0	1	0	$0.30 \times V_{CC}$ to $0.45 \times V_{CC}$
0	0	1	$0.15 \times V_{CC}$ to $0.30 \times V_{CC}$
0	0	0	0 to $0.15 \times V_{CC}$

Note

1. Accuracy is $\pm 0.03 \times V_{CC}$.

POWER-ON RESET

Table 11 Default bits at power-on reset

NAME	BYTE	BITS							
		MSB							LSB
Address byte	ADB	1	1	0	0	0	MA1	MA0	X
Divider byte 1	DB1	0	X	X	X	X	X	X	X
Divider byte 2	DB2	X	X	X	X	X	X	X	X
Control byte	CB	1	1	0	0	1	X	1	0
Band switch byte	BB	X	X	X	X	0	0	0	0

The power-on detection threshold voltage V_{POR} is set to V_{CC} = 2 V at room temperature. Below this threshold, the device is reset to the power-on state.

At power-on state, the charge-pump current is set to 280 μA, the tuning voltage output is disabled, the test bits T2, T1 and T0 are set to '001' (automatic charge-pump switch 'ON') and RSB is set to 1.

PUHF is 'OFF', which means that the UHF oscillator and the UHF mixer are switched off. Consequently, the VHF oscillator and the VHF mixer are switched on. PVHFL and PVHFH are 'OFF', which means that the VHF tank circuit is working in the VHF I sub-band. The tuning amplifier is switched off until the first transmission. In that case, the tank circuit in VHF I is supplied with the maximum tuning voltage. The oscillator is therefore working at the end of the VHF I sub-band.

3-wire bus mode (SW = OPEN or V_{CC})

During a HIGH-level on the CE input (ENABLE line), the data is clocked into the data register at the HIGH-to-LOW transition of the clock. The first four bits control the PNP ports and are loaded into the internal band switch register on the 5th rising edge of the clock pulse. The frequency bits are loaded into the frequency register at the HIGH-to-LOW transition of the chip enable line when an 18-bit or 19-bit data word is transmitted (see Figs 4 and 5).

When a 27-bit data word is transmitted, the frequency bits are loaded into the frequency register on the 20th rising edge of the clock pulse and the control bits at the HIGH-to-LOW transition of the chip enable line (see Fig.6). In this mode, the reference divider is given by the RSA and RSB bits (see Table 7). The test bits T2, T1 and T0, the charge-pump bit CP, the ratio select bit RSB and the OS bit can only be selected or changed with a 27-bit transmission. They remain programmed if an 18-bit or 19-bit transmission occurs. Only RSA is controlled by the transmission length when the 18-bit or 19-bit format is used. When an 18-bit data word is transmitted, the most significant bit of the divider N14 is internally set to 0 and the bit RSA is set to 1. When a 19-bit data word is transmitted, the bit RSA is set to 0.

A data word of less than 18 bits will not affect the frequency register of the device. The definition of the bits is unchanged compared to I^{2}C-bus mode.

It is not allowed to address the devices with words whose length is different from 18, 19 or 27 bits.

POWER-ON RESET

The power-on detection threshold voltage V_{POR} is set to V_{CC} = 2 V at room temperature. Below this threshold, the device is reset to the power-on state.

At power-on state, the charge-pump current is set to 280 μA, the tuning voltage output is disabled, the test bits T2, T1 and T0 are set to '001' (automatic charge-pump switch 'ON') and RSB is set to 1.

PUHF is 'OFF', which means that the UHF oscillator and the UHF mixer are switched off. Consequently, the VHF oscillator and the VHF mixer are switched on. PVHFL and PVHFH are 'OFF', which means that the VHF tank circuit is working in the VHF I sub-band. The tuning amplifier is switched off until the first transmission. In that case, the tank circuit in VHF I is supplied with the maximum tuning voltage. The oscillator is therefore working at the end of the VHF I sub-band.

If the first sequence transmitted to the device has 18 or 19 bits, the reference divider ratio is set to 512 or 1024, depending on the sequence length.
If the sequence has 27 bits, the reference divider ratio is fixed by RSA and RSB bits (see Table 7).

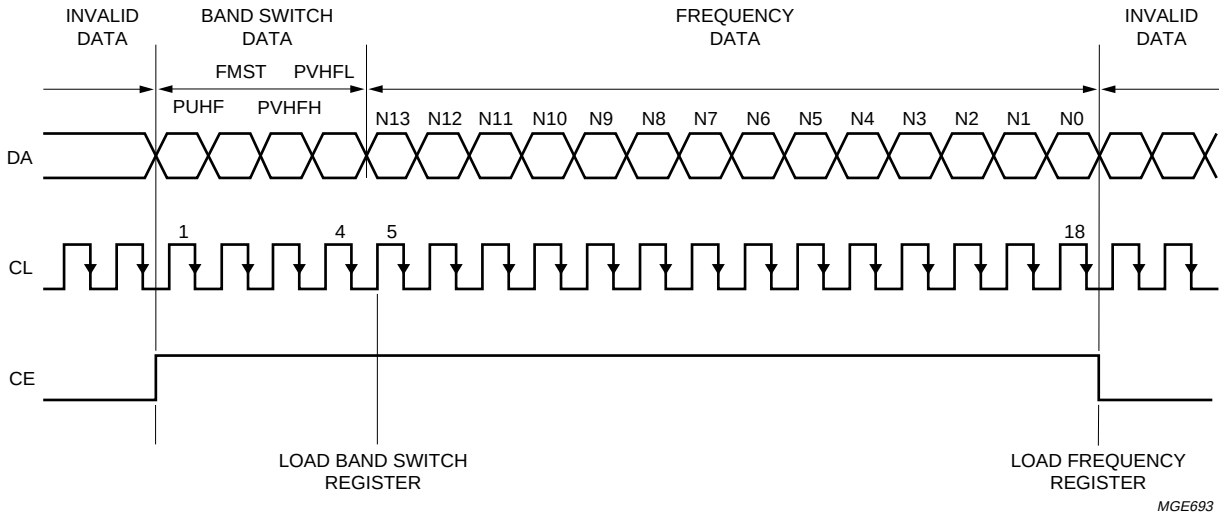


Fig.4 Normal mode; 18-bit data format (RSA = 1).

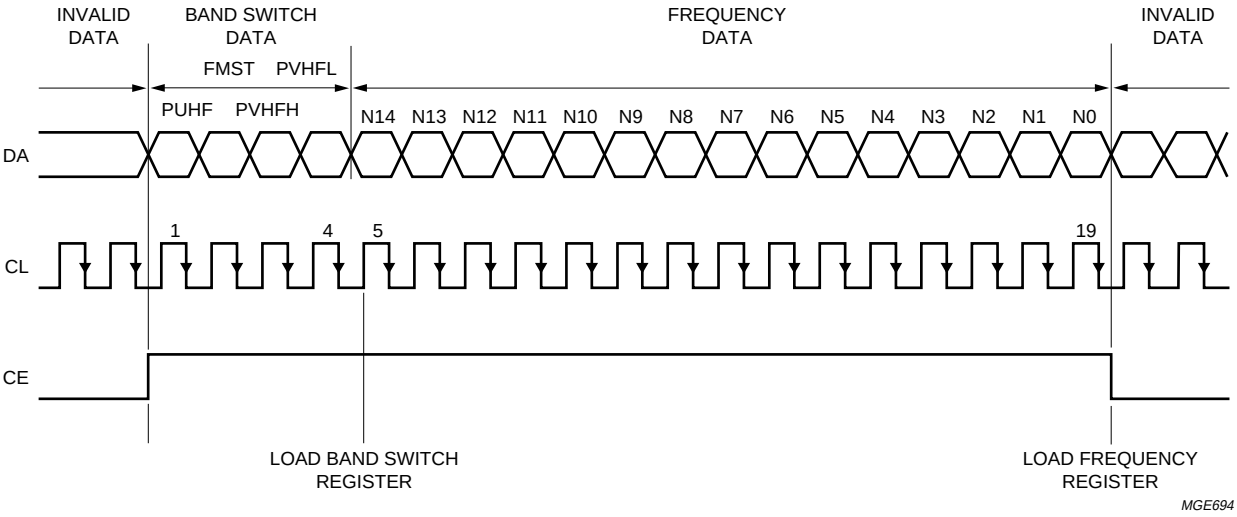


Fig.5 Normal mode; 19-bit data format (RSA = 0).

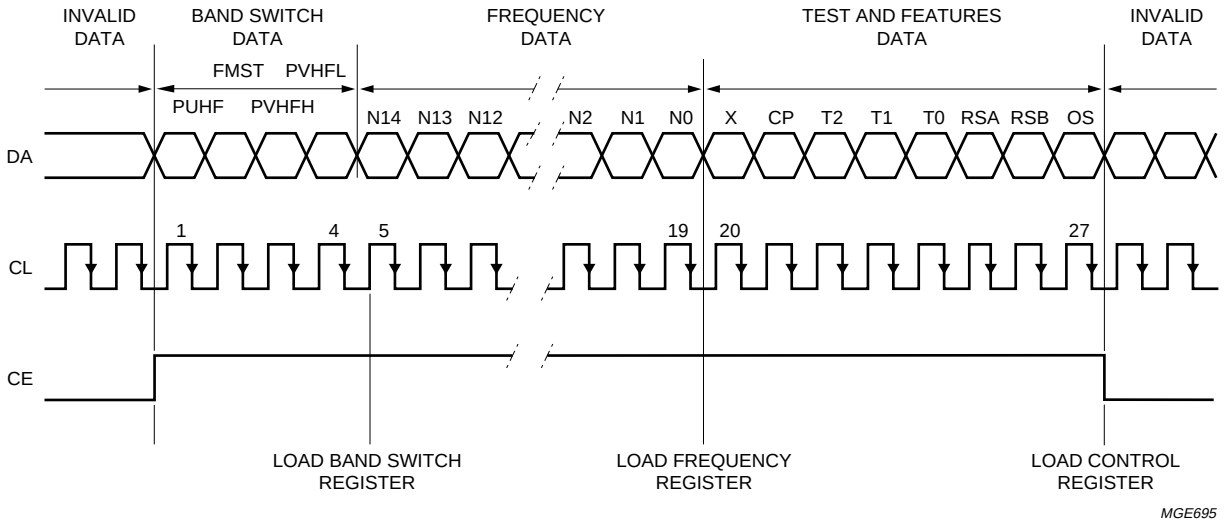


Fig.6 Test and features mode; 27-bit data format.

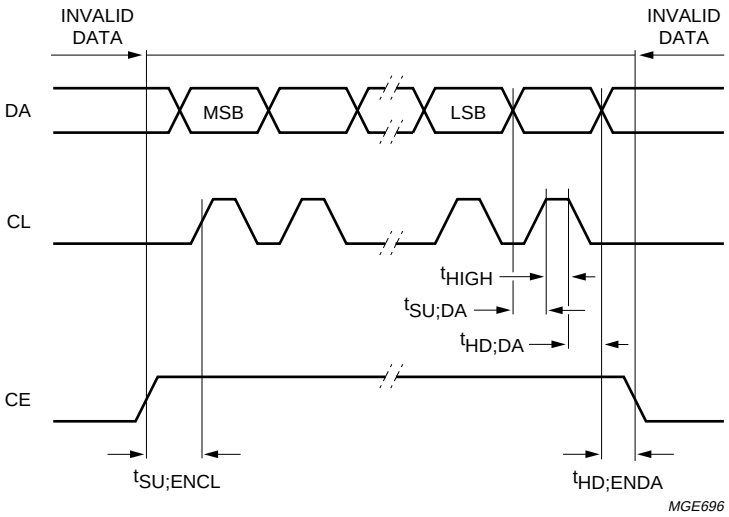


Fig.7 Timing diagram for 3-wire bus; SDA, SCL and CE.

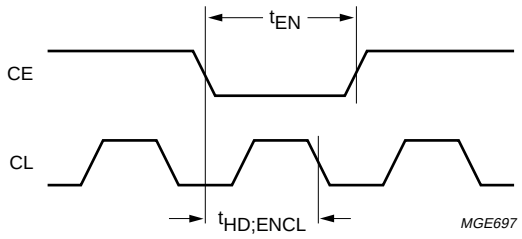


Fig.8 Timing diagram for 3-wire bus; CE and SCL.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PIN		PARAMETER	MIN.	MAX.	UNIT
	TDA6402	TDA6403				
V_{CC}	19	10	supply voltage	–0.3	+6	V
			operating supply voltage	4.5	5.5	V
V_{BSn}	7 to 10	19 to 22	PNP port output voltage	–0.3	+6	V
I_{BSn}	7 to 10	19 to 22	PNP port output current	–1	+30	mA
V_{CP}	16	13	charge-pump output voltage	–0.3	+6	V
V_{SW}	11	18	bus format selection input voltage	–0.3	+6	V
V_{VT}	17	12	tuning voltage output	–0.3	+35	V
$V_{LOCK/ADC}$	15	14	LOCK/ADC input/output voltage	–0.3	+6	V
V_{CL}	14	15	serial clock input voltage	–0.3	+6	V
V_{DA}	13	16	serial data input/output voltage	–0.3	+6	V
I_{DA}	13	16	data output current (I^2C-bus mode)	–1	+10	mA
V_{CE}	12	17	chip enable/address selection input voltage	–0.3	+6	V
V_{XTAL}	18	11	crystal input voltage	–0.3	+6	V
I_O	1 to 6, 19 to 28	1 to 10, 23 to 28	output current of each pin to ground	–	–10	mA
$t_{sc(max)}$	–	–	maximum short-circuit time (all pins to V_{CC} and all pins to GND, OSCGND, RFGND)	–	10	s
T_{stg}	–	–	IC storage temperature	–40	+150	°C
T_{amb}	–	–	operating ambient temperature	–10	+85	°C
T_j	–	–	junction temperature	–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	100	K/W

PLL PART CHARACTERISTICS

V_{CC} = 4.5 to 5.5 V; T_{amb} = –10 to 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PLL part						
SUPPLY						
V_{CC}	supply voltage		4.5	5.0	5.5	V
I_{CC}	supply current	I_{CC} measured at $V_{CC(max)}$	–	68	77	mA
		one PNP port is 'ON'; sourcing 25 mA	–	98	110	mA
		one PNP port is 'ON'; sourcing 25 mA and a second one is 'ON'; sourcing 5 mA	–	108	117	mA
FUNCTIONAL RANGE						
V_{POR}	power-on reset supply voltage	supply voltage below which power-on reset is active	1.5	2.0	–	V
T_{amb}	operating ambient temperature		–10	–	+85	°C
N	divider ratio	15-bit frequency word	256	–	32767	
		14-bit frequency word	256	–	16383	
f_{XTAL}	crystal oscillator	R_{XTAL} = 25 to 300 Ω	3.2	4.0	4.48	MHz
$\|Z_{XTAL}\|$	input impedance (absolute value)	f_{XTAL} = 4 MHz	600	1200	–	Ω
PNP PORTS						
$I_{BSn(off)}$	leakage current	V_{CC} = 5.5 V; V_{Pn} = 0 V	–10	–	–	μA
$V_{BSn(sat)}$	output saturation voltage	one buffer output is 'ON', sourcing 25 mA; $V_{Pn(sat)} = V_{CC} - V_{Pn}$	–	0.25	0.4	V
LOCK OUTPUT IN 3-WIRE BUS MODE (PNP COLLECTOR OUT)						
I_{UNLOCK}	output current when the PLL is out-of-lock	V_{CC} = 5.5 V; V_{OUT} = 5.5 V	–	–	100	μA
V_{UNLOCK}	output saturation voltage when the PLL is out-of-lock	I_{SOURCE} = 200 μA; $V_{UNLOCK} = V_{CC} - V_{OUT}$	–	0.4	0.8	V
V_{LOCK}	output voltage	the PLL is locked	–	0.01	0.40	V
ADC INPUT IN I^2C-BUS MODE						
V_{ADC}	ADC input voltage	see Table 10	0	–	V_{CC}	V
I_{ADCH}	HIGH-level input current	$V_{ADC} = V_{CC}$	–	–	10	μA
I_{ADCL}	LOW-level input current	V_{ADC} = 0 V	–10	–	–	μA
SW INPUT (BUS FORMAT SELECTION)						
V_{SWL}	LOW-level input voltage		0	–	1.5	V
V_{SWH}	HIGH-level input voltage		3	–	V_{CC}	V
I_{SWH}	HIGH-level input current	$V_{SW} = V_{CC}$	–	–	10	μA
I_{SWL}	LOW-level input current	V_{SW} = 0 V	–100	–	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CE/AS INPUT (CHIP ENABLE/ ADDRESS SELECTION)						
$V_{CE/ASL}$	LOW-level input voltage		0	–	1.5	V
$V_{CE/ASH}$	HIGH-level input voltage		3	–	5.5	V
$I_{CE/ASH}$	HIGH-level input current	$V_{CE/AS}$ = 5.5 V	–	–	10	µA
$I_{CE/ASL}$	LOW-level input current	$V_{CE/AS}$ = 0 V	–10	–	–	µA
CL AND DA INPUTS						
$V_{CL/DAL}$	LOW-level input voltage		0	–	1.5	V
$V_{CL/DAH}$	HIGH-level input voltage		3	–	5.5	V
$I_{CL/DAH}$	HIGH-level input current	V_{BUS} = 5.5 V; V_{CC} = 0 V	–	–	10	µA
		V_{BUS} = 5.5 V; V_{CC} = 5.5 V	–	–	10	µA
$I_{CL/DAL}$	LOW-level input current	V_{BUS} = 1.5 V; V_{CC} = 0 V	–	–	10	µA
		V_{BUS} = 0 V; V_{CC} = 5.5 V	–10	–	–	µA
DA OUTPUT (I^2C-BUS MODE)						
I_{DAH}	leakage current	V_{DA} = 5.5 V	–	–	10	µA
V_{DA}	output voltage	I_{DA} = 3 mA (sink current)	–	–	0.4	V
CLOCK FREQUENCY						
f_{clk}	clock frequency		–	100	400	kHz
CHARGE-PUMP OUTPUT CP						
I_{CPH}	HIGH-level input current (absolute value)	CP = 1	–	280	–	µA
I_{CPL}	LOW-level input current (absolute value)	CP = 0	–	60	–	µA
V_{CP}	output voltage	PLL is locked; T_{amb} = 25 °C	–	1.95	–	V
V_{CPleak}	off-state leakage current	T2 = 0; T1 = 1	–15	–0.5	+15	nA
TUNING VOLTAGE OUTPUT VT						
I_{VTOFF}	leakage current when switched-off	OS = 1; tuning supply = 33 V	–	–	10	µA
V_{VT}	output voltage when the loop is closed	OS = 0; T2 = 0; T1 = 0; T0 = 1; R_{LOAD} = 22 kΩ; tuning supply = 33 V	0.2	–	32.7	V
3-WIRE BUS TIMING						
t_{HIGH}	clock HIGH time	see Fig.7	2	–	–	µs
$t_{SU;DA}$	data set-up time	see Fig.7	2	–	–	µs
$t_{HD;DA}$	data hold time	see Fig.7	2	–	–	µs
$t_{SU;ENCL}$	enable to clock set-up time	see Fig.7	10	–	–	µs
$t_{HD;ENDA}$	enable to data hold time	see Fig.7	2	–	–	µs
t_{EN}	enable time between two transmissions	see Fig.8	10	–	–	µs
$t_{HD;ENCL}$	enable to clock active edge hold time	see Fig.8	6	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mixer/Oscillator part (V_{CC} = 5 V) (measured in circuit of Fig.19; unless otherwise specified)						
VHF MIXER (INCLUDING IF AMPLIFIER)						
f_{RF}	RF frequency	note 1	55.25	–	361.25	MHz
G_v	voltage gain	f_{RF} = 57.5 MHz; see Fig.12	16.5	19	21.5	dB
		f_{RF} = 357.5 MHz; see Fig.12	16.5	19	21.5	dB
NF	noise figure	f_{RF} = 50 MHz; see Figs 13 and 14	–	8.5	9.5	dB
		f_{RF} = 150 MHz; see Figs 13 and 14	–	8.5	10.5	dB
		f_{RF} = 300 MHz; see Fig.14	–	9.5	12.5	dB
V_o	output voltage causing 1% cross modulation in channel	f_{RF} = 55.25 MHz; see Fig.15	105	108	–	dBµV
		f_{RF} = 361.25 MHz; see Fig.15	105	108	–	dBµV
V_i	input voltage causing pulling in channel (750 Hz)	f_{RF} = 361.25 MHz; note 2	–	83	–	dBµV
g_{os}	optimum source conductance for noise figure	f_{RF} = 50 MHz	–	0.7	–	mS
		f_{RF} = 150 MHz	–	0.9	–	mS
		f_{RF} = 300 MHz	–	1.5	–	mS
g_i	input conductance	f_{RF} = 55.25 MHz; see Fig.9	–	0.25	–	mS
		f_{RF} = 361.25 MHz; see Fig.9	–	0.5	–	mS
C_i	input capacitance	f_{RF} = 57.5 to 357.5 MHz; see Fig.9	–	1.3	–	pF
VHF OSCILLATOR; see Fig.19						
f_{OSC}	oscillator frequency	note 3	101	–	407	MHz
$\Delta f_{OSC(V)}$	oscillator frequency shift	ΔV_{CC} = 5%; note 4	–	20	120	kHz
		ΔV_{CC} = 10%; note 4	–	110	–	kHz
$\Delta f_{OSC(T)}$	oscillator frequency drift	ΔT = 25 °C; with compensation; note 5	–	1600	2000	kHz
$\Delta f_{OSC(t)}$	oscillator frequency drift	5 s to 15 min after switch on; note 6	–	600	1100	kHz
Φ_{OSC}	phase noise, carrier to noise sideband	±100 kHz frequency offset; worst case in the frequency range	–	100	–	dBc/Hz
RSC	ripple susceptibility of V_P (peak-to-peak value)	V_P = 5 V; worst case in the frequency range; ripple frequency 500 kHz; note 7	15	20	–	mV
UHF MIXER (INCLUDING IF AMPLIFIER)						
f_{RF}	RF frequency	note 1	367.25	–	801.25	MHz
G_v	voltage gain	f_{RF} = 369.5 MHz; see Fig.16	26	29	32	dB
		f_{RF} = 803.5 MHz; see Fig.16	26	29	32	dB
NF	noise figure (not corrected for image)	f_{RF} = 369.5 MHz; see Fig.17	–	9	11	dB
		f_{RF} = 803.5 MHz; see Fig.17	–	10	12	dB
V_o	output voltage causing 1% cross modulation in channel	f_{RF} = 367.25 MHz; see Fig.18	105	108	–	dBµV
		f_{RF} = 801.25 MHz; see Fig.18	105	108	–	dBµV
V_i	input voltage causing pulling in channel (750 Hz)	f_{RF} = 801.25 MHz; note 2	–	82	–	dBµV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Z_i	input impedance ($R_S + jL_S\omega$)	R_S at f_{RF} = 367.25 MHz; see Fig.10	–	30	–	Ω
		R_S at f_{RF} = 801.25 MHz; see Fig.10	–	38	–	Ω
		L_S at f_{RF} = 367.25 MHz; see Fig.10	–	9	–	nH
		L_S at f_{RF} = 801.25 MHz; see Fig.10	–	6	–	nH
UHF OSCILLATOR						
f_{OSC}	oscillator frequency	note 3	413	–	847	MHz
$\Delta f_{OSC(V)}$	oscillator frequency shift	ΔV_{CC} = 5%; note 4	–	10	80	kHz
		ΔV_{CC} = 10%; note 4	–	300	–	kHz
$\Delta f_{OSC(T)}$	oscillator frequency drift	ΔT = 25 °C; with compensation; note 5	–	2000	2700	kHz
$\Delta f_{OSC(t)}$	oscillator frequency drift	5 s to 15 min after switching on; note 6	–	300	1300	kHz
Φ_{OSC}	phase noise, carrier to noise sideband	±100 kHz frequency offset; worst case in the frequency range	–	100	–	dBc/Hz
RSC	ripple susceptibility of V_P (peak-to-peak value)	V_P = 5 V (worst case in the frequency range); ripple frequency 500 kHz; note 7	15	28	–	mV
IF AMPLIFIER						
S_{22}	output reflection coefficient	magnitude; see Fig.11	–	–13.1	–	dB
		phase; see Fig.11	–	2.9	–	°
Z_o	output impedance ($R_S + jL_S\omega$)	R_S at 43.5 MHz; see Fig.11	–	75	–	Ω
		L_S at 43.5 MHz; see Fig.11	–	6.6	–	nH
REJECTION AT THE IF OUTPUT						
INT_{DIF}	level of divider interferences in the IF signal	note 8; worst case: channel C	–	25	–	dBμV
$INTR_{XTAL}$	crystal oscillator interferences rejection	V_{IF} = 100 dBμV; worst case in the frequency range; note 9	60	–	–	dBc
$INTRF_{REF}$	reference frequency rejection	V_{IF} = 100 dBμV; worst case in the frequency range; note 10	50	–	–	dBc
INT_{CH6}	channel 6 beat	$V_{RFpix} = V_{RFsnd}$ = 80 dBμV; note 11	57	–	–	dBc
INT_{CHA-5}	channel A-5 beat	V_{RFpix} = 80 dBμV; note 12	60	–	–	dBc

Notes

1. The RF frequency range is defined by the oscillator frequency range and the intermediate frequency (IF).
2. This is the level of the RF signal (100% amplitude modulated with 11.89 kHz) that causes a 750 Hz frequency deviation on the oscillator signal; it produces sidebands 30 dB below the level of the oscillator signal.
3. Limits are related to the tank circuits used in Fig.19; frequency bands may be adjusted by the choice of external components.
4. The frequency shift is defined as a change in oscillator frequency when the supply voltage varies from V_{CC} = 5 to 4.75 V (4.5 V) or from V_{CC} = 5 to 5.25 V (5.5 V). The oscillator is free running during this measurement.
5. The frequency drift is defined as a change in oscillator frequency when the ambient temperature varies from T_{amb} = 25 to 50 °C or from T_{amb} = 25 to 0 °C. The oscillator is free running during this measurement.
6. Switch-on drift is defined as the change in oscillator frequency between 5 s and 15 min after switch on. The oscillator is free running during this measurement.

7. The ripple susceptibility is measured for a 500 kHz ripple at the IF output using the measurement circuit of Fig.19; the level of the ripple signal is increased until a difference of 53.5 dB occurs between the IF carrier fixed at 100 dBμV and the sideband components.
8. This is the level of divider interferences close to the IF frequency. For example channel C: f_{OSC} = 179 MHz, $\frac{1}{4} f_{OSC}$ = 44.75 MHz. Divider interference is measured with the Philips 37511 demonstration board in accordance with Fig.19. All ground pins are connected to a single ground plane under the IC. The VHFIN input must be left open (i.e. not connected to any load or cable); The UHFIN1 and UHFIN2 inputs are connected to a hybrid.
   The measured levels of divider interference are influenced by layout, grounding and port decoupling.
   The measurement results could vary by as much as 10 dB with respect to the specification.
9. Crystal oscillator interference means the 4 MHz sidebands caused by the crystal oscillator. The rejection has to be greater than 60 dB for an IF output signal of 100 dBμV.
10. The reference frequency rejection is the level of reference frequency sidebands related to the sound sub-carrier. The rejection has to be greater than 50 dB for an IF output signal of 100 dBμV.
11. Channel 6 beat is the interfering product of $f_{RFpix} + f_{RFsnd} - f_{OSC}$ of channel 6 at 42 MHz.
12. Channel A-5 beat is the interfering product of f_{RFpix}, f_{IF} and f_{OSC} of channel A-5; f_{BEAT} = 45.5 MHz. The possible mechanisms are: $f_{OSC} - 2 \times f_{IF}$ or $2 \times f_{RFpix} - f_{OSC}$. For the measurement V_{RF} = 80 dBμV.

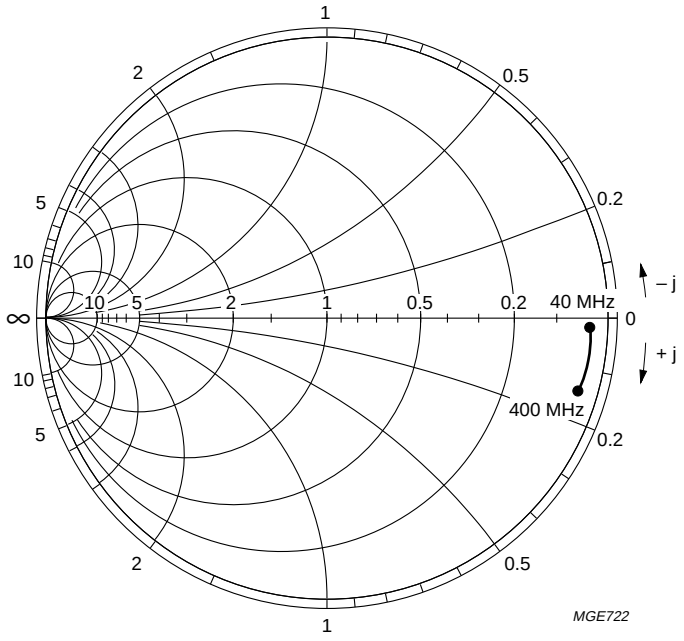


Fig.9 Input admittance (S_{11}) of the VHF mixer input (40 to 400 MHz); Y_0 = 20 mS.

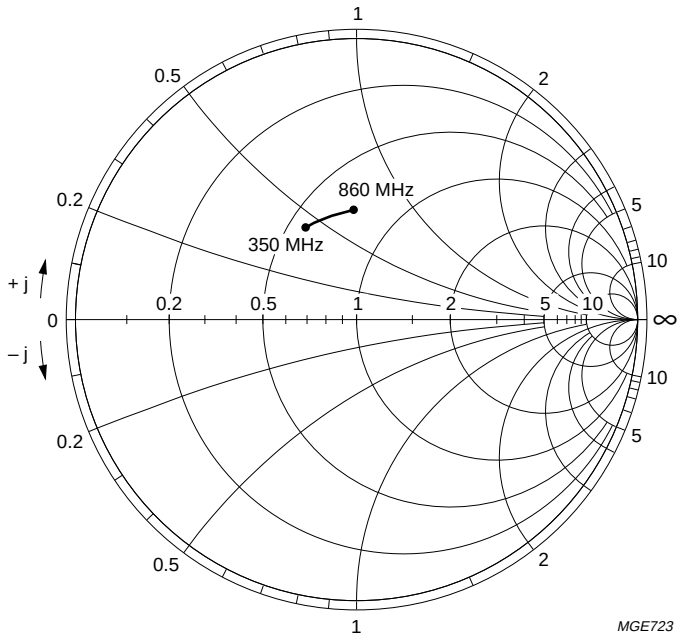


Fig.10 Input impedance (S_{11}) of the UHF mixer input (350 to 860 MHz); Z_0 = 50 Ω.

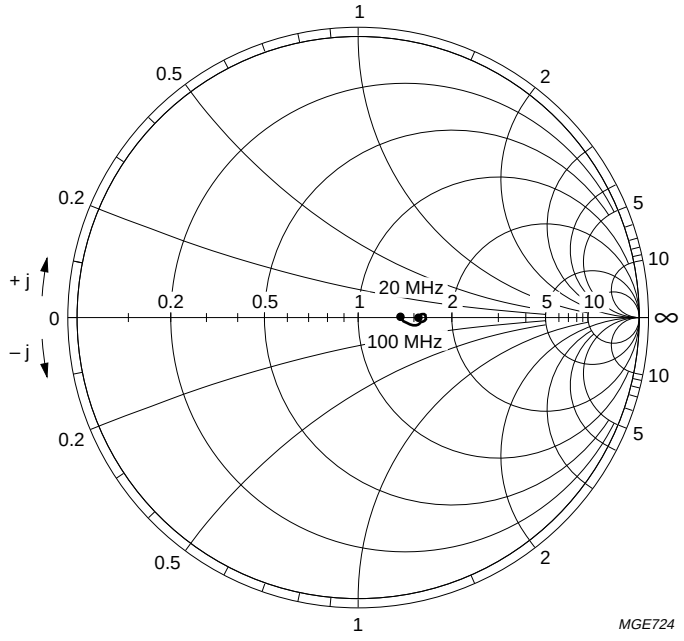
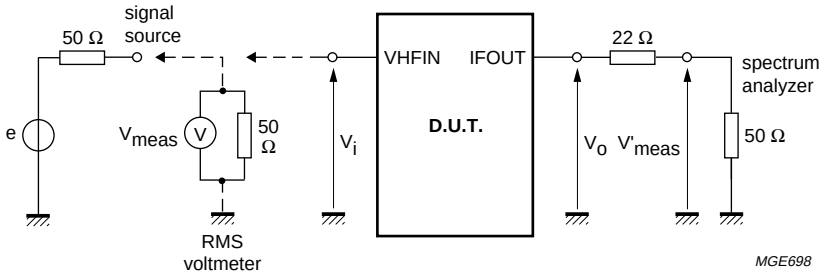


Fig.11 Output impedance (S_{22}) of the IF amplifier (20 to 60 MHz); Z_0 = 50 Ω.

TEST AND APPLICATION INFORMATION



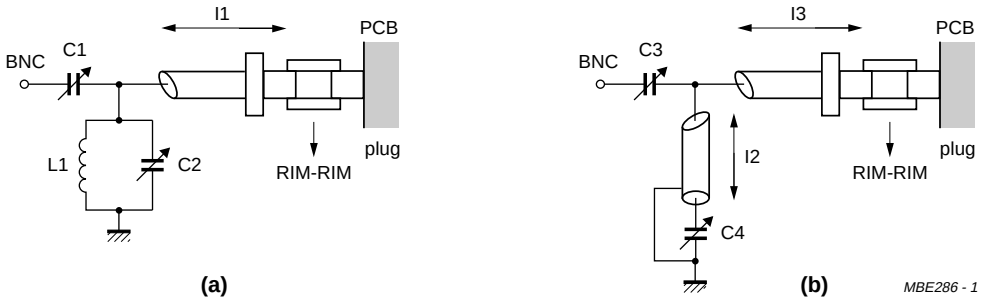
(1) $Z_i >> 50\ \Omega \Rightarrow V_i = 2 \times V_{meas} = 80\ dB\mu V$.

(2) $V_i = V_{meas} + 6\ dB = 80\ dB\mu V$.

(3) $V_o = V'_{meas} \times \frac{50 + 22}{50}$.

(4) $G_v = 20\log \frac{V_o}{V_i}$.

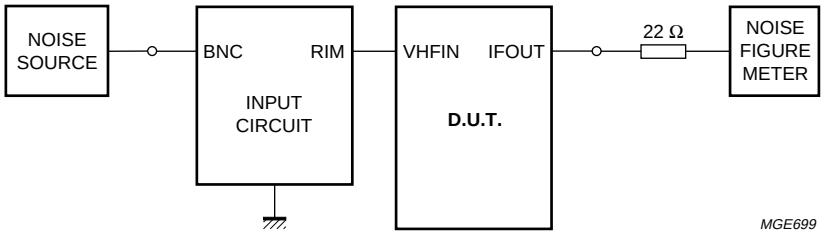
Fig.12 Gain measurement in VHF band.



(a) For f_{RF} = 50 MHz:
mixer A frequency response measured = 57 MHz, loss = 0 dB
image suppression = 16 dB
C1 = 9 pF
C2 = 15 pF
L1 = 7 turns (∅ 5.5 mm, wire ∅ = 0.5 mm)
l1 = semi rigid cable (RIM): 5 cm long
(semi rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

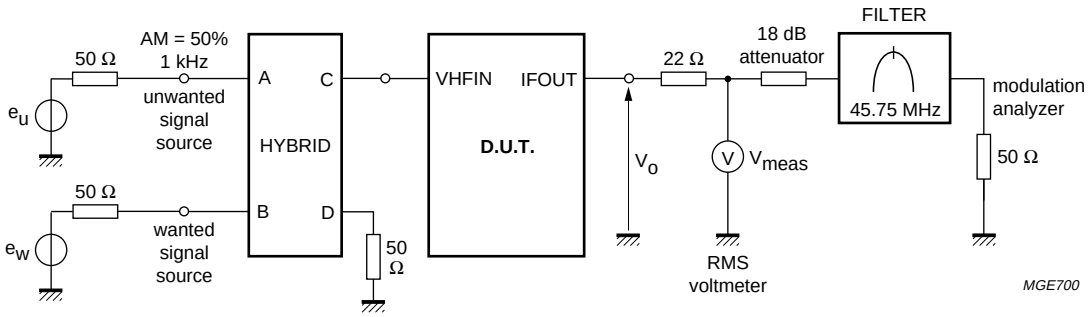
(b) For f_{RF} = 150 MHz:
mixer A frequency response measured = 150.3 MHz, loss = 1.3 dB
image suppression = 13 dB
C3 = 5 pF
C4 = 25 pF
l2 = semi rigid cable (RIM): 30 cm long
l3 = semi rigid cable (RIM): 5 cm long
(semi rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

Fig.13 Input circuit for optimum noise figure in VHF band.



NF = NF_{meas} – loss (of input circuit) (dB).

Fig.14 Noise figure (NF) measurement in VHF band.



$V_{meas} = V_o \times \frac{50 + 22}{50}$.

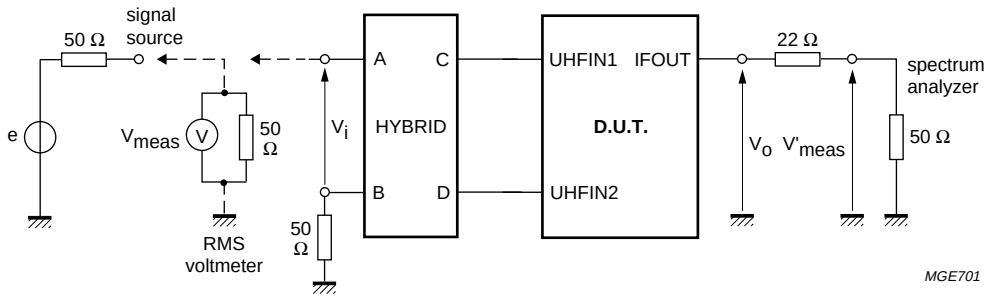
Wanted output signal at f_{RFW} = 55.25 (361.25) MHz; $V_{o(w)}$ = 100 dBµV.

Measuring the level of the unwanted signal $V_{o(u)}$ causing 0.5% AM modulation in the wanted output signal; f_{RFU} = 59.75 (365.75) MHz.

f_{OSC} = 101 (407) MHz.

Filter characteristics: f_C = 45.75 MHz, $f_{-3dB(BW)}$ = 1.4 MHz, $f_{-30dB(BW)}$ = 3.1 MHz.

Fig.15 Cross modulation measurement in VHF band.



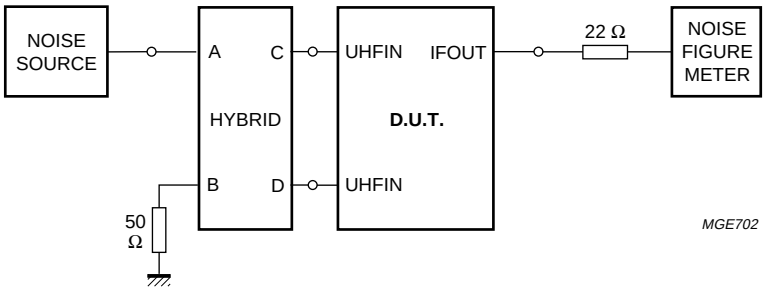
Loss (in hybrid) = 1 dB.

$V_i = V_{meas}$ – loss (in hybrid) = 70 dBμV.

$$V_o = V'_{meas} \times \frac{50 + 22}{50}.$$

$$G_v = 20\log\frac{V_o}{V_i}.$$

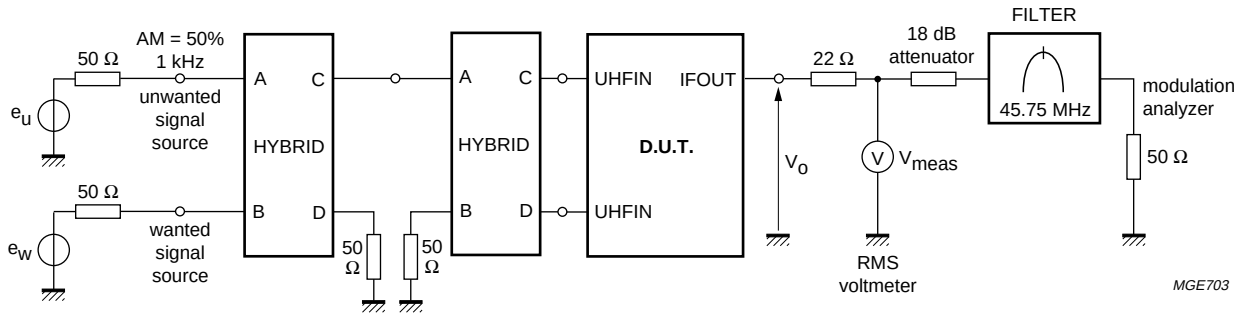
Fig.16 Gain (G_v) measurement in UHF band.



Loss (in hybrid) = 1 dB.

$NF = NF_{meas}$ – loss (in hybrid).

Fig.17 Noise figure (NF) measurement in bands UHF.



$V_{meas} = V_o \times \frac{50 + 22}{50}$.

Wanted output signal at f_{RFW} = 367.25 (801.25) MHz: $V_{o(w)}$ = 100 dBµV.

Measuring the level of the unwanted output signal $V_{o(u)}$ causing 0.5% AM modulation in the wanted output signal; f_{RFU} = 371.25 (805.75) MHz.

f_{OSC} = 413 (847) MHz.

Filter characteristics: f_C = 45.75 MHz, $f_{-3dB(BW)}$ = 1.4 MHz, $f_{-30dB(BW)}$ = 3.1 MHz.

Fig.18 Cross modulation measurement in UHF band.

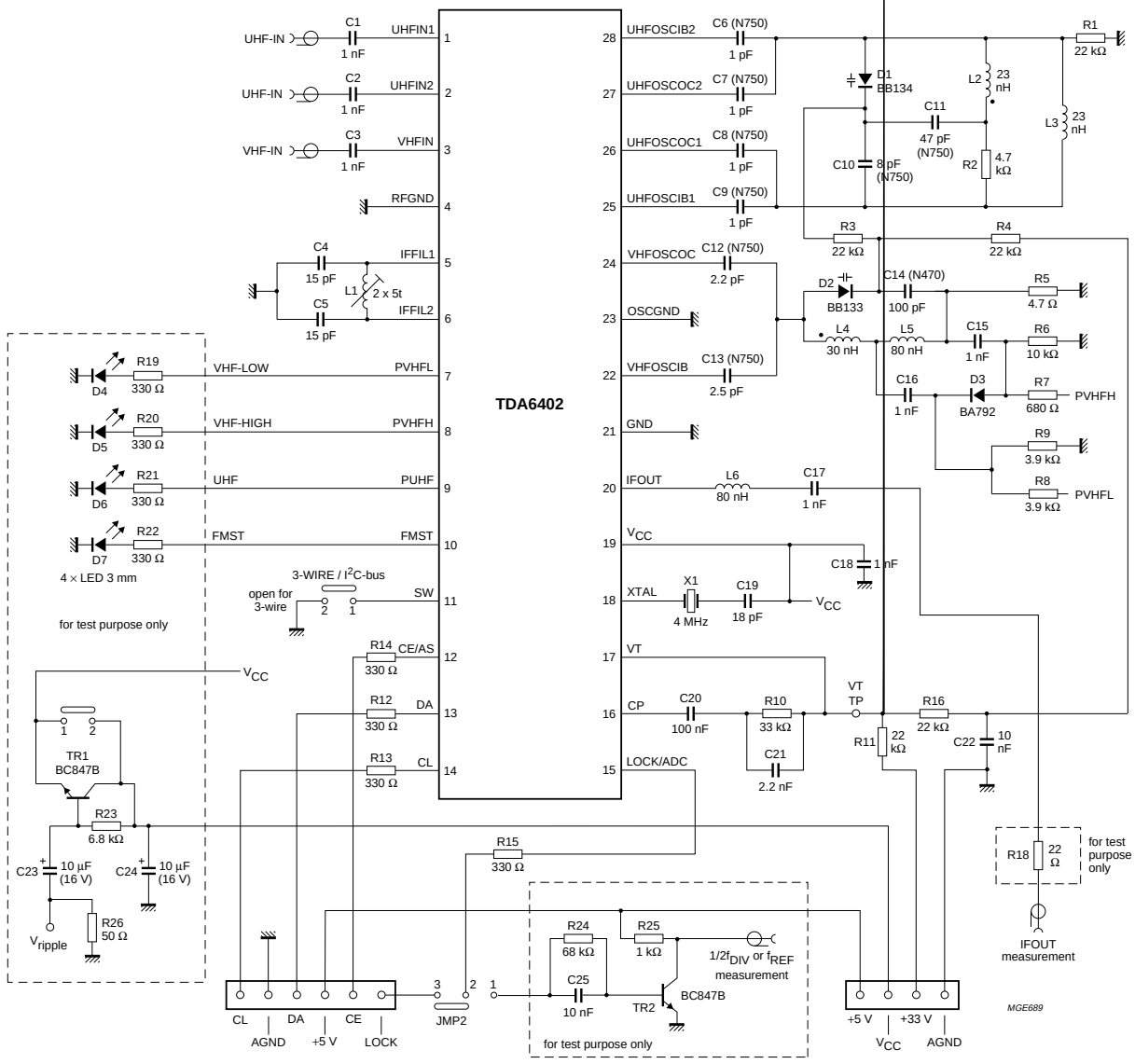


Fig.19 Measurement circuit.

Component values for measurement circuit

Table 12 Capacitors (all SMD and NP0)

COMPONENT	VALUE
C1	1 nF
C2	1 nF
C3	1 nF
C4	15 pF
C5	15 pF
C6	1 pF (N750)
C7	1 pF (N750)
C8	1 pF (N750)
C9	1 pF (N750)
C10	8 pF (N750)
C11	47 pF (N750)
C12	2.2 pF (N750)
C13	2.7 pF (N750)
C14	100 pF (N470)
C15	1 nF
C16	1 nF
C17	1 nF
C18	1 nF
C19	18 pF
C20	100 nF
C21	2.2 nF
C22	10 nF
C23	10 μF (16 V; electrolytic)
C24	10 μF (16V; electrolytic)
C25	10 nF

Table 13 Resistors (all SMD)

COMPONENT	VALUE
R1	22 kΩ
R2	4.7 kΩ
R3	22 kΩ
R4	22 kΩ
R5	4.7 Ω
R6	10 kΩ
R7	680 Ω
R8	3.9 kΩ
R9	3.9 kΩ
R10	33 kΩ
R11	22 kΩ
R12	330 Ω
R13	330 Ω
R14	330 Ω
R15	330 Ω
R16	22 kΩ
R18	22 Ω
R19	330 Ω
R20	330 Ω
R21	330 Ω
R22	330 Ω
R23	6.8 kΩ
R24	68 kΩ
R25	1 kΩ
R26	50 Ω

Table 14 Diodes and ICs

COMPONENT	VALUE
D1	BB134
D2	BB133
D3	BA792
IC	TDA6402 or TDA6403

Table 15 Coils (wire size 0.4 mm)

COMPONENT	VALUE
L2	23 nH
L3	23 nH
L4	30 nH
L5	80 nH
L6	80 nH

Table 16 Transformer (note 1)

COMPONENT	VALUE
L1	2 × 5 turns

Note

1. Coil type: TOKO 7kN; material: 113 kN; screw core: 03-0093; pot core: 04-0026.

Table 17 Crystal

COMPONENT	VALUE
X1	4 MHz

Table 18 Transistors

COMPONENT	VALUE
TR1	BC847B
TR2	BC847B

Tuning amplifier

The tuning amplifier is capable of driving the varicap voltage without an external transistor. The tuning voltage output must be connected to an external load of 27 kΩ which is connected to the tuning voltage supply rail. The loop filter design depends on the oscillator characteristics and the selected reference frequency.

Crystal oscillator

The crystal oscillator uses a 4 MHz crystal connected in series with an 18 pF capacitor thereby operating in the series resonance mode. Connecting the oscillator to the supply voltage is preferred, but it can also be connected to ground.

Examples of I^2C-bus sequences (SW = V_{CC})

Tables 19 to 23 show the various sequences where:

f_{OSC} = 100 MHz

PVHFL = ‘ON’ to switch on VHF I

FMST is ‘ON’ to switch on an FM sound trap

I_{CP} = 280 μA

N = 512

f_{XTAL} = 4 MHz

S = start

A = acknowledge

P = stop.

For the complete sequence see Table 19 (sequence 1) or Table 20 (sequence 2).

Table 19 Complete sequence 1

start	address byte		divider byte 1		divider byte 2		control byte		band switch byte		stop
S	C2	A	06	A	40	A	CE	A	09	A	P

Table 20 Complete sequence 2

start	address byte		control byte		band switch byte		divider byte 1		divider byte 2		stop
S	C2	A	CE	A	09	A	06	A	40	A	P

Table 21 Divider bytes only sequence

S	C2	A	06	A	40	A	P

Table 22 Control and band switch bytes only sequence

S	C2	A	CE	A	09	A	P

Table 23 Control byte only sequence

S	C2	A	CE	A	P

Table 24 Status byte acquisition

S	C3	A	XX(1)	X(2)	P

Notes

1. XX = Read status byte.
2. X = No acknowledge from the master means end of sequence.

Table 25 Two status bytes acquisition

S	C3	A	XX(1)	A	XX(1)	X(2)	P

Notes

1. XX = Read status byte.
2. X = No acknowledge from the master means end of sequence.

Other I^2C-bus addresses may be selected by applying an appropriate voltage to the CE input.

Examples of 3-wire bus sequences (SW = OPEN)

Table 26 18-bit sequence (f_{OSC} = 800 MHz; PUHF = ON)

1	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0

The reference divider is automatically set to 512 assuming that RSB has been set to logic 1 at power-on. If RSB has been set to logic 0, in a previous 27-bit sequence, the reference divider will still be set at 640. In that event, the 18-bit sequence has to be adapted to the 640 divider ratio.

Table 27 19-bit sequence (f_{OSC} = 650 MHz; PUHF = ON)

1	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	0

The reference divider is automatically set to 512 assuming that RSB has been set to logic 1 at power-on. If RSB has been set to logic 0 in a previous 27-bit sequence, the reference divider will still be set at 640. In that event, the 19-bit sequence has to be adapted to the 640 divider ratio.

Table 28 27-bit sequence (f_{OSC} = 750 MHz; PUHF = ON; N = 640; I_{CP} = 60 μA; no test function)

1	0	0	0	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0

Table 29 19-bit sequence

1	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0	0

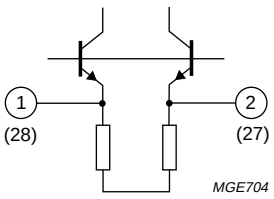
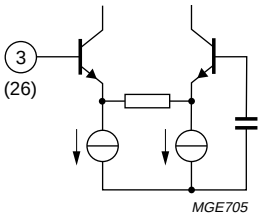
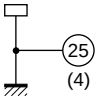
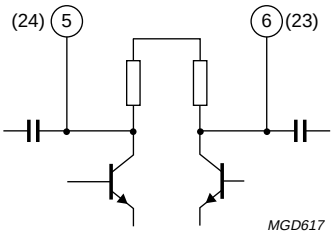
This sequence will program f_{OSC} to 600 MHz in 50 kHz steps; I_{CP} remains at 60 μA.

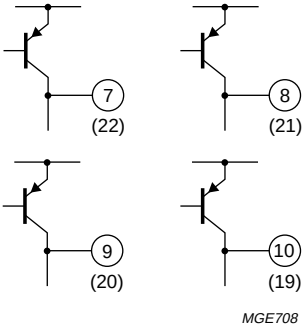
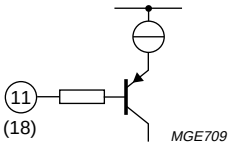
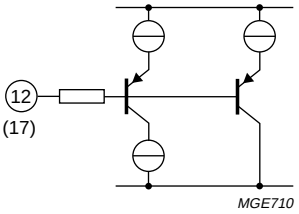
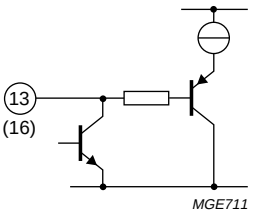
Table 30 18-bit sequence

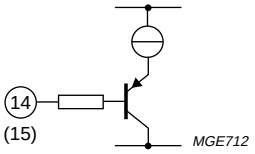
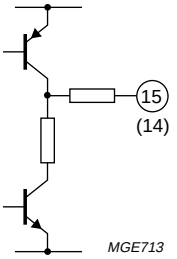
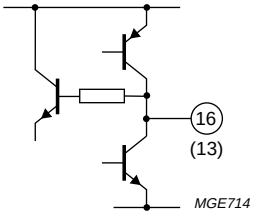
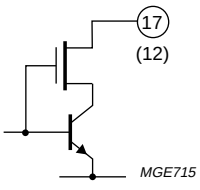
1	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0	0

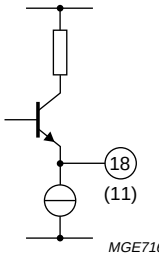
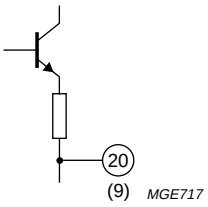
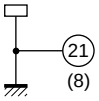
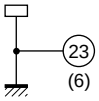
This sequence will program f_{OSC} to 600 MHz in 50 kHz steps; I_{CP} remains at 60 μA.

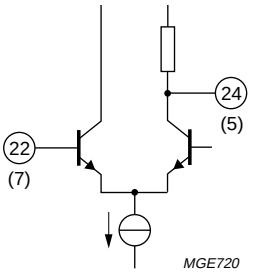
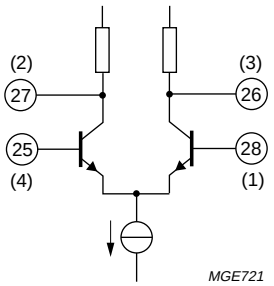
INTERNAL PIN CONFIGURATION

SYMBOL	PIN		DESCRIPTION(1)	AVERAGE DC VOLTAGE (V) (measured in Fig.19)	
	TDA6402	TDA6403		VHF	UHF
UHFIN1	1	28		n.a.	1.0
UHFIN2	2	27		n.a.	1.0
VHFIN	3	26		1.8	n.a.
RFGND	4	25		0.0	0.0
IFFIL1	5	24		3.6	3.6
IFFIL2	6	23		3.6	3.6

SYMBOL	PIN		DESCRIPTION(1)	AVERAGE DC VOLTAGE (V) (measured in Fig.19)	
	TDA6402	TDA6403		VHF	UHF
PVHFL	7	22		0.0 or ($V_{CC} - V_{CE}$)	0.0
PVHFH	8	21		($V_{CC} - V_{CE}$) or 0.0	0.0
PUHF	9	20		0.0	($V_{CC} - V_{CE}$)
FMST	10	19		0.0 or ($V_{CC} - V_{CE}$)	0.0
SW	11	18		5.0	5.0
CE/AS	12	17		1.25	1.25
DA	13	16		n.a.	n.a.

SYMBOL	PIN		DESCRIPTION(1)	AVERAGE DC VOLTAGE (V) (measured in Fig.19)	
	TDA6402	TDA6403		VHF	UHF
CL	14	15		n.a.	n.a.
LOCK/ADC	15	14		4.6	4.6
CP	16	13		1.9	1.9
VT	17	12		V_{VT}	V_{VT}

SYMBOL	PIN		DESCRIPTION(1)	AVERAGE DC VOLTAGE (V) (measured in Fig.19)	
	TDA6402	TDA6403		VHF	UHF
XTAL	18	11		3.4	3.4
V_{CC}	19	10	supply voltage	5.0	5.0
IFOUT	20	9		2.1	2.1
GND	21	8		0.0	0.0
OSCGND	23	6		0.0	0.0

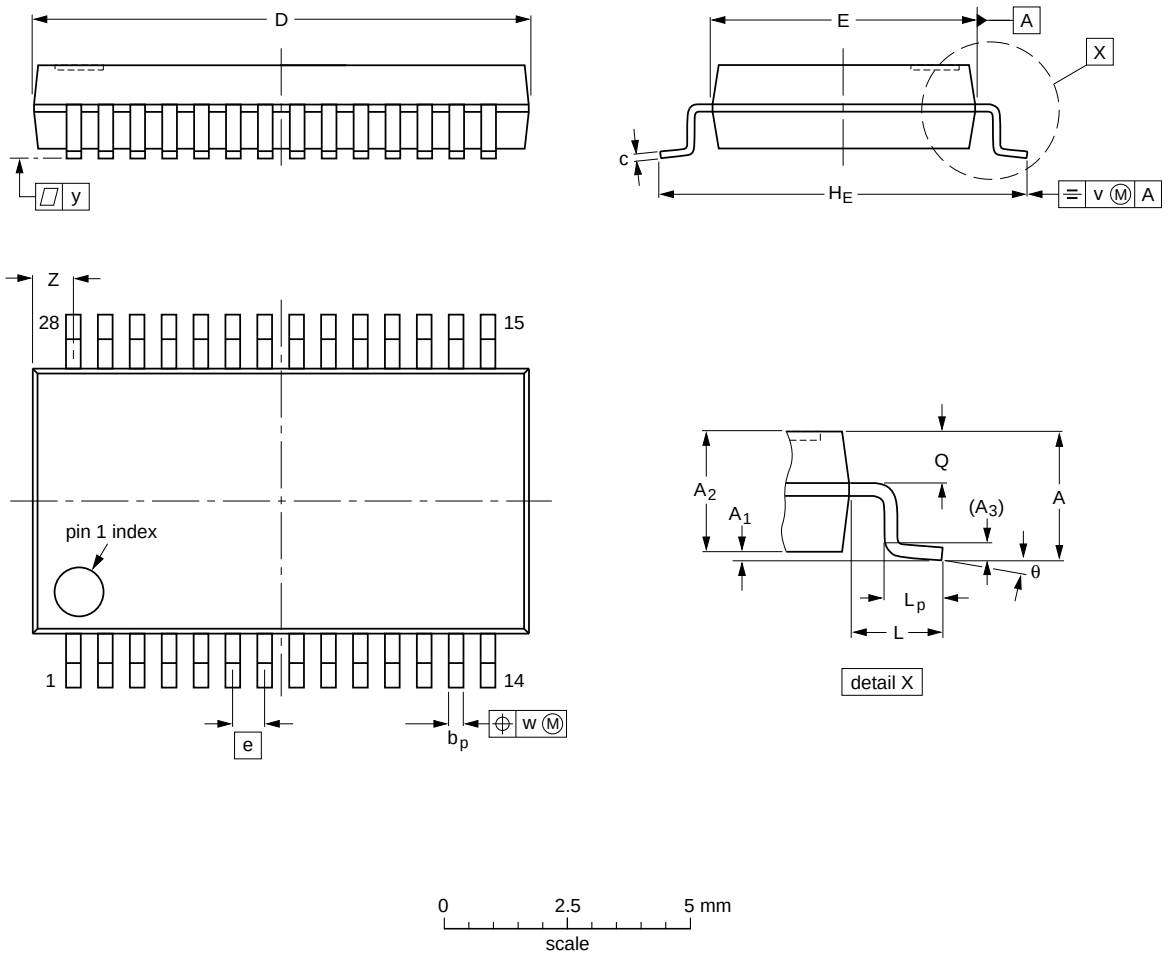
SYMBOL	PIN		DESCRIPTION(1)	AVERAGE DC VOLTAGE (V) (measured in Fig.19)	
	TDA6402	TDA6403		VHF	UHF
VHFOSCIB	22	7		1.8	n.a.
VHFOSCOC	24	5		3.0	n.a.
UHFOSCIB1	25	4		n.a.	1.9
UHFOSCOC1	26	3		n.a.	2.9
UHFOSCOC2	27	2		n.a.	2.9
UHFOSCIB2	28	1		n.a.	1.9

Note

1. The pin numbers in parenthesis represent the TDA6403.
2. n.a. = not applicable.

PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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