DATA SHEET

TDA4884
Three gain control video pre-amplifier for OSD

Preliminary specification
File under Integrated Circuits, IC02

June 1994

Philips
Semiconductors

PHILIPS

Three gain control video pre-amplifier for OSD TDA4884

FEATURES

- 85 MHz video controller
- Fully DC controllable
- 3 separate video channels
- Input black level clamping
- White level adjustment for 3 channels
- Contrast control for all 3 channels simultaneously
- Cathode feedback to internal reference for cut-off control, which allows unstabilized video supply voltage
- Current outputs for RGB signal currents
- RGB voltage outputs to external peaking circuits
- Blanking and switch-off input for screen protection
- Sync on green operation possible
- OSD application very easily.

GENERAL DESCRIPTION

The TDA4884 is a monolithic integrated RGB amplifier for colour monitor systems with super VGA performance, intended for DC or AC coupling of the colour signals to the cathodes of the CRT. With special advantages the circuit can be used in conjunction with the TDA485x monitor deflection IC family.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 7)		7.2	8.0	8.8	V
I_P	supply current		–	48	–	mA
$V_{I(b-w)}$	input voltage (black-to-white; pins 2, 5 and 8)		–	0.7	1.0	V
$V_{O(b-w)}$	output voltage (black-to-white; pins 19, 16 and 13)	nominal contrast; pins 3, 1 and 11 open-circuit	–	0.79	–	V
$I_{O(b-w)}$	output current (black-to-white; pins 20, 17 and 14)		–	50	–	mA
I_M	peak output current (pins 20, 17 and 14)		–	–	100	mA
B	bandwidth	–3 dB	70	85	–	MHz
G_{nom}	nominal gain (pins 2, 5 and 8 to pins 19, 16 and 13)	nominal contrast; pins 3, 1 and 11 open-circuit	–	1	–	dB
G_v	gain control for all channels (relative to G_{nom})		–5	–	+2.6	dB
C_v	contrast control	V_6 = 1 to 6 V	–22	–	+3.4	dB
C_{OSD}	minimum contrast for OSD	V_6 = 0.7 V	–	–40	–	dB
T_{amb}	operating ambient temperature		–20	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4884	20	DIL	plastic	SOT146(1)

Note

1. SOT146-1; 1996 November 22.

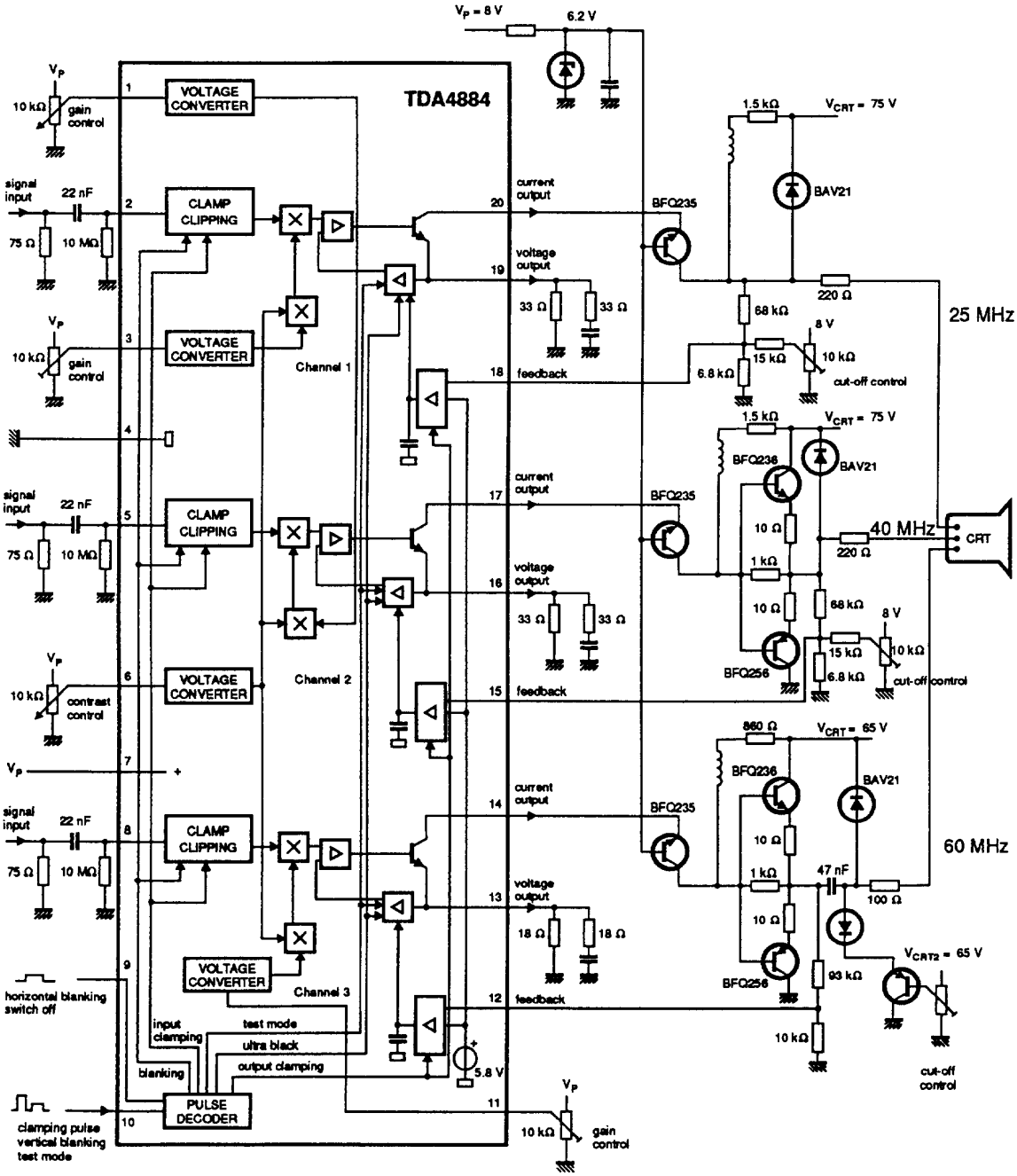


Fig.1 Block diagram and basic application circuit for DC and AC coupling.

PINNING

SYMBOL	PIN	DESCRIPTION
G_{C2}	1	gain control Channel 2
V_{I1}	2	signal input Channel 1
G_{C1}	3	gain control Channel 1
GND	4	ground
V_{I2}	5	signal input Channel 2
C_C	6	contrast control, OSD switch
V_P	7	supply voltage
V_{I3}	8	signal input Channel 3
HBL	9	horizontal blanking, switch-off
CL	10	input clamping, vertical blanking, test mode
G_{C3}	11	gain control Channel 3
FB_3	12	feedback Channel 3
V_{O3}	13	voltage output Channel 3
I_{O3}	14	current output Channel 3
FB_2	15	feedback Channel 2
V_{O2}	16	voltage output Channel 2
I_{O2}	17	current output Channel 2
FB_1	18	feedback Channel 1
V_{O1}	19	voltage output Channel 1
I_{O1}	20	current output Channel 1

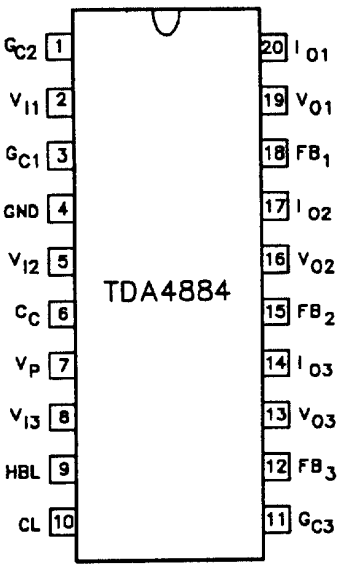


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The RGB input signals (0.7 $V_{(p-p)}$) are capacitively coupled into the TDA4884 (pins 2, 5 and 8) from a low ohmic source and are clamped to an internal DC voltage (artificial black level). Composite signals will not disturb normal operations because an internal clipping circuit cuts all signal parts below black level. All channels have a maximum total voltage gain of 7 dB (maximum contrast and maximum individual channel gain). With the nominal channel gain of 1 dB and nominal contrast setting the nominal black-to-white output amplitude is 0.79 $V_{(p-p)}$.

DC voltages are used for contrast and gain control.

Contrast control is achieved by a voltage at pin 6 and affects the three channels simultaneously. To provide the correct white point, an individual **gain control** (pins 3, 1 and 11) adjusts the signals of Channels 1, 2 and 3.

Each **output stage** provides a current output (pins 20, 17 and 14) and a voltage output (pins 19, 16 and 13). External cascode transistors reduce power consumption of the IC and prevent breakdown of the output transistors. Signal output currents and peaking characteristics are determined by external components at the voltage outputs and the video supply. The channels have separate internal feedback loops which ensure large signal linearity and marginal signal distortion in spite of output transistor thermal V_{BE} variation.

The **clamping pulse** (pin 10) is used for **input clamping** only. The input signals have to be at black level during the clamping pulse and are clamped to an internal artificial black level. The coupling capacitors are used in this way for black level storage. Because the threshold for the clamping pulse is higher than that for vertical blanking (pin 10) the rise and fall times of the clamping pulse have to be faster than 75 ns/V during transition from 1 V to 3.5 V.

The **vertical blanking pulse** will be detected if the input voltage (pin 10) is higher than the threshold voltage for approximately 320 ns but does not exceed the threshold for the clamping pulse in the time between. During the vertical blanking pulse the input clamping is disabled in order to avoid misclamping in the event of composite input signals.

The input signal is blanked and the artificial black level is inserted instead, thus the output signal is at reference black level. The DC value of the reference black level will be adjusted by cut-off stabilization (see below).

During **horizontal blanking** (pin 9) the output signal is set to reference black level as previously described and **output clamping** is activated. If the voltage at pin 9 exceeds the **switch-off** threshold the signal is blanked and switched to ultra black level for screen protection and spot suppression during V-flyback. Ultra black level is the lowest possible output voltage (at voltage outputs) and does not depend on cut-off stabilization.

For **cut-off stabilization** (DC coupling to the CRT) respectively **black level stabilization** (AC coupling) the video signal at the cathode or the coupling capacitor is divided by an adjustable voltage divider and fed to the feedback inputs (pins 18, 15 and 12). During the horizontal blanking time this signal is compared with an internal DC voltage of approximately 5.8 V. Any difference will lead to a reference black level correction by charging or discharging the integrated capacitor which stores the reference black level information between the horizontal blanking pulses.

For OSD fast switching of control pin 6 to less than 1 V (e.g. 0.7 V) blanks the input signals. The OSD signals can easily be inserted to the external cascode transistor (see Fig.3).

During **test mode** (pins 9 and 10 connected to V_P) the black levels at the voltage outputs (pins 12, 16 and 13) are internally set to typical 0.5 V (3 V DC at signal inputs (pins 2, 5 and 8)).

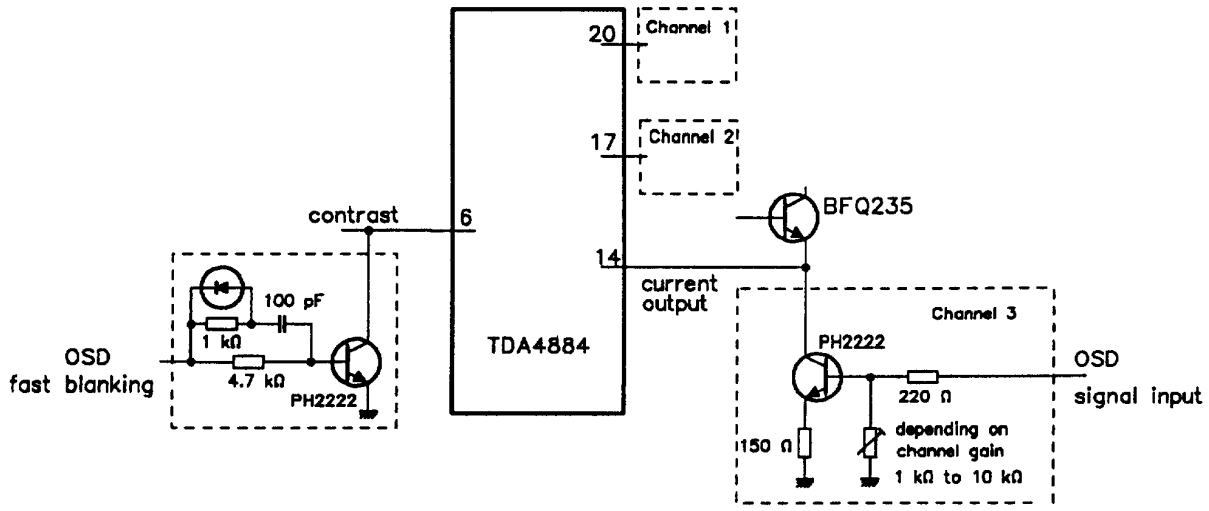


Fig.3 OSD application.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 7)	0	8.8	V
V_I	input voltage (pins 2, 5 and 8)	–0.1	V_P	V
V_{ext}	external DC voltage			
	pins 20, 17 and 14	–0.1	V_P	V
	pins 19, 16 and 13	no external voltages		
	pins 1, 3, 6 and 11	–0.1	V_P	V
	pin 9	–0.1	$V_P + 0.7$	V
	pin 10	–0.1	$V_P + 0.7$	V
I_O	average output current (pins 20, 17 and 14; note 1)	0	50	mA
I_M	peak output current (pins 20, 17 and 14)	0	100	mA
P_{tot}	total power dissipation	–	1200	mW
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	–20	+70	°C
T_j	junction temperature	–25	+150	°C
V_{ESD}	electrostatic handling for all pins (note 2)	–500	+500	V

Notes to the limiting values

1. Signal amplitude of 50 mA black-to-white is possible if the average current (including blanking times and signal variation against time) does not exceed 50 mA. The maximum power dissipation of 1200 mW has to be considered.
2. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	65 K/W

CHARACTERISTICS

V_P = 8.0 V; T_{amb} = +25 °C; all voltages measured to GND (pin 4); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 7)		7.2	8.0	8.8	V
I_P	supply current (pin 7)		36	48	60	mA
Video signal inputs (Channel 1: pin 2, Channel 2: pin 5 and Channel 3: pin 8)						
$V_{I(b-w)}$	input voltage (black-to-white value; pins 2, 5 and 8)		–	0.7	1.0	V
$V_{IC2,5,8}$	DC voltage during input clamping (artificial black + V_{BE})	note 1	2.8	3.1	3.4	V
$I_{2,5,8}$	DC current	no clamping; $V_{2,5,8} = V_{IC2,5,8}$; T_{amb} = –20 to +70 °C	–0.05	+0.05	+0.250	µA
		during clamping; $V_{2,5,8} = V_{IC2,5,8} \pm 0.7$ V	±50	±75	±120	µA
Contrast control (pin 6; note 2)						
V_6	input voltage		1.0	–	6.0	V
	maximum input voltage		–	–	V_P – 1	V
V_{N6}	input voltage for nominal contrast	note 3	–	4.3	–	V
I_6	input current	V_6 = 4.3 V	–5	–1	–0.1	µA
C_v	contrast relative to nominal contrast	V_6 = 6.0 V; pins 3, 1 and 11 open-circuit	2.4	3.4	–	dB
		V_6 = 1.0 V; pins 3, 1 and 11 open-circuit	–26	–22	–19	dB
V_{M6}	input voltage for minimum contrast	pins 3, 1 and 11 open-circuit	–	0.7	–	V
Tr	tracking of output signals of Channels 1, 2 and 3	1 V < V_6 < 6 V; note 4	–	0	0.5	dB
t_{dfC}	delay between leading edges (falling) of step in contrast voltage and output signals at voltage outputs (pins 19, 16 and 13)	V_6 = 4.3 V to 0.7 V; input fall time at pin 6: t_{fCC} = 2 ns; note 5	–	7	20	ns
t_{drC}	delay between trailing edges (rising) of step in contrast voltage and output signals at voltage outputs (pins 19, 16 and 13)	V_6 = 0.7 V to 4.3 V; input rise time at pin 6: t_{rCC} = 2 ns; note 5	–	15	25	ns
t_{fC}	fall time of output signals at voltage outputs (pins 19, 16 and 13)	90% to 10% amplitude; input fall time at pin 6: t_{fCC} = 2 ns; note 5	–	6	15	ns
t_{rC}	rise time of output signals at voltage outputs (pins 19, 16 and 13)	10% to 90% amplitude; input rise time at pin 6: t_{rCC} = 2 ns; note 5	–	6	15	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain control (pin 3 for Channel 1, pin 1 for Channel 2 and pin 11 for Channel 3; note 6)						
$V_{3,1,11}$	input voltage		1.0	–	6.0	V
$V_{N3,1,11}$	input voltage for nominal gain	pins 3, 1 and 11 open-circuit	3.6	3.75	3.95	V
$R_{3,1,11}$	input resistance		44	55	66	kΩ
G_v	gain relative to nominal gain	V_6 = 4.3 V; $V_{3,1,11}$ = 6 V	2	2.6	3.3	dB
		V_6 = 4.3 V; $V_{3,1,11}$ = 1 V	–5.5	–5	–4.5	dB
Feedback input (Channel 1: pin 18, Channel 2: pin 15 and Channel 3: pin 12; note 7)						
V_{int}	internal reference voltage		5.6	5.8	6.1	V
$I_{18,15,12}$	maximum output current	during output clamping; $V_{18,15,12}$ = 3 V	–500	–100	–60	nA
ΔV_{CRT}	Δ black level at CRT	note 8	0	40	200	mV
$\Delta_T V_{int}$	variation of V_{int} in the temperature range	T_{amb} = –20 to +70 °C	0	20	50	mV
$\Delta_V V_{int}$	variation of V_{int} with supply voltage	7.2 V ≤ V_P ≤ 8.8 V	0	60	100	mV
Voltage outputs (Channel 1: pin 19, Channel 2: pin 16 and Channel 3: pin 13; note 1)						
$V_{O(b-w)}$	nominal signal output voltage (black-to-white value)	V_6 = 4.3 V; $V_{I(b-w)}$ = 0.7 V; pins 3, 1 and 11 open-circuit	0.69	0.79	0.89	V
V_{blx}	maximum adjustable black level voltage	during output clamping; T_{amb} = –20 to +70 °C	1	1.2	1.4	V
V_{blSO}	black level voltage during switch-off, equal to minimum adjustable black level voltage	V_9 = V_P; R_O = 33 Ω; T_{amb} = –20 to +70 °C	30	45	100	mV
V_{blT}	black level voltage during test mode	V_9 = V_P; V_{10} = V_P; pin 1 open-circuit; $V_{2,5,8}$ = $V_{IC2,5,8}$; note 9	0.3	0.7	1.2	V
S/N	signal-to-noise ratio	note 10	–	50	44	dB
D_{Th}	output thermal distortion	$I_{O(b-w)}$ = 50 mA; note 11	–	0.6	1	%
$\Delta_{LF} V_{bl}$	Δ black level between clamping pulses	line frequency 30 kHz	–	0.5	4.5	mV
V_{off}	maximum offset during sync clipping	$V_{2,5,8}$ < $V_{IC2,5,8}$; note 12	0	7	15	mV
$\Delta_T V_{O(b-w)}$	variation of nominal output signal (black-to-white value) with temperature	V_6 = 4.3 V; $V_{I(b-w)}$ = 0.7 V; T_{amb} = –20 to +70 °C; pins 3, 1 and 11 open-circuit	0	2.5	10	%
Current outputs (Channel 1: pin 20, Channel 2: pin 17 and Channel 3: pin 14; note 13)						
$I_{O(b-w)}$	signal current (black-to-white value)		–	50	–	mA
		with peaking	–	–	100	mA
V_{20-19}; V_{17-16}; V_{14-13}	start of HF-saturation of output transistors	I_O = 50 mA	–	–	2.0	V
		I_O = 100 mA	–	–	2.2	V
I_{blSO}	output current during switch-off	V_9 = V_P; R_O = 33 Ω	0	20	900	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Frequency response at voltage outputs (note 14)						
G_{vf}	gain decrease by frequency response at pins 19, 16 and 13	70 MHz; single channel	–	1.3	3	dB
t_{rO}	rise time at voltage output (pins 19, 16 and 13)	10% to 90% amplitude; input rise time = 1 ns	–	4.1	5.0	ns
dV_O	overshoot of output signal pulse related to actual output pulse amplitude	single channel; input rise time = 2.5 ns; $V_{I(b\text{-}w)}$ = 0.7 V; V_6 = 4.3 V; pins 3, 1 and 11 open-circuit	–	4	8	%
Crosstalk at outputs with speed up circuit (note 15)						
C_{tr}	transient crosstalk		–	–	0.1	–
Threshold voltages for clamping, blanking and switch-off (pins 9 and 10; note 16)						
V_9	threshold for horizontal blanking (blanking, output clamping)		1.2	1.4	1.6	V
	threshold for switch-off (blanking, minimum black level, no output clamping)		5.8	6.5	6.8	V
R_9	input resistance	against ground	50	80	110	kΩ
V_{10}	threshold for vertical blanking (blanking, no input clamping)	note 17	1.2	1.4	1.6	V
	threshold for clamping (input clamping, no blanking)	note 17	2.6	3.0	3.5	V
	threshold for test mode (no clamping, no blanking, for V_{blT} see above)	for test mode also $V_9 > 6.8$ V (switch-off)	$V_P - 1$	–	V_P	V
I_{10}	current	$V_{10} < V_P - 1$ V	–3	–1	–	µA
		$V_{10} \geq V_P - 1$ V	–	100	–	µA
$t_{r,f10}$	rise and fall time for clamping pulse	note 17	–	–	75	ns/V
t_{w10}	width of clamping pulse		0.6	–	–	µs

Notes to the characteristics

1. Definition of levels:

   Artificial black level: internal signal level behind input emitter follower during input clamping and signal clipping. This level is inserted instead of the input signal during blanking.

   Reference black level: DC voltage during output clamping at voltage outputs, not influenced by contrast or gain setting, adjustable by cut-off stabilization.

   Cut-off level: corresponding DC voltage at CRT cathode in closed feedback loop.

   Black level: actual signal black level at either voltage outputs or cathode. At voltage outputs the black level is equal to reference black level because there is no brightness control via TDA4884. At cathode the black level is equal to cut-off level. Brightness can be adjusted via grid 1.

   Ultra black level, switch-off level: lowest adjustable reference black level, lowest signal level at voltage outputs. The minimum guaranteed control range for reference black level is 0.1 to 1 V.
   The ultra black level is depending on the external resistor R_O at voltage outputs (pins 13, 16 and 19) to ground.

   $$V_{bISO} \approx \frac{R_O}{3.5\,k\Omega + R_O} \times 4.65\ V.$$

   Signal processing see Fig.4.

2. Linear control range is 1 to 6 V for V_6, independent from supply voltage. Open pin 6 leads to absolute maximum contrast setting. It is recommended to not exceed $V_6 = V_P - 1$ V in order to avoid saturation of internal circuitry. For $V_6 < V_{M6} \sim 0.7$ V a small negative signal (~ –40 dB) will appear. For frequency dependence of contrast control see note 14. Typical contrast characteristic see Fig.5.

3. Definition for nominal output signals: input $V_{I(b-w)} = 0.7$ V, gain pins 3, 1 and 11 open-circuit, contrast control $V_6 = V_{N6}$.

4. $$Tr = 20 \times \text{maximum of } \left| \log\left(\frac{A_1}{A_{10}} \times \frac{A_{20}}{A_2}\right)\right|; \left| \log\left(\frac{A_1}{A_{10}} \times \frac{A_{30}}{A_3}\right)\right|; \left| \log\left(\frac{A_2}{A_{20}} \times \frac{A_{30}}{A_3}\right)\right| \ [dB]$$

   A_x: signal output amplitude in Channel x at any contrast between 1 and 6 V.

   A_{x0}: signal output amplitude in Channel x at nominal contrast and same gain setting.

5. Typical step in contrast voltage and response at signal outputs for nominal input signal $V_{I(b-w)} = 0.7$ V. Typical OSD fast blanking input/output see Fig.6.

6. Linear control range is 1 to 6 V for V_3, V_1 and V_{11}, independent from supply voltage. Typical gain characteristic see Fig.7.

7. The internal reference voltage can be measured at pins 18, 15 and 12 during output clamping ($V_9 = 2$ V) in closed feedback loop. Typical variation of V_{int} with temperature and power supply voltage see Fig.8.

8. Slow variations of video supply voltage V_{CRT} (see Fig.1) will be suppressed at CRT cathode by cut-off stabilization. Change of V_{CRT} by 5 V leads to specified change of cut-off voltage.

9. The test mode allows testing without input and output clamping pulses. The signal inputs (pins 2, 5 and 8) have to be biased via resistors to the previously measured clamp voltages of approximately 3 V (artificial black level + V_{BE}). Signal blanking is not possible during test mode.

10. The signal-to-noise ratio is calculated by the formula (frequency range 1 to 70 MHz):

    $$\frac{S}{N} = 20\log\frac{\text{peak-to-peak value of the nominal signal output voltage}}{\text{RMS value of the noise output voltage}}\ [dB]$$

11. Large output swing e.g. $I_{O(b-w)} = 50$ mA leeds to signal depending power dissipation in output transistors. Thermal V_{BE} variation is compensated.

12. Composite signals will not disturb normal operations because an internal clipping circuit cuts all signal parts below black level. Typical sync clipping see Fig.9.

13. The output current approximately follows the equation $I_O = V_O\left(\frac{1}{R_O} + \frac{1}{2.2\ k\Omega}\right) - 500\ \mu A$ for $V_O > V_{bISO}$ and with

    R_O = external resistor at voltage output to ground.

    The external RC combination at pins 19, 16 and 13 (see Fig.1) enables peak currents during transients.

14. Frequency response, crosstalk and pulse response have been measured at voltage outputs in a special printed-circuit board with 50 Ω line in/out connections and without peaking (see TEST PCB). Typical frequency response see Fig.10, typical pulse response see Fig.11 and typical characteristic of contrast control versus frequency see Fig.12.

15. Crosstalk between any two output pins.

    Input conditions: One channel (Channel A) with nominal input signal and minimum rise time. The inputs of the other channels capacitively coupled to ground (Channel B). Gain pins 3, 1 and 11 open-circuit.

    Output conditions: Output signal of Channel A controlled by contrast setting (pin 6) to $V_{O(b-w)} = V_A = 0.7$ V, the rise time should be 5 ns. Output signal of Channel B then is $V_{O(b-w)} = V_B$.

    Transient crosstalk: $C_{tr} = \frac{V_B}{V_A}$.

    Crosstalk versus frequency has been measured without peaking circuit, with nominal input signal and nominal settings. Typical frequency dependent crosstalk between channels see Figs 13, 14 and 15.

16. The internal threshold voltages are derived from a stabilized voltage. The internal pulses are generated while the input pulses are higher than the thresholds. Voltages of less than –0.1 V at pins 9 and 10 can influence black level control and should be avoided.

17. For 75 ns/V < t_{rf10} < 240 ns/V generation of internal input clamping and blanking pulse is not defined. Any pulses not exceeding the threshold of input clamping (typical 3 V) will be detected as blanking pulse. Timing of pulses at pin 10 see Fig.16.

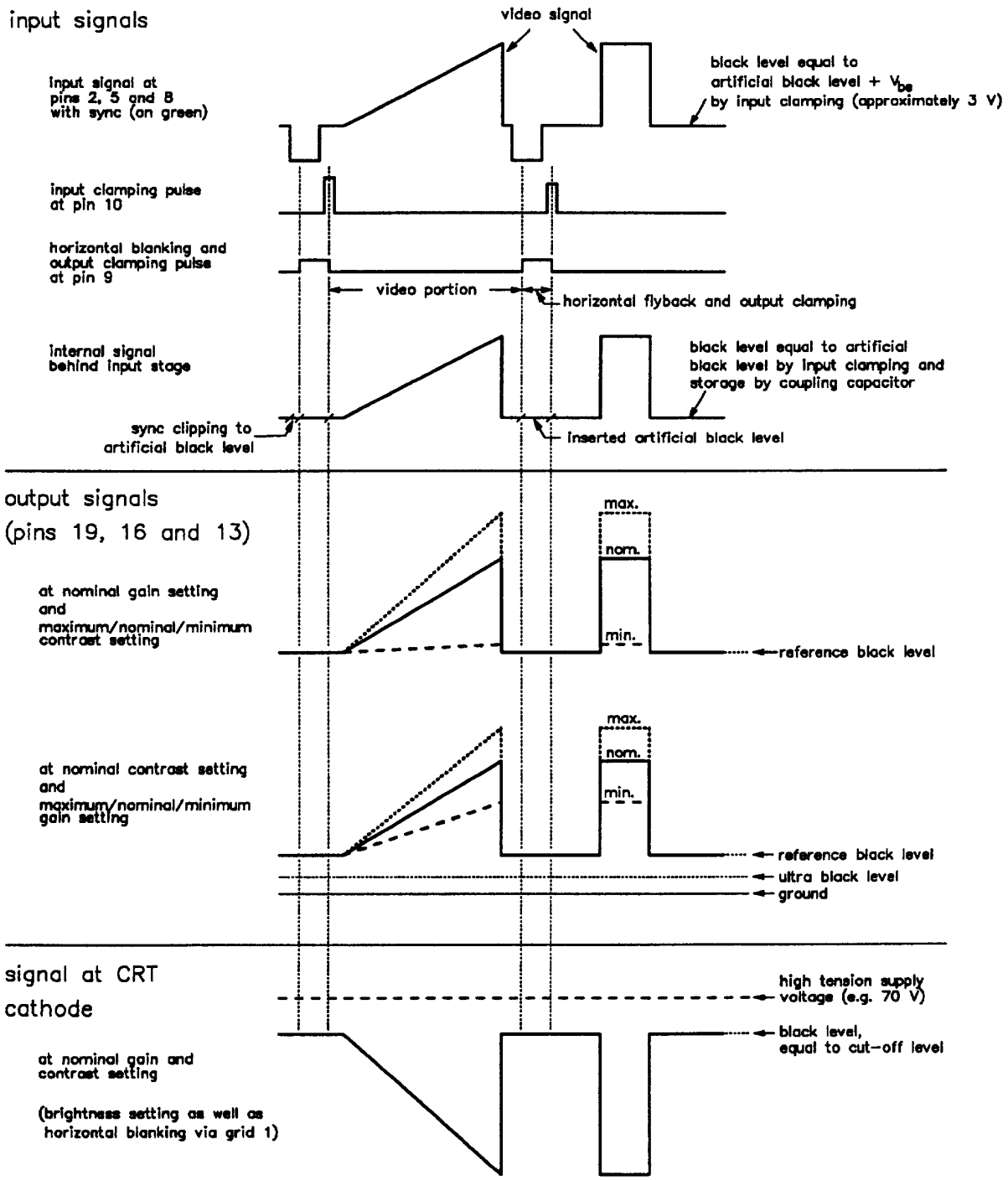


Fig.4 Signal processing.

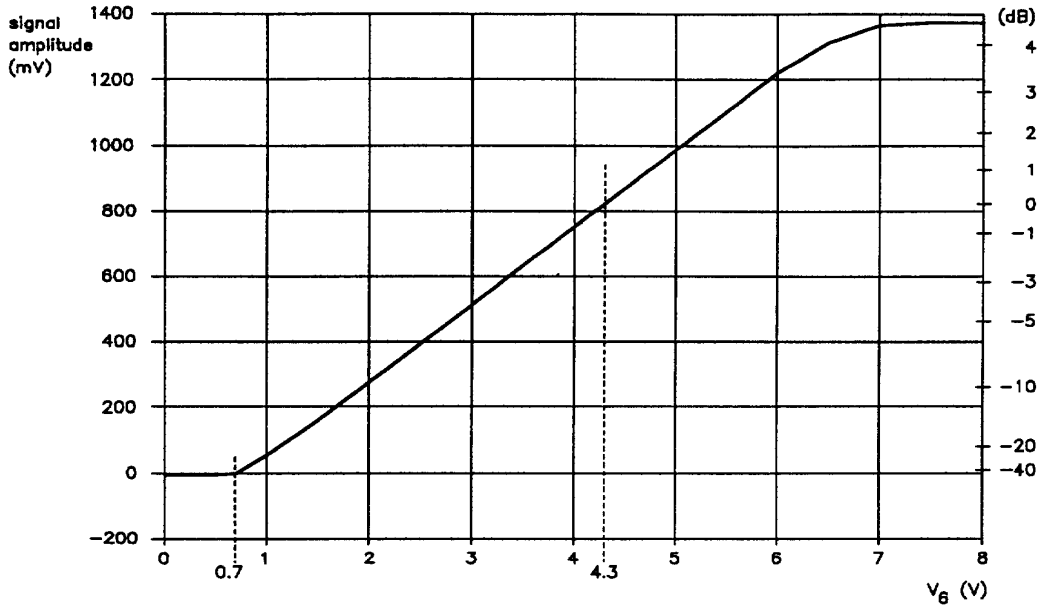


Fig.5 Typical contrast characteristic.

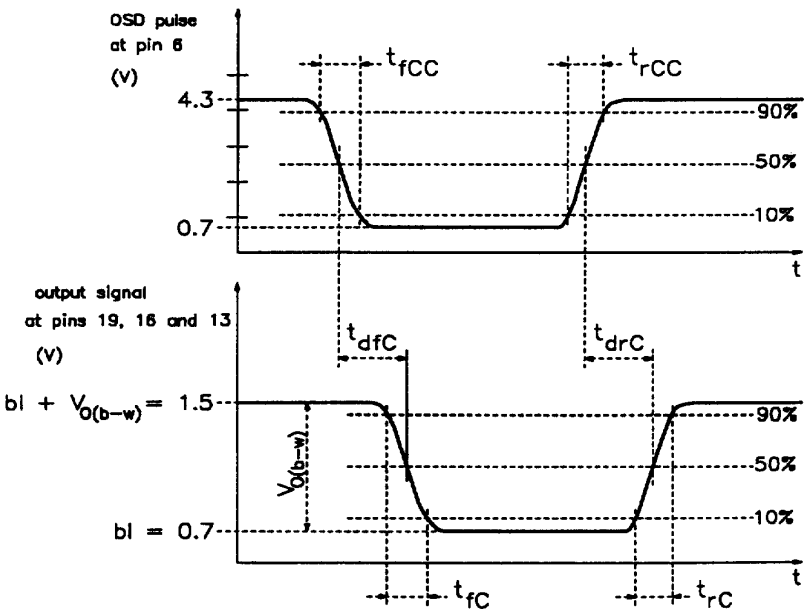


Fig.6 Typical OSD fast blanking input/output.

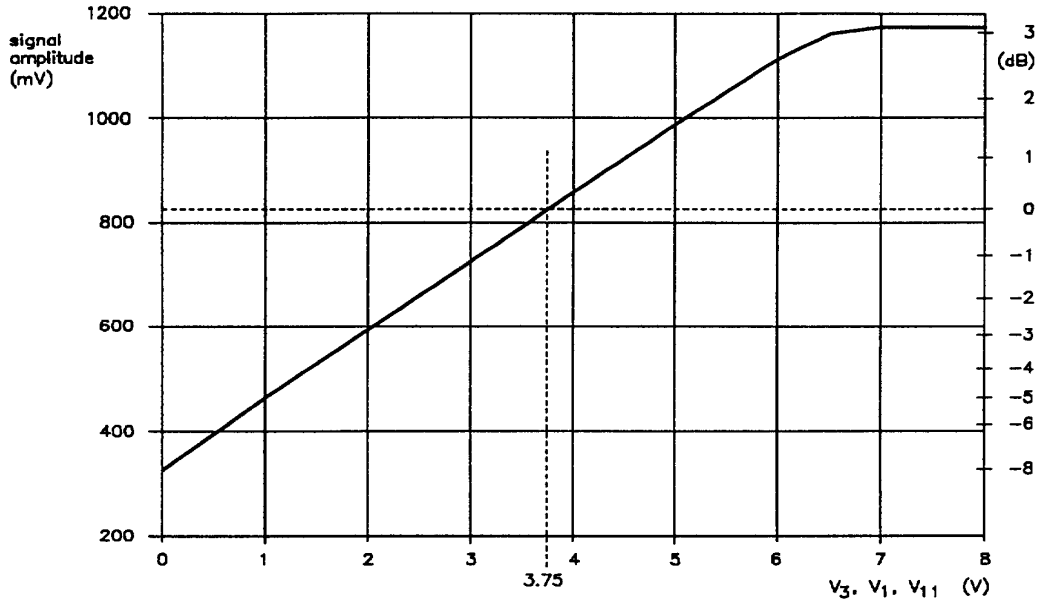


Fig.7 Typical gain characteristic.

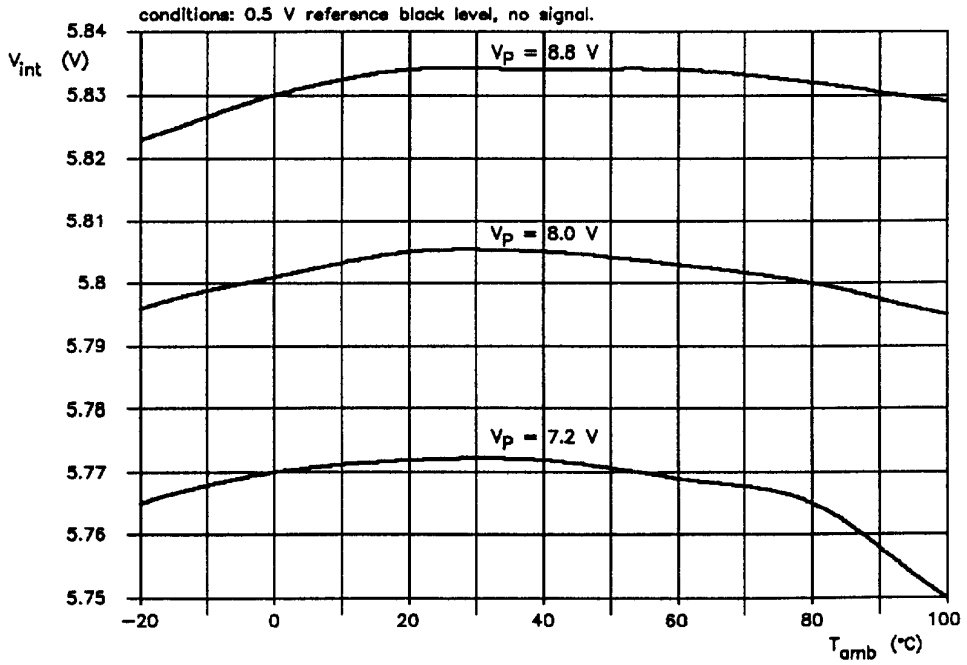


Fig.8 Typical variation of V_{int} with temperature and power supply voltage.

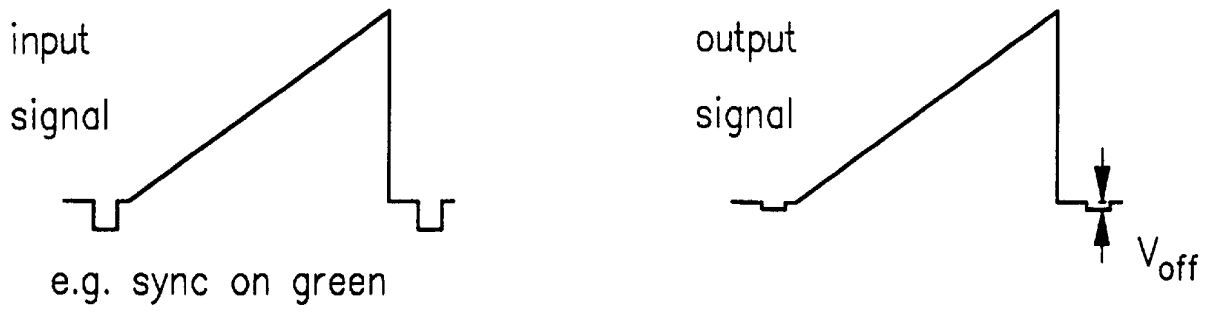


Fig.9 Typical sync clipping.

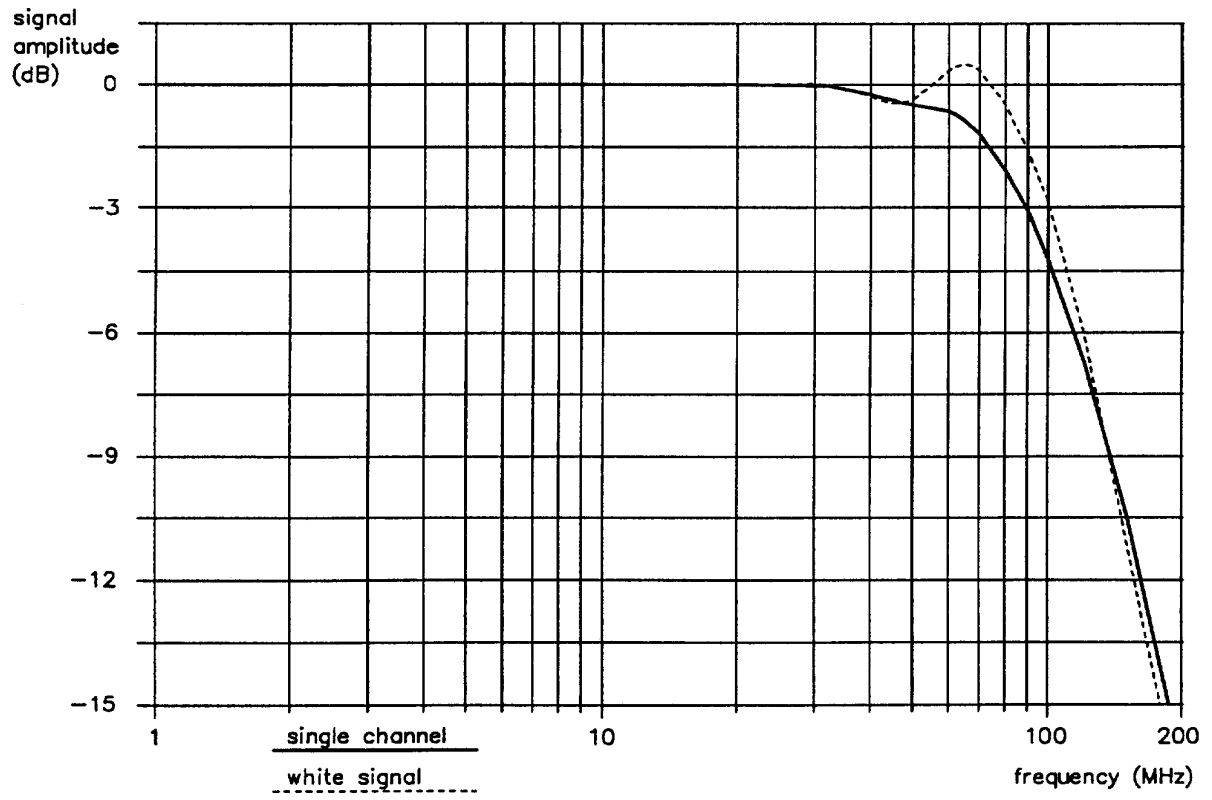


Fig.10 Typical frequency response.

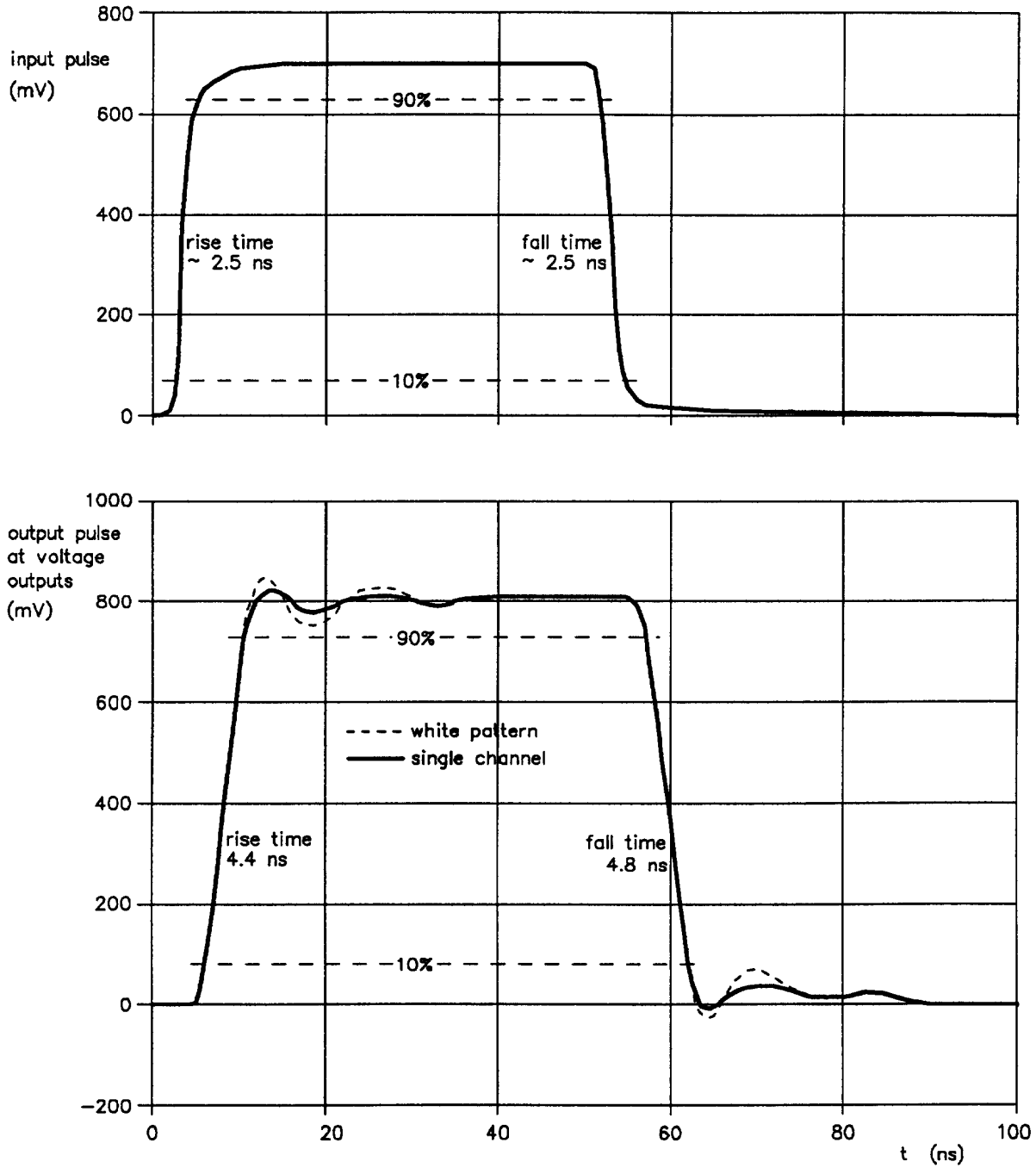


Fig.11 Typical pulse response.

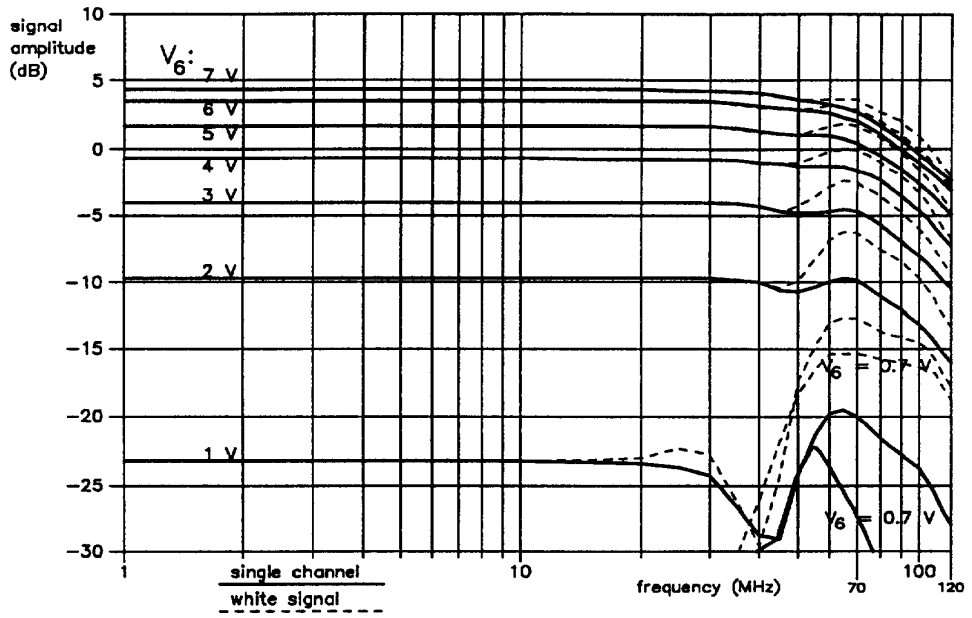


Fig.12 Typical characteristic of contrast control versus frequency.

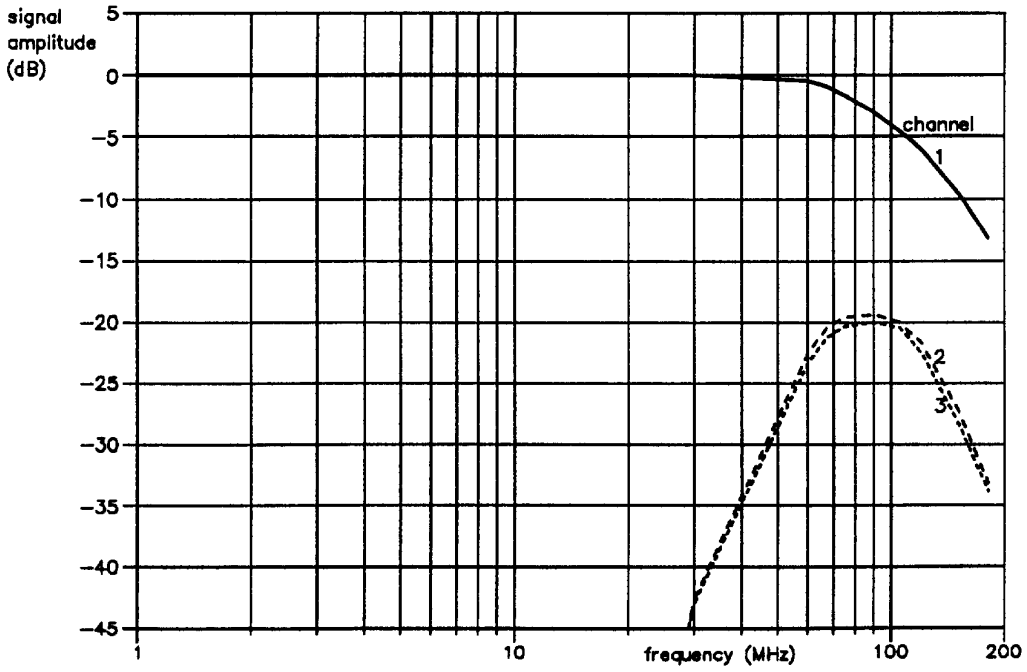


Fig.13 Typical crosstalk: Channel 1 → 2 and 3.

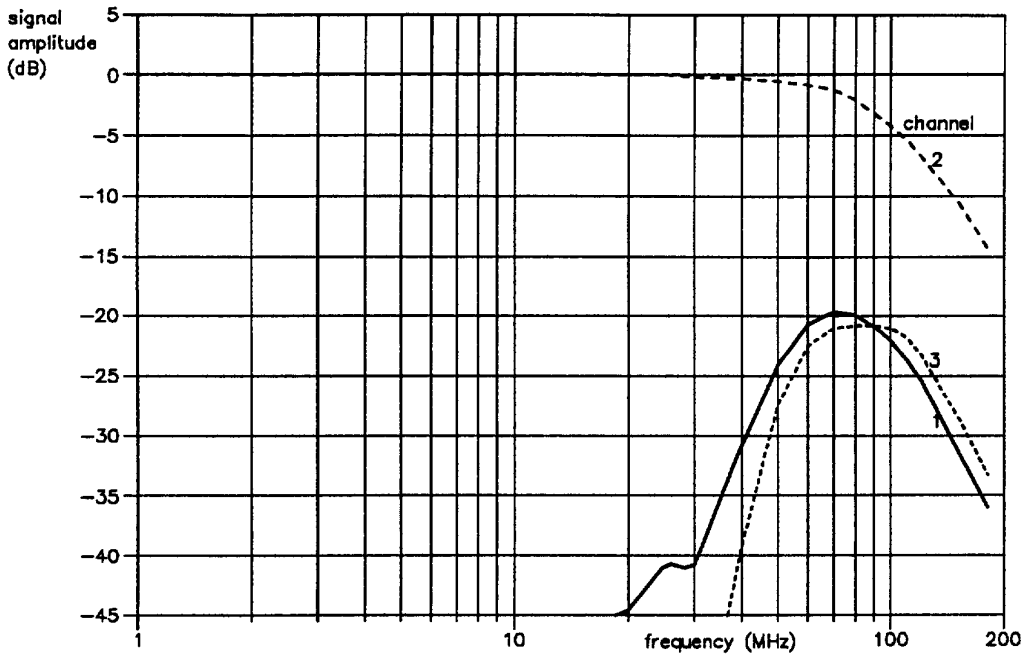


Fig.14 Typical crosstalk: Channel 2 → 1 and 3.

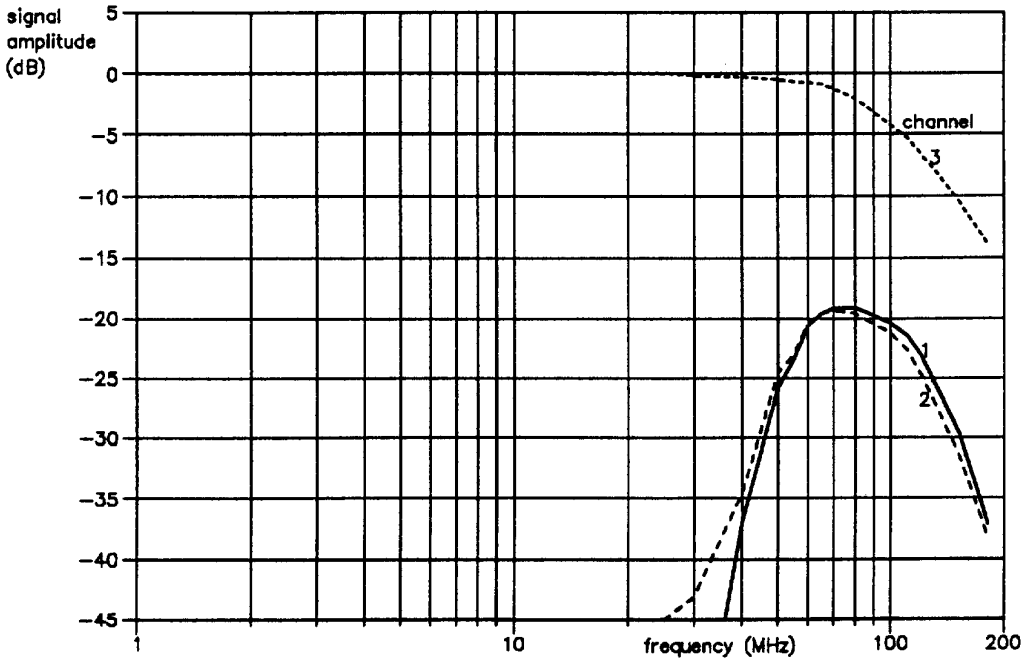


Fig.15 Typical crosstalk: Channel 3 → 1 and 2.

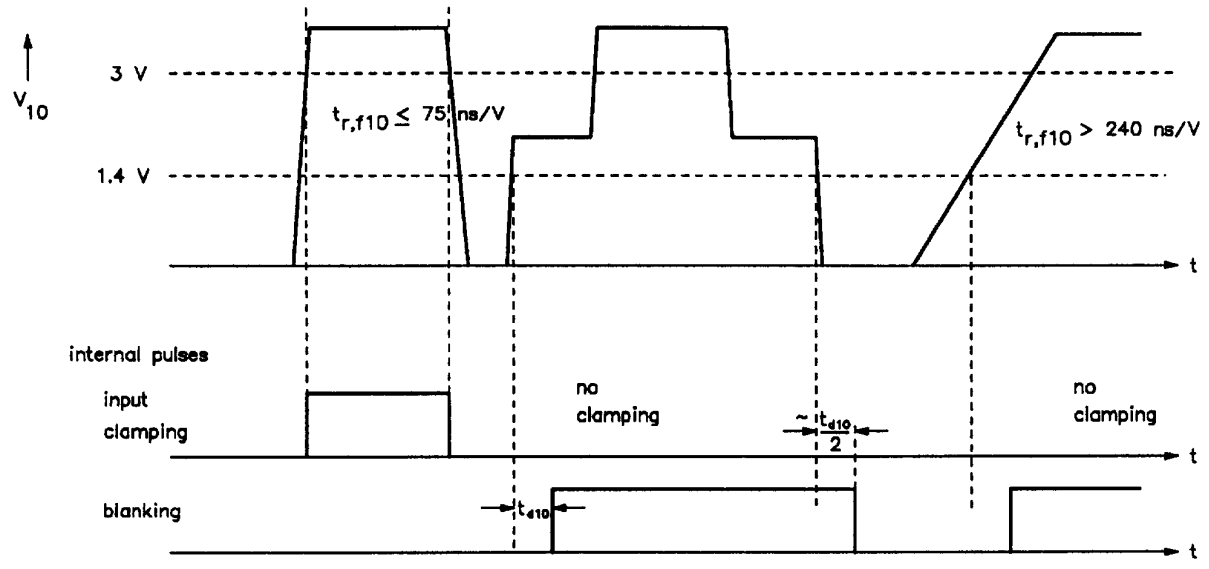


Fig.16 Timing of pulses at pin 10.

TEST PCB

For high frequency measurements a special application and printed-circuit board with only a few external components is built. Fig.17 shows the application circuit and Fig.18 the layout of the double sided printed board. All components on the rear (below) are of SMD type as well as R13, R14 and R15 on the front. Short HF loops and minimum crosstalk between the channels as well as input and output are achieved by properly shaped ground areas star connected to the IC ground pin.

The HF input signals can be fed to the subclick connectors X1, X2 and X3 by a 50 Ω line. The line is then terminated by a 51 Ω resistor on the board. With choice of jumper connections (JA1, JA2 and JA3) it is possible to connect channel inputs to its input connector, to connect all channels to one input connector (white pattern) and to ground each input via the coupling capacitor.

For operation without input clamping (e.g. test mode) the DC bias can be provided by VIDC (connector X21) if a short at JA4, JA5 and JA6 is made (solder short or small SMD resistor).

The output signal can be monitored via 50 Ω terminated lines at the voltage outputs (subclick connectors X4, X5 and X6). With 100 Ω in parallel to the 50 Ω terminated line the effective load resistance at the voltage outputs is 33 Ω. The mismatch seen from the line towards the IC has no significant effect if the line is match terminated. A peaking circuit (C15, R16 Channel 1) can be added for realistic loading of the voltage outputs.

Black level adjustment is done by VIOS, UFBX (connector X21) and resistors R19, R22 and R25 (Channel 1). If R19 is equal to the effective load resistor at the voltage output the reference black level is approximately

$$U_{REF} = VIOS - V(I01) \text{ and}$$

$$V(I01) = V_{int} + (V_{int} - UFBX) \times \frac{R22}{R25}.$$

V_{int} is the internal reference voltage at the feedback input (typical 5.8 V). By this it is possible to adjust the reference black level and the voltage at the current outputs independently.

DC control for contrast and gain is prepared at connectors X21 and X22. Contrast control can also be set by the potentiometer P1 (jumper JA11). The series resistor R11 is necessary if fast OSD switching is activated via 50 Ω line (X10), a line termination can be done at the connector X9. Clamping and blanking pulses are fed to the IC via connectors X7 and X8. Connector X23 is used for power supply. The capacitors C7 and C8 should be located as near as possible to the IC pins.

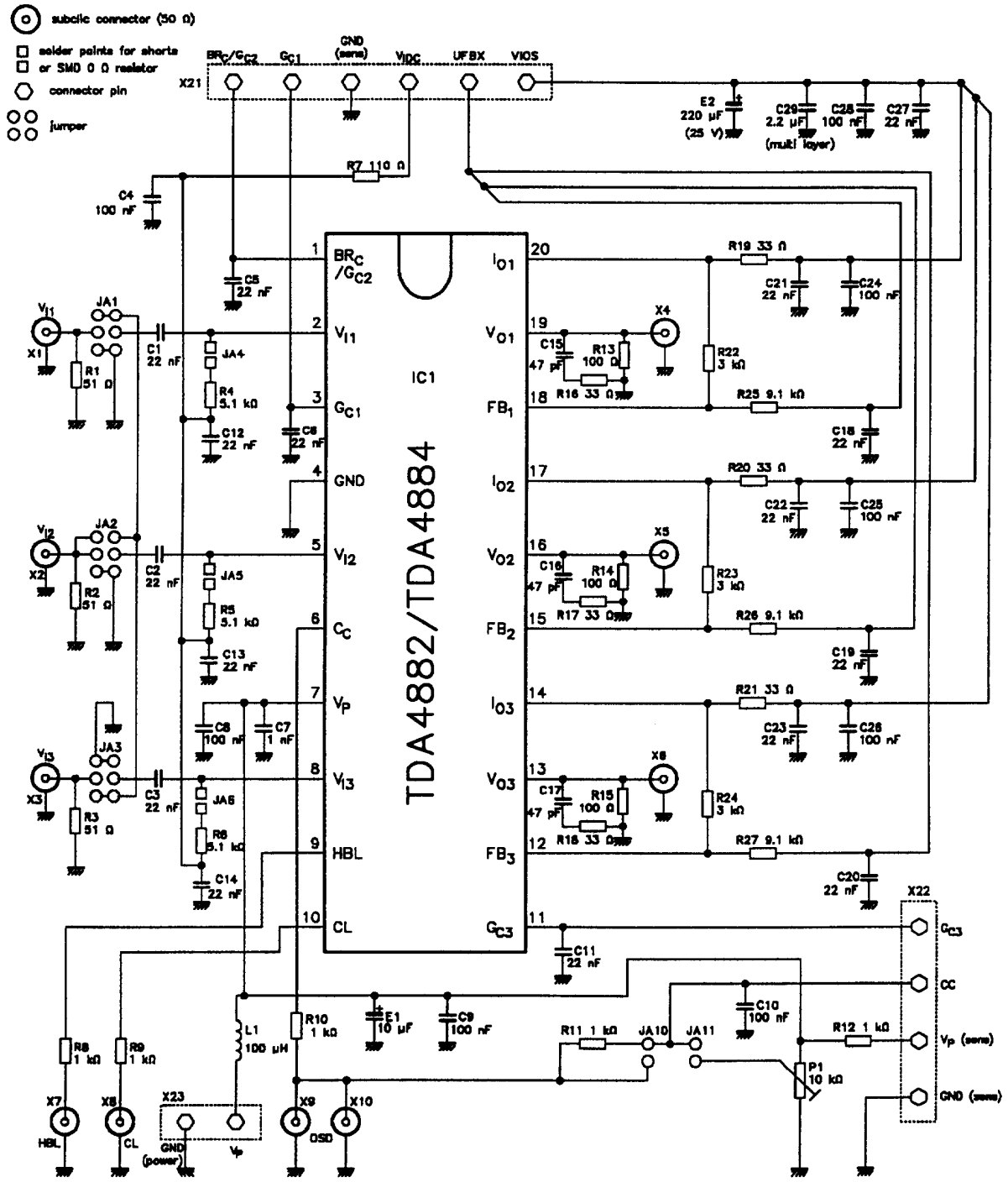


Fig.17 Application circuit for test PCB.

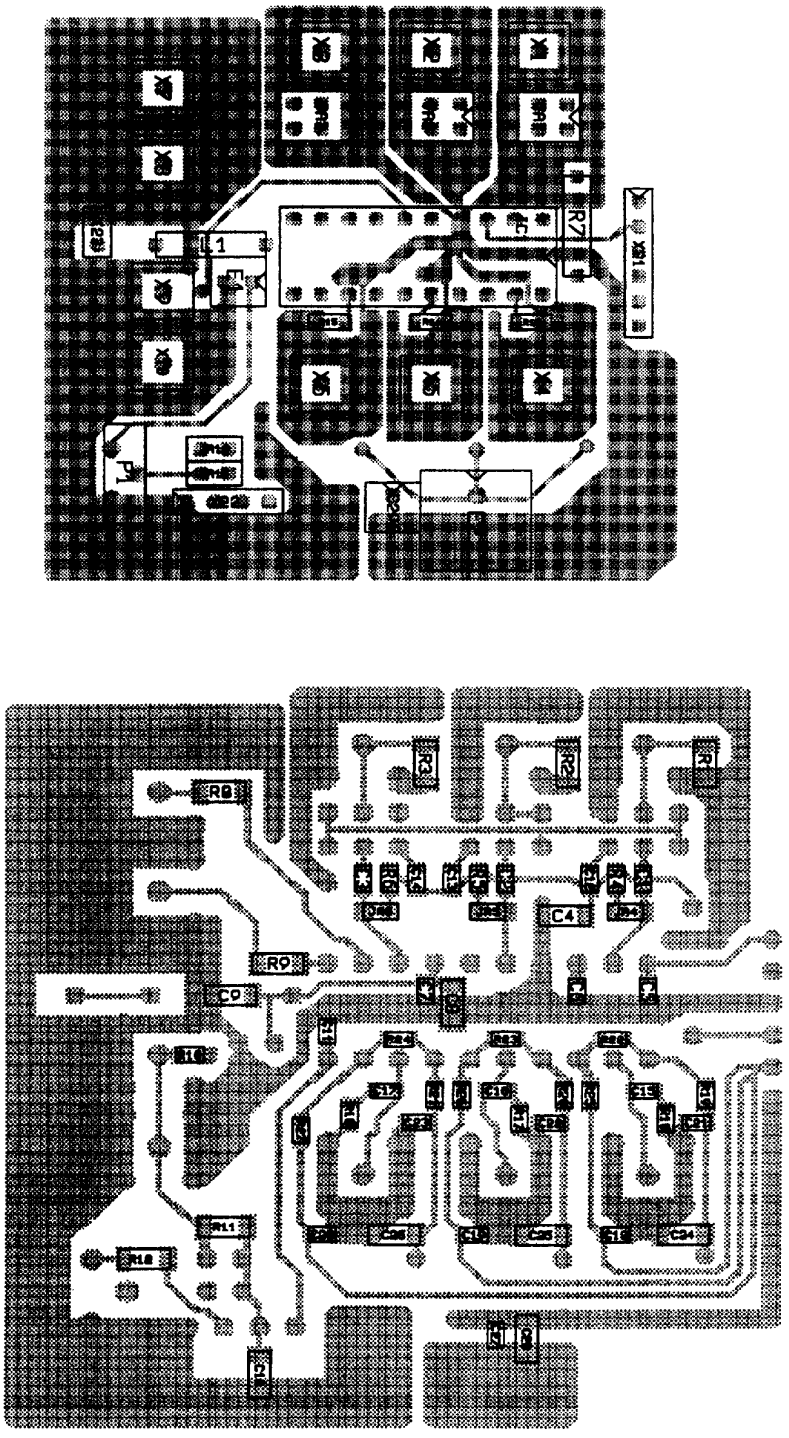


Fig.18 Double sided test PCB layout.

RECOMMENDATIONS FOR BUILDING THE APPLICATION BOARD

General

- Double sided board
- Short HF loops by large ground plane on the rear .

Voltage outputs

- Capacitive loads as small as possible
- Short interconnection via resistor to ground.

Supply voltage

- Capacitors as near as possible to the pins
- Use of high frequency capacitors (low self inductance, e.g. SMD).

Current outputs, emitter of cascode transistors

- The external interconnection inductivity can build a resonance together with the internal substrate capacity, a damping resistor of some 10 Ω near to the IC pin can suppress such oscillations.

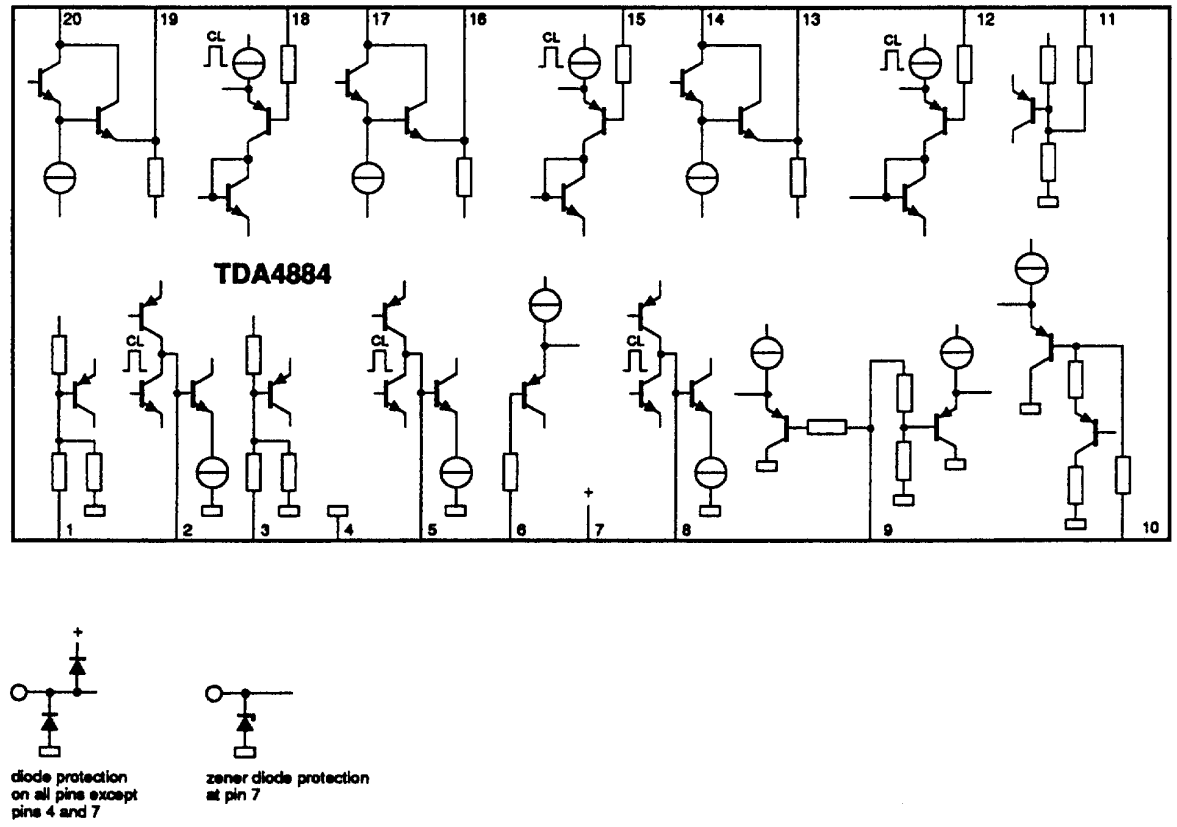
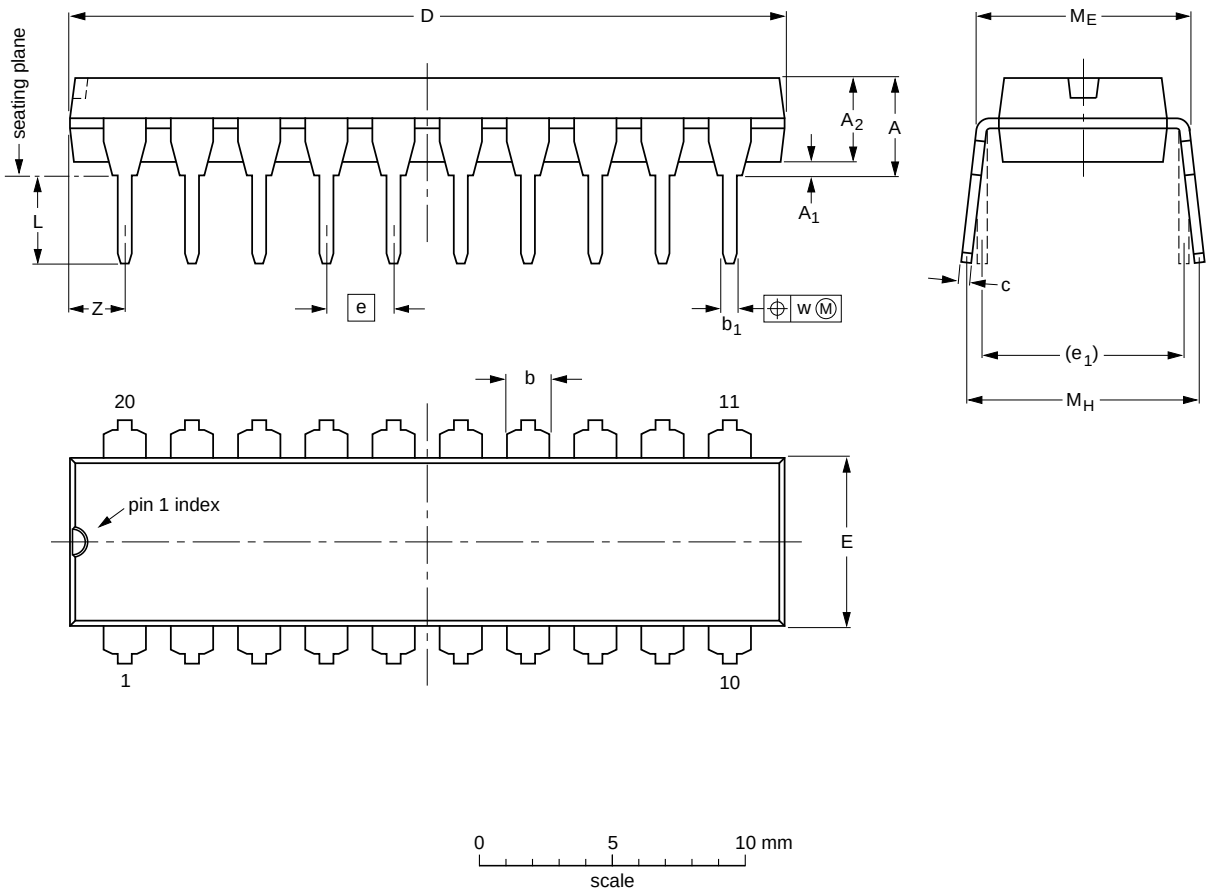


Fig.19 Internal circuits.

PACKAGE OUTLINE

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.