DATA SHEET

TDA4780
RGB video processor with automatic cut-off control and gamma adjust

Preliminary specification
File under Integrated Circuits, IC02

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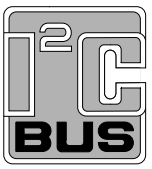
TDA4780

FEATURES



- Gamma adjust
- Dynamic black control (adaptive black)
- All input signals clamped on black-levels
- Automatic cut-off control, alternative: output clamping on fixed levels
- Three adjustable reference voltage levels via I²C-bus for automatic cut-off control
- Luminance/colour difference interface
- Two luminance input levels allowed
- Two RGB interfaces controlled by either fast switches or by I²C-bus
- Two peak drive limiters, selection via I²C-bus
- Blue stretch, selection via I²C-bus
- Luminance output for scan velocity modulation (SCAVEM)
- Extra luminance output; same pin can be used as hue control output e.g. for the TDA4650 and TDA4655
- Non standard operations like 50 Hz/32 kHz are also possible
- Either 2 or 3 level sandcastle pulse applicable
- High bandwidth for 32 kHz application
- White point adjusts via I²C-bus
- Average beam current and improved peak drive limiting
- Two switch-on delays to prevent discolouration during start-up
- All functions and features programmable via I²C-bus
- PAL/SECAM or NTSC matrix selection.

GENERAL DESCRIPTION

The TDA4780 is a monolithic integrated circuit with a luminance and a colour difference interface for video processing in TV receivers. Its primary function is to process the luminance and colour difference signals from a colour decoder which is equipped e.g. with the multistandard decoder TDA4655 or TDA9160 plus delay line TDA4661 or TDA4665 and the Picture Signal Improvement (PSI) IC TDA467x or from a Feature Module. *(continued)*

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)	7.2	8.0	8.8	V
I_P	supply current (pin 5)	80	100	120	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value) (C)VBS	–	0.45/ 1.43	–	V
$V_{6(p-p)}$	−(B−Y) input (peak-to-peak value)	–	1.33	–	V
$V_{7(p-p)}$	−(R−Y) input (peak-to-peak value)	–	1.05	–	V
V_{14}	three-level sandcastle pulse				
	H+V	–	2.5	–	V
	H	–	4.5	–	V
	BK	–	8.0	–	V
	two-level sandcastle pulse				
	H+V	–	2.5	–	V
	BK	–	4.5	–	V
V_i	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (black-to-white value)	–	0.7	–	V
$V_{O(p-p)}$	RGB output at pins 24, 22 and 20 (black-to-white value)	–	2.0	–	V
T_{amb}	operating ambient temperature	−20	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4780	28	DIL	plastic	SOT117(1)

Note

1. SOT117-1; 1996 December 9.

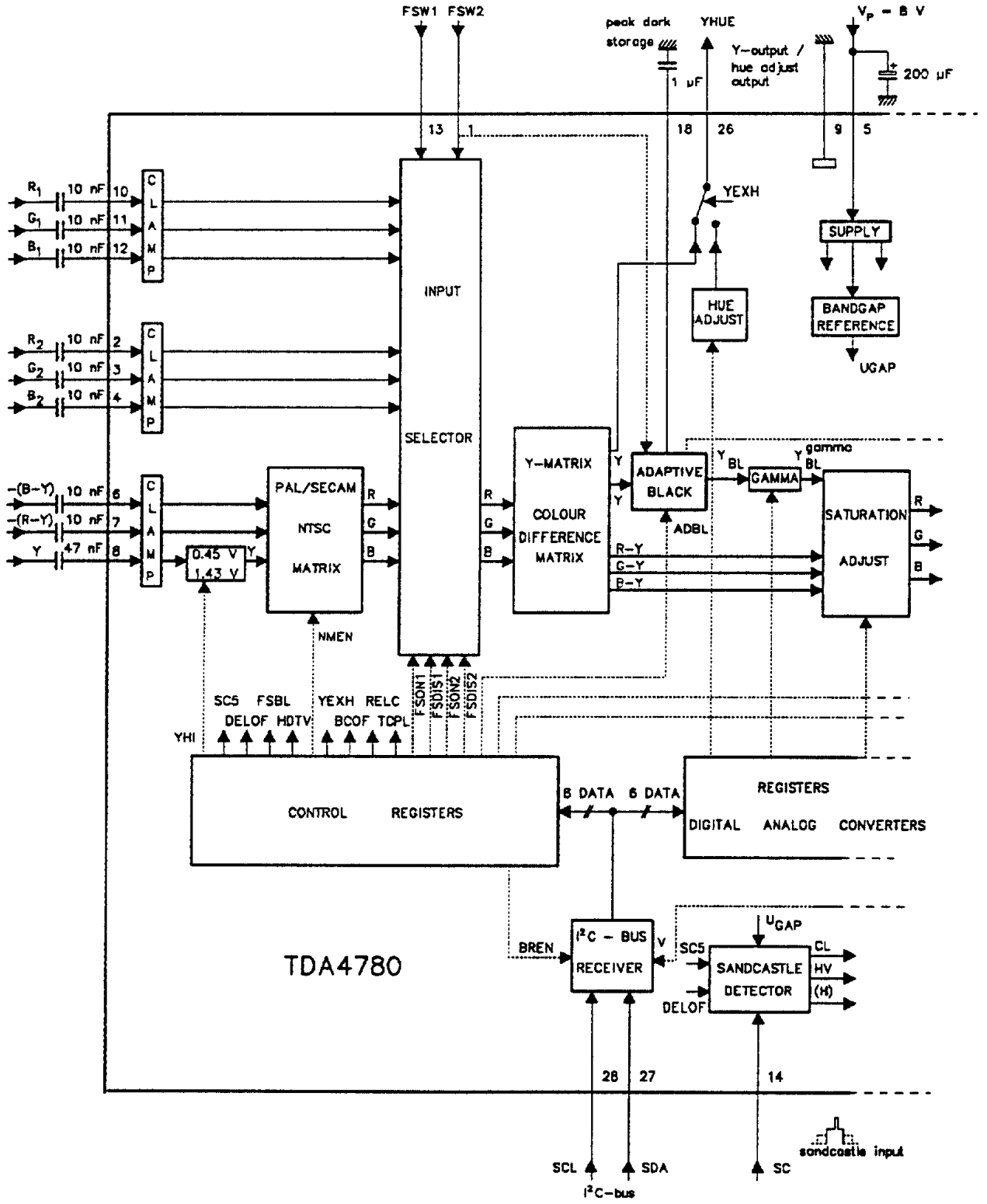


Fig.1 Block diagram (continued in Fig.2)

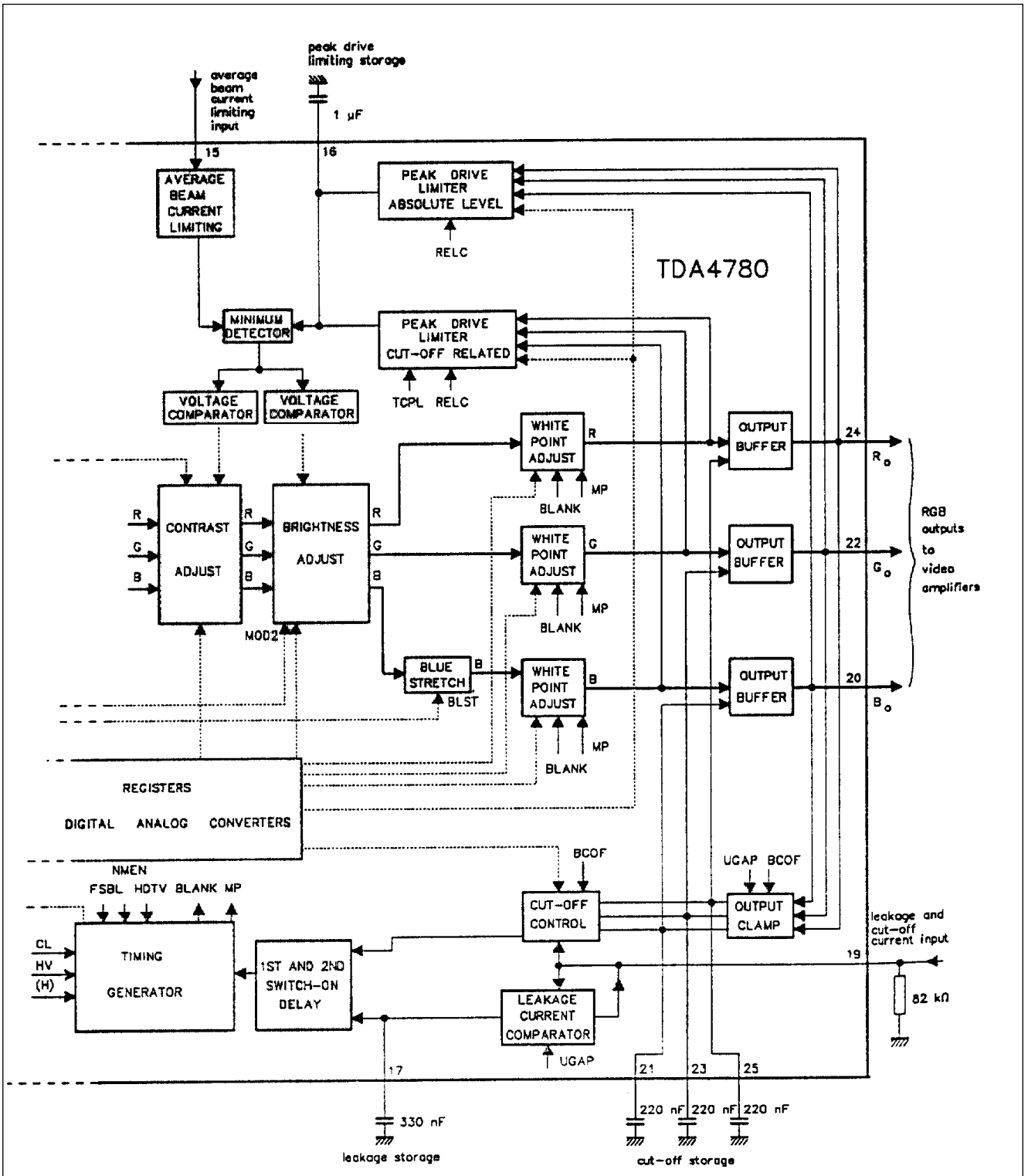


Fig.2 Block diagram (continued from Fig.1)

PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
–(B–Y)	6	colour difference input –(B–Y)
–(R–Y)	7	colour difference input –(R–Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak limiting
C_L	17	storage capacitor for leakage current compensation
C_{PDST}	18	storage capacitor for peak dark
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
YHUE	26	Y-output/hue adjust output
SDA	27	I^2C-bus serial data input/acknowledge output
SCL	28	I^2C-bus serial clock input

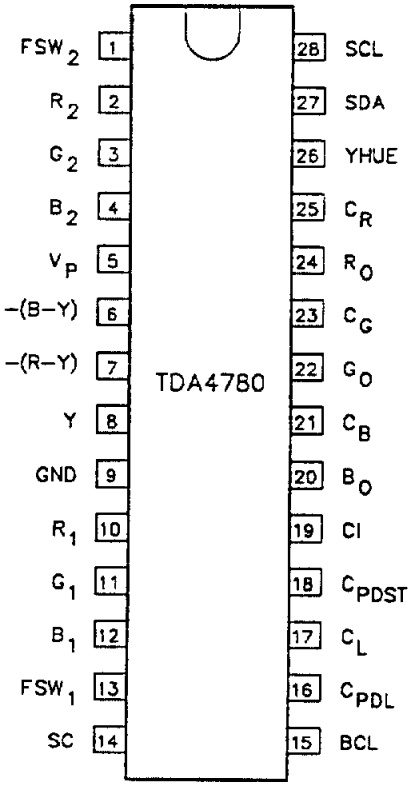


Fig.3 Pin configuration.

GENERAL DESCRIPTION

(continued)

The required input signals are:

- luminance and negative colour difference signals
- 2- or 3-level sandcastle pulse for internal timing pulse generation
- I²C-bus data and clock signals

Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector (SCART plug) and the other one from an on-screen display (OSD) generator. The TDA4780 has I²C-bus control of all parameters and functions with automatic cut-off control of the picture tube cathode currents. It provides RGB output signals for the video output stages. In clamped output mode it can also be used as an RGB source.
The main differences to the sister type TDA4680 are:

- additional features, namely gamma adjust, adaptive black, blue stretch and two different peak drive limiters.
- the measurement lines are triggered by the trailing edge of the vertical component of the sandcastle pulse.
- I²C-bus receiver only. Automatic white level control is not provided; the white levels are determined directly by the I²C-bus data.
- the TDA4780 is pin compatible (except pin 18) to the TDA4680. The slave address via the I²C-bus can be used for both ICs; where a function is not included in the TDA4680 then the I²C-bus command is not executed. Special commands (except control bit FSWL) for the TDA4680 will be ignored by the TDA4780.

FUNCTIONAL DESCRIPTION

Signal input stages

The TDA4780 contains 3 sets of input signal stages for:
a) Luminance/colour-difference signals: (Y: 0.45 V(p-p) VBS or 1.43 V(p-p) VBS, selectable via I²C-bus, −(R−Y): 1.05 V(p-p); −(B−Y): 1.33 V(p-p)). The capacitively coupled signals are matrixed to RGB signals by either a PAL/SECAM or NTSC matrix (selected via I²C-bus).
b) $(RGB)_1$ signals (0.7 V(p-p) VB), capacitively coupled (e.g. from external source).
c) $(RGB)_2$ signals (0.7 V(p-p) VB), capacitively coupled (e.g. videotext, OSD).
All input signals are clamped in order to have the same black levels at the signal switch input. Displayed signals must be synchronous with the sandcastle pulse.

Signal switches

Both fast signal switches can be operated by switching pins (e.g. SCART facilities) or set via the I²C-bus. By switch 1 the Y-CD signals or the $(RGB)_1$ signals can be selected, by switch 2 the above selected signals or the $(RGB)_2$ signals are enabled. During the vertical and horizontal blanking time an artificial black level equal to the clamped black level is inserted in order to clip off the sync pulse of the luminance signal and to suppress hum during the cut-off measurement time and eliminate noise during these intervals.

Saturation, gamma, contrast and brightness adjust

Saturation, contrast and brightness adjusts are adjusted via the I²C-bus and act on Y, CD as well as on RGB input signals. Gamma acts on the luminance content of the input signals.

Gamma adjust

The gamma adjust stage has a non-linear transmission characteristic according to the formula $y = x^{gamma}$, where x represents the input and y the output signal. If gamma is smaller than unity, the lower parts of the signal are amplified with higher gain.

Adaptive black (ADBL)

The adaptive black stage detects the lowest voltage of the luminance component of the internal RGB signals during the scanning time and shifts it to the nominal black level. In order to keep the nominal white level the contrast is increased simultaneously.

Blue stretch (BLST)

The blue stretch channel gets additional amplification if the blue signal is greater than 80% of the nominal signal amplitude. In that case the white point is shifted towards higher colour temperature so that white parts of a picture seem to be brighter.

Measurement pulse and blanking stage

During the vertical and horizontal blanking time and the measurement period the signals are blanked to an ultra black level, so the leakage current of the picture tube can be measured and automatically compensated for.
During the cut-off measurement lines (one line period for each R, G or B) the output signal levels are at cut-off measurement level.
The vertical blanking period is timed by the sandcastle pulse. The measurement pulses (leakage, R, G and B) are triggered by the negative going edge of the vertical pulse of the sandcastle pulse and start after the following horizontal pulse.
The IC is prepared for $2f_H$ (32 kHz) application.

Output amplifier and white adjust potentiometer

The RGB signals are amplified to nominal 2 V(p-p), the DC-levels are shifted according to cut-off control.
The nominal signal amplitude can be varied by ±50% by the white point adjustment via the I²C-bus (individually for RGB respect).

Automatic cut-off control

During leakage measurement time the leakage current is compensated in order to get a reference voltage at the cut-off measurement info pin.
This compensation value is stored in an external capacitor.
During cut-off current measurement times for the R, G and B channels, the voltage at this pin is compared with the reference voltage, which is individually adjustable via I²C-bus for each colour channel. The so derived control voltages are stored in the external feedback capacitors. Shift stages add these voltages to the corresponding output signals.
The automatic cut-off control may be disabled via the I²C-bus. In this mode the output voltage is clamped to 2.5 V. Clamping periods are the same as the cut-off measurement periods.

Signal limiting

The TDA4780 provides two kinds of signal limiting. First, an average beam limiting, that reduces signal level if a certain average is exceeded. Second, a peak drive limiting, that is activated if one of the RGB signals even shortly exceeds a via I²C-bus adjusted threshold. The latter can be either referred to the cut-off measurement level of the outputs or to ground.
When signal limiting occurs, contrast is reduced, and at minimum contrast brightness is reduced additionally.

Sandcastle decoder and timer

A 3-level detector separates the sandcastle pulse into combined line and field pulses, line pulses, and clamping pulses. The timer contains a line counter and controls the cut-off control measurement. Application with a 2-level 5 V sandcastle pulse is possible.

Switch on delay circuit

After switch on all signals are blanked and a warm up test pulse is fed to the outputs during the cut-off measurement lines. If the voltage at the cut-off measurement input exceeds an internal level the cut-off control is enabled but the signal remains still blanked. The signal blanking is finished when the cut-off control has stabilized. In case of output clamping, the cut-off control is disabled and the switch on procedure will be skipped.

Y output and hue adjust

The TDA4780 contains a D/A converter for hue adjust. The analog information can be fed, e.g. to the multistandard decoder TDA4650 or TDA4655. This output pin may be switched to a Y output signal, which can be used for scan velocity modulation (SCAVEM). The Y output is the Y input signal or the matrixed (RGB) input signal according to the switch position of fast switch.

I²C-bus

The TDA4780 contains an I²C-bus receiver for control function.

ESD protection

Pins are provided with protection diodes against ground and supply voltage (see pin description).
I²C-bus input pins do not shunt the I²C-bus signals in case of missing supply voltage.

EMC

Pins are protected against electromagnetic radiation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{stg}	storage temperature	–20	+150	°C
T_{amb}	operating ambient temperature	–20	+70	°C
P_{tot}	total power dissipation	–	1200	mW
$V_{5-9} = V_P$	supply voltage	–0.1	+9.0	V
$V_{10,11,12-9}$	$(RGB)_1$ inputs	–0.1	V_P	V
$V_{2,3,4-9}$	$(RGB)_2$ inputs	–0.1	V_P	V
$V_{8,7,6-9}$	Y, CD-inputs	–0.1	V_P	V
$V_{13,1-9}$	switch I, II	–0.1	V_P	V
$V_{25,23,21,17-9}$	black level, leakage storage	–0.1	V_P	V
V_{14-9}	sandcastle	–0.7	$V_P + 5.8$	V
V_{15-9}	average current inf.	–0.7	$V_P + 0.7$	V
V_{16-9}	peak drive storage	–0.1	V_P	V
$V_{27,28-9}$	I^2C-bus	–0.1	V_P	V
I_{26}	Y output / hue adjust	–8	–	mA
V_{18-9}	peak dark storage	–0.1	V_P	V
V_{19-9}	cut-off control input	–0.7	$V_P + 0.7$	V
$I_{24,22,20}$	output peak	–20	–	mA
$I_{24,22,20}$	output average	–10	–	mA
ESD	electrostatic handling (note 1) for all pins	–500	+500	V

Note to the Limiting Values

1. Charge device model class A: discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	47 K/W

QUALITY SPECIFICATION

URV-4-2-59/601

CHARACTERISTICS

T_{amb} = +25 °C; V_P = 8 V; V_{nom}: nominal signal amplitude (black-white) 2000 mV (peak-to-peak value) at output pins; gamma = 1; adaptive black inactive; brightness, contrast, saturation and white balance at nominal settings; no beam current or peak drive limiting; all voltages are related to ground (pin 9) and measured in Figs 1 and 2; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)		7.2	8	8.8	V
I_P	supply current (pin 5)		–	100	120	mA
Colour-difference inputs (–(B–Y): pin 6, –(R–Y): pin 7; capacitively coupled to a low ohmic source; recommendation: maximum 600 Ω)						
V_6	–(B–Y) signal (peak-to-peak value)	75% colour bar signal	–	1.33	–	V
$V_{6,7}$	internal bias during clamping		–	4.0	–	V
$I_{6,7}$	DC input current between clamping pulses		–	–	0.1	µA
$I_{6,7}$	maximum input current during clamping		100	180	260	µA
V_7	–(R–Y) signal (peak-to-peak value)	75% colour bar signal	–	1.05	–	V
$R_{6,7}$	AC input resistance		10.0	–	–	MΩ
Y input (pin 8; capacitively coupled to a low ohmic source; recommendation: maximum 600 Ω)						
V_8	input signal (composite signal; VBS; peak-to-peak value)	adaption to two different signal levels via control bit YHI				
		YHI = 0	–	0.45	–	V
		YHI = 1	–	1.43	–	V
R_8	AC input resistance		10.0	–	–	MΩ
V_8	internal bias during clamping	YHI = 0	–	3.7	–	V
		YHI = 1	–	4.6	–	V
I_8	DC input current between clamping pulses		–	–	0.1	µA
I_8	maximum input current during clamping		100	180	260	µA
RGB input 1 (R_1: pin 10, G_1: pin 11, B_1: pin 12; capacitively coupled to a low ohmic source; recommendation: maximum 600 Ω; note 1)						
$V_{10,11,12}$	input signal (peak-to-peak value)		–	0.7	–	V
$R_{10,11,12}$	AC input resistance		10.0	–	–	MΩ
$V_{10,11,12}$	internal bias during clamping		–	5.1	–	V
$I_{10,11,12}$	DC input current between clamping pulses		–	–	0.1	µA
$I_{10,11,12}$	maximum input current during clamping		100	180	260	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB input 2 (R_2: pin 2, G_2: pin 3, B_2: pin 4; capacitively coupled to a low ohmic source; recommendation: maximum 600 Ω; note 1)						
$V_{2,3,4}$	input signal (peak-to-peak value)		–	0.7	–	V
$R_{2,3,4}$	AC input resistance		10.0	–	–	MΩ
$V_{2,3,4}$	internal bias during clamping		–	5.1	–	V
$I_{2,3,4}$	DC input current between clamping pulses		–	–	0.1	μA
$I_{2,3,4}$	maximum input current during clamping		100	180	260	μA
PAL/SECAM and NTSC matrix (note 2; for demodulation axis see appendix)						
PAL/SECAM matrix		control bit NMEN = 0				
NTSC matrix		control bit NMEN = 1; hue position set on (–2) degrees				
Fast signal switches and blanking (fast signal switch 1 (pin 13); Y, CD / R_1, G_1; B_1; control bits FSDIS1, FSON1)						
V_{13}	voltage to select Y and CD		–	0	0.4	V
V_{13}	voltage range to select R_1, G_1 and B_1		0.9	1.0	5.5	V
R_{13}	internal resistor to ground		3.3	3.8	4.8	kΩ
Crosstalk (see Table 2)						
$t_s - t_i$	difference between transit times for signal switching and signal insertion		–	–	10	ns
Fast signal switch 2 (pin 1; Y, CD or R_1, G_1, B_1 / R_2, G_2, B_2; control bits FSDIS2, FSON2)						
V_1	voltage to select Y and CD / R_1, G_1 and B_1		–	0	0.4	V
V_1	voltage range to select R_2, G_2 and B_2		0.9	1.0	5.5	V
V_1	required minimal voltage to switch off the ADBL measurement		–	0.87	1.0	V
R_1	internal resistor to ground	$R_1 > R_{13}$	2.8	4.2	6.0	kΩ
Crosstalk (see Table 2)						
$t_s - t_i$	difference between transit times for signal switching and signal insertion		–	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Adjust stages (adaptive black, gamma, contrast, saturation, brightness and white point adjust, blue stretch)						
Adaptive black (detectors inactive status due to action of fast switch 2 (pin 1); see Table 1, Fig.9 and note 3)						
I_{18}	discharge current of peak dark storage capacitor	outside active measurement window	0.1	0.5	1.0	µA
		inside active measurement window	1.5	2.5	3.5	µA
I_{18}	charge current of peak dark storage capacitor		–360	–300	–250	µA
	maximum level shift: Δ black level in percent of nominal signal amplitude		10	13	16	%
	difference between nominal black and adaptive black in percent of nominal signal amplitude		–3	0	+3	%
	detectors inactive time before blanking		2.3	3.1	4.0	µs
	detectors inactive time after blanking		2.3	2.5	3.4	µs
Gamma adjust Acts on internal Y signal; Y matrix see Y output; I²C-bus controlled potentiometer (subaddress 0B) Resolution 6 bit						
	range of gamma minimum ($3F_{HEX}$) maximum (00_{HEX})		 – –	 0.7 1.0	 – –	 – –
	maximum gain at minimum gamma	near nominal black	5	6	7	dB
Saturation adjust Acts on RGB signals; Y matrix see Y output; I²C-bus controlled potentiometers (subaddress 01) Resolution 1.5% of maximum saturation						
	I²C-bus data for nominal saturation		1F	20	21	HEX
	maximum saturation	I²C-bus data $3F_{HEX;}$ measured at 100 kHz; relative to nominal saturation	4.9	5.5	6.1	dB
	minimum saturation	I²C-bus data $00_{HEX;}$ measured at 100 kHz; relative to typical value of maximum saturation	–	–	–50	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Contrast adjust Acts on RGB signals; I^2C-bus controlled potentiometers (subaddress 02) Resolution 1.5% of maximum contrast						
	I^2C-bus data for nominal contrast		20	22	24	HEX
	maximum contrast	I^2C-bus data $3F_{HEX;}$ limiters inactive; relative to nominal contrast	–	4.5	5.5	dB
	minimum contrast	I^2C-bus data $00_{HEX;}$ relative to maximum	–28	–22	–16	dB
Brightness adjust Acts on RGB signals; I^2C-bus controlled potentiometers (subaddress 00) Resolution 1.5% of range; Δ black level in percent of nominal signal amplitude referred to cut-off measuring level						
	maximum brightness: Δ black level	$3F_{HEX}$	23	30	37	%
	nominal brightness: Δ black level	29_{HEX}	–7	0	+7	%
	minimum brightness: Δ black level	00_{HEX}	–58	–50	–42	%
	maximum brightness: Δ black level	$3F_{HEX;}$ control bits BCOF = 1 and MOD2 = 0	23	30	37	%
	minimum brightness: Δ black level	$00_{HEX;}$ control bits BCOF = 1 and MOD2 = 0	–58	–50	–42	%
Blue stretch Blue stretch is activated by I^2C-bus control bit BLST = 1 (see Fig.11)						
	increase of small signal gain	100% of nominal signal amplitude and at 1 MHz	15	20	25	%
Differences of black level steps Differences from channel to channel of the ratio of the difference (black level cut-off measurement level) to actual nominal signal amplitude (V_{nom24}, V_{nom22}, V_{nom20}) over the whole contrast, brightness and saturation range, switching matrix or switching fast switches, gamma = 1, BLST = 0, ADBL = 0						
dV/V_{nom}	static deviation	$dV/V_{nom} = dV_{24}/V_{nom24} - dV_{22}/V_{nom22} = dV_{24}/V_{nom24} - dV_{20}/V_{nom20} = dV_{22}/V_{nom22} - dV_{20}/V_{nom20;}$ ripple on pin 5 during clamping ≤ 1 mV; note 8	–1.0	–	+1.0	%
		at nominal saturation	–0.5	–	+0.5	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB outputs (output for positive RGB signals (R: pin 24, G: pin 22, B: pin 20); following data without external load)						
$R_{24,22,20}$	differential output resistance		–	25	30	Ω
$I_{24,22,20}$	maximum output current		4.0	5.0	–	mA
$V_{24,22,20}$	minimum output voltage	note 9	–	–	0.8	V
$V_{24,22,20}$	maximum output voltage	$R_L \geq 2$ kΩ	6.3	7.0	–	V
$V_{24,22,20}$	maximum signal amplitude (black-white) due to internal limits (peak-to-peak value)		3.3	–	–	V
$V_{24,22,20}$	nominal signal amplitude (black-white; peak-to-peak value)	at nominal white adjust; contrast and saturation setting; gamma = 1; nominal input signals	1.7	2.0	2.3	V
$V_{24,22,20}$	range of cut-off measurement level	note 9	1.0	–	5.0	V
$V_{24,22,20}$	recommended cut-off measurement level		–	3.0	–	V
Output clamp (RGB)						
$V_{20,22,24}$	clamp voltage black level	control bit BCOF = 1	2.3	2.5	2.7	V
White potentiometers						
	I^2C-bus data for nominal settings		21	22	23	HEX
	maximum increase of AC gain	$3F_{HEX}$	40	50	60	%
	maximum decrease of AC gain	00_{HEX}	40	50	60	%
Overall white point deviation						
dV/V_{nom}	$dV/V_{nom} = dV_{24}/V_{nom24} - dV_{22}/V_{nom22} = dV_{24}/V_{nom24} - dV_{20}/V_{nom20} = dV_{22}/V_{nom22} - dV_{20}/V_{nom20}$ meaning of actual nominal signal see ‘differences of black level step’; over whole contrast range see ‘contrast adjust’	input: $(RGB)_{1,2}$ differences from channel to channel of the ratio of the difference (signal white level cut-off measurement level) to actual nominal signal amplitude ($V_{nom\ 24}$, $V_{nom\ 22}$, $V_{nom\ 20}$) over the whole saturation range at nominal contrast, brightness and nominal input signals; ripple on pin 5 during clamping ≤ 1 mV; note 8	–2.0	–	+2.0	%
Frequency behaviour, crosstalk						
Between the Y input (pin 8) and the RGB outputs (pins 24, 22 and 20)						
	decrease in gain	1 MΩ and 20 pF load at 13 MHz	–	–	3	dB
Between the colour-difference inputs (pins 7 and 6) and the corresponding R and B outputs (pins 24 and 20)						
	decrease in gain	at 13 MHz	–	–	3	dB
Between the $(RGB)_{1,2}$ inputs (pins 10, 11 and 12 or 2, 3 and 4) and the RGB outputs (pins 24, 22 and 20)						
	decrease in gain	at 22 MHz	–	–	3	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sandcastle input (pin 14; control bit SC5; note 4)						
I_{14}	input current	$V_{14} < 0.5$ V	–	–	–100	µA
C_{14-9}	input capacitance		–	–	10	pF
V_{14}	required voltage range for horizontal and vertical blanking pulses	SC5 = 0 or SC5 = 1	2.0	2.5	3.0	V
	for horizontal pulses (line count)	SC5 = 0	4.0	4.5	4.9	V
	for burst key pulses	SC5 = 0	6.1	–	$V_P + 5.8$	V
	for burst key pulses and line count	SC5 = 1	4.0	–	$V_P + 5.8$	V
Clamp pulse delay						
	delay of leading edge of clamping pulse	nominal sandcastle pulse				
		DELOF = 0	1.2	1.5	1.8	µs
		DELOF = 1	–	0	–	µs
Required minimal burst gate pulse width						
	DELOF = 0	line frequency = 16 kHz	3	–	–	µs
	DELOF = 1	line frequency = 32 kHz	1.5	–	–	µs
Generation of measurement lines and blanking						
Blanking to ultra black level occurs during time DG except MR in R-channel, MG in G-channel, MB in B-channel (see pulse diagram Fig.12) Difference between ultra black level (VUB) and measurement level (VCL) in percent of nominal signal amplitude (independent of white point adjust)						
dV/V_{nom}	dV = VCL – VUB	no clipping	25	35	45	%
Leakage current measuring time: LM will start after the end of vertical sandcastle (see pulse diagram)						
Vertical blanking period and cut-off measurement lines (see pulse diagram) The vertical component will be identified if it contains 2 or more burst key pulses in case of SC5 = 1 or two or more line pulses (H) in case of SC5 = 0 The line counter is triggered by the leading edge The blanking time is valid for a vertical pulse detected by the sandcastle decoder The internal blank pulse is OR gated with the sandcastle vertical pulse and the end of the measurement pulses						
Insertion time: full line period Measurement time: line period minus horizontal period (50/60 Hz)						
Line sequence of measuring lines: First line after end of horizontal pulse which followed the end of vertical pulse: leakage measurement LM First line after leakage pulse: red measurement MR Second line after leakage pulse: green measurement MG Third line after leakage pulse: blue measurement MB (see pulse diagram)						

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Warm up test pulse during MT (see pulse diagram)						
V_{WU}	warm up level	$V_{WU} = V_{PL} - 1$ V; V_{PL} = peak drive level (see also signal limiting); given by I^2C-bus; subaddress OA; no warm up test pulse in case of output clamping (BCOF = 1)	–	–	–	–
	maximum warm up level	$3F_{HEX}$	5.6	6.0	6.3	V
Threshold for Power On Reset (POR) during time DG (see pulse diagram)						
$V_{20,22,24\ POR}$	output voltage to cause POR	RELC = 0	–	V_{PL}	–	V
		RELC = 1	–	V_{PL} + 1	–	V
Y output (pin 26; note 5)						
V_{26}	nominal signal amplitude (black-white; independent of gamma, adaptive black and contrast; peak-to-peak value)	control bit YEXH = 1; hue DAC (register 03) set $> 28_{HEX}$	0.85	1.0	1.15	V
V_{26}	black level	YEXH = 1				
		$3F_{HEX}$	–	4.0	–	V
		20_{HEX}	–	2.0	–	V
	Y matrix coefficients	$Y = a_r R + a_g G + a_b B$				
	a_r		0.27	0.30	0.33	–
	a_g		0.53	0.59	0.65	–
	a_b		0.10	0.11	0.12	–
R_{26}	differential output resistance		–	190	230	Ω
$\Delta\tau_{26}$	group delay time	between RGB outputs and Y output	20	25	30	ns
f_g	3 dB bandwidth		11	15	–	MHz
Automatic cut-off control (pin 19; measurement periods see beam info on pin 19)						
V_{19}	permissible voltage (also during scanning period)		–	–	$V_P - 1.4$	V
V_{REF0}	internally controlled voltage on pin 19	during leakage measurement time LM	2.4	2.7	3.0	V
I_{19}	maximum output current		–350	–	–250	μA
I_{19}	maximum input current		250	–	350	μA
R_{19}	input resistance for measurement input		1	–	–	MΩ
I_{19}	additional input current	only during warm up	–	0.5	–	mA
V_{19}	threshold of warm up detector (active in line MG)		4.3	4.5	4.7	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{MEAS}	difference between input voltage for cut-off and $V_{REF0;}$ adjustable via I^2C-bus (subaddress for reference: R: 07, G: 08 and B: 09)		–	–	–	–
	maximum V_{MEAS}	$3F_{HEX}$	1.5	1.6	1.7	V
	nominal V_{MEAS}	20_{HEX}	0.9	1.0	1.1	V
	minimum V_{MEAS}	00_{HEX}	0.4	0.45	0.5	V
Storage of cut-off control voltage / output clamping voltage (pins 25, 23 and 21)						
$I_{25,23,21}$	input currents of storage inputs outside of the measurement time		–	–	0.1	µA
$\lvert I_{25,23,21} \rvert$	maximum charge / discharge current during measurement time		0.2	0.3	0.4	mA
	amplification from storage pins 25, 23 and 21 to outputs		–	1.7	–	–
Storage of leakage information (pin 17)						
I_{17}	maximum charge / discharge current at time LM		300	400	–	µA
I_{17}	discharge current	peak limiting during time MK active	–	4	–	mA
I_{17}	leakage current	outside time LM	–	–	0.1	µA
V_{17}	voltage to reset IC to switch on conditions	V_{17} is below	2.3	2.5	3.0	V
Signal limiting (The limitation acts on contrast and at low contrast on brightness)						
Average beam current limiting (pin 15)						
V_{15}	start of contrast reduction		–	4	–	V
dV_{15}	input range for full contrast reduction		–	–2	–	V
V_{15}	start of brightness reduction		–	2.5	–	V
dV_{15}	input range for full brightness reduction		–	–1.6	–	V
I_{15}	input current		–	–	–0.5	µA
Peak signal limiting of output signals (pin 16) The limitation acts 1 H delayed Limiting level adjustable by I^2C-bus (subaddress OA; control bit RELC = 0)						
$V_{24,22,20}$	maximum limiting level	extrapolated from 2F	6.8	–	7.2	V
$V_{24,22,20}$	minimum limiting level	00_{HEX}	–	2.3	3	V
I_{16}	maximum discharge current at peak drive	RELC = 0	4	–	6	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Peak signal limiting (pin 16) Control bit RELC = 1; Limiting Level (V_{LiL}) adjustable by I^2C-bus (subaddress OA)						
V_{LiL}		equal gain in white point adjust; signal only in one output channel				
	maximum limiting level	$3F_{HEX}$	3.3	3.5	3.9	V
	minimum limiting level	00_{HEX}	1.3	1.5	1.7	V
Peak drive limiting starts, if the maximum of the RGB signals after white point adjustment exceeds a threshold Cut-off measurement level MX = MR or MB or MG						
Discharge currents						
The total discharge current is a summation of $I_{16(1)} + I_{16(2)} + I_{16(3)}$						
Threshold 1 (TH1)						
$I_{16(1)}$	maximum discharge current	TH1 = MX + V_{LiL}; 1 line delayed and low-pass filtered	4.5	6	7.5	mA
	steepness		–	1.5	–	mA / 0.1 V
Low-pass filter, control bit TCPL						
t_{DPDL}	time constant low-pass filter	TCPL = 1 (at $1f_H$); RELC = 1	0.9	1.2	1.5	µs
t_{DPDL}	time constant low-pass filter	TCPL = 0 (at $2f_H$); RELC = 1	0.4	0.6	0.8	µs
Threshold 2 (TH2)						
$I_{16(2)}$	maximum discharge current	TH2 = MX + $V_{LiL} \times 1.10$; 1 line delayed	4.5	6	7.5	mA
	steepness		–	1.5	–	mA / 0.1 V
Threshold 3 (TH3)						
$I_{16(3)}$	maximum discharge current	TH3 = MX + V_{LiL}; undelayed	0.45	0.6	0.75	mA
	steepness		–	0.15	–	mA / 0.1 V
Charge current						
I_{16}	charge current		–0.5	–1	–2	µA
V_{16}	start of contrast reduction		–	4	–	V
dV_{16}	input range for full contrast reduction		–	–2	–	V
V_{16}	start of brightness reduction		–	2.5	–	V
dV_{16}	input range for full brightness reduction		–	–1.6	–	V
V_{16}	maximum voltage by internal limitation		4.5	–	–	V
Hue adjust output (pin 26; note 6)						
V_{26}	minimum output voltage	YEXH = 0; 00_{HEX}	0.5	–	1.0	V
V_{26}	nominal output voltage	YEXH = 0; 20_{HEX}	3.0	3.2	3.4	V
V_{26}	maximum output voltage	YEXH = 0; $3F_{HEX}$	4.8	–	5.5	V
I_{26}	current of internal emitter follower		500	700	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus inputs						
f_{28}	clock frequency range		0	–	100	kHz
$t_{SU;DAT}$	data set-up		250	–	–	ns
t_H	clock pulse HIGH		4	–	–	µs
t_L	clock pulse LOW		4.7	–	–	µs
t_r	rise time		–	–	1	µs
t_f	fall time		–	–	0.3	µs
Input levels						
V_{27}	LOW level input voltage		–	–	1.5	V
V_{28}			–	–	1.5	V
V_{27}	HIGH level input voltage		3.0	–	5.5	V
V_{28}			3.0	–	5.5	V
I_{27}	input current	V_{27} = 0.4 V	–10	–	–	µA
I_{28}		V_{28} = 0.4 V	–10	–	–	µA
I_{27}	input current	V_{27} = 0.9 V	–	–	10	µA
I_{28}		V_{28} = 0.9 V	–	–	10	µA
V_{27}	LOW level output voltage		–	–	0.4	V
I_{27}	output current	V_{27} = 0.4 V	3.0	–	–	mA

Notes to the characteristics

1. RGB signals controlled by saturation, adaptive black, contrast and brightness, gamma affects the Y component of the internal RGB signals.
2. Matrix coefficients should be tested by comparing RGB output signals with a reference RGB colour bar, which is fed in at $(RGB)_1$ or $(RGB)_2$ inputs. In case of NMEN = 1 (NTSC) at minimum saturation the Y output and RGB output signals are not identical to the Y input signal. PAL/SECAM signals are matrixed by the equation:
   $V_{G-Y} = -0.51V_{R-Y} - 0.19V_{B-Y}$
   NTSC signals are matrixed by the equations (hue phase shift of −2 degrees):
   $V_{R-Y}^* = 1.39V_{R-Y} - 0.07V_{B-Y}$; $V_{G-Y}^* = -0.46V_{R-Y} - 0.15V_{B-Y}$; $V_{B-Y}^* = V_{B-Y}$
   In the matrix equations: V_{R-Y} and V_{B-Y} are conventional PAL demodulation axes and amplitudes at the output of the demodulator. V_{R-Y}^*, V_{G-Y}^* and V_{B-Y}^* are the NTSC-modified colour-difference signals.
3. Adaptive black control acts on Y signal, which is either Y input or Y output from RGB matrix. Negative set-up is not affected. The level shift value is determined by the peak dark detector, operation selected by control bit ADBL. The peak dark detector is inactive during blanking. Peak dark detector activated by internal line counter, which starts after the end of the vertical blank of the sandcastle. Active from line 16 (after end of vertical sandcastle) to line 224 (NTSC mode, NMEN = 1) or line 272 (PAL mode, NMEN = 0). It is recommended to increase the contrast value (subaddress 02) by 15% if ADBL = 1. The line numbers are doubled if control bit HDTV = 1.
4. Sandcastle pulse detector (pin 14)
   The sandcastle pulse is compared with 3 (control bit SC5 = 0) or 2 (SC5 = 1) internal threshold levels to separate the various pulses; the internal pulses are generated while the input pulse is higher than the thresholds. The thresholds are independent of supply voltage and temperature.
5. Y output can be switched to hue adjust output via I^2C-bus control bit YEXH. Output without sync pulse. Recommendation: Hue adjust DAC set to $3F_{HEX}$. Black level adjustable via hue adjust DAC.
6. Output can be switched to Y output via I^2C-bus control bit YEXH (via I^2C-bus, resolution 6 bit, bus subaddress 03).
7. At minimum gamma ($3F_{HEX}$) any differences in black level steps are amplified by 6 dB.
8. Series resistor in supply voltage should be less than 0.3 Ω.
9. At 1.0 V cut-off measurement level the function of the cut-off control loop is not guaranteed because the blanking level is limited to the minimum output voltage. For proper working a guide number for the minimum cut-off measurement level is 1.3 V.

APPENDIX

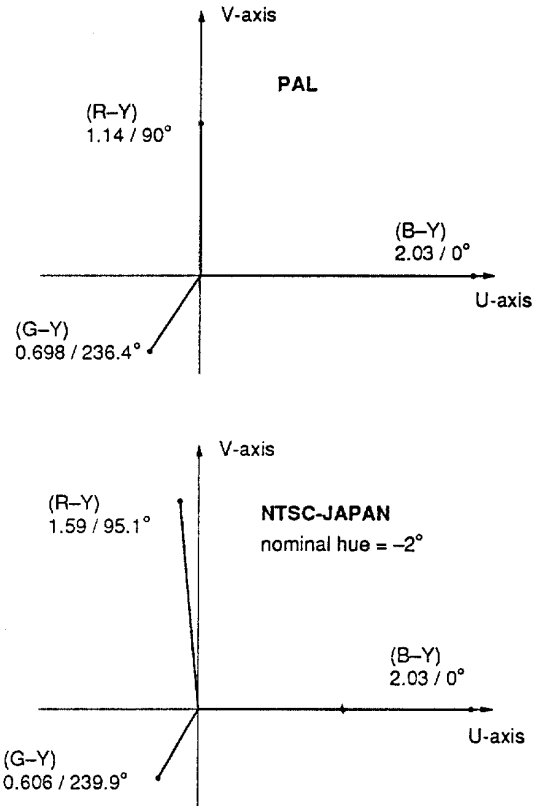


Fig.4 Demodulation axes.

I²C-BUS RECEIVER (pins 27 and 28)

S: start condition
P: stop condition
W: write
A: acknowledge

slave address:

A6	A5	A4	A3	A2	A1	A0	$\overline{W}$
1	0	0	0	1	0	0	0

receiver (write mode)
slave receiver format is (BREN = 0)

S	SLAVE ADDRESS A	SUBADDRESS A	DATA BYTE A ... DATA BYTE A n data bytes with auto-increment of subaddresses	P

All subaddresses within the range 00 to 0F are automatically incremented. The subaddress counter wraps around from 0F to 00. Only in this case 0F will be acknowledged too.
Subaddresses outside the range 00 to 0E are not acknowledged by the device and neither auto-increment nor any other internal operation takes place.
All eight bits of the subaddress have to be decoded by the device.
If BREN = 1 (control register 1) auto-increment is not possible, the slave receiver format is:
S, SLAVE ADDRESS A, SUB ADDRESS A, DATA BYTE A, P

:

Table 1 Signal input selection and effect on adaptive black measurements by fast source switches and I²C-bus.

I²C-BUS CONTROLLED BITS				ANALOG SWITCH		SELECTED SIGNALS			
FSON2	**FSDIS2**	**FSON1**	**FSDIS1**	**FSW2 (pin 1)**	**FSW1 (pin 13)**	**RGB_2 (pins 2, 3 and 4)**	**ADBL**	**RGB_1 (pins 10, 11 and 12**	**TV (pins 6, 7 and 8)**
L	L	L	L	L	L		active		ON
				L	H		active	ON	
				H	*	ON	off		
L	L	L	H	L	*		active		ON
				H	*	ON	off		
L	L	H	*	L	*		active	ON	
				H	*	ON	off		
L	H	L	L	*	L		active		ON
				*	H		active	ON	
L	H	L	H	*	*		active		ON
L	H	H	*	*	*		active	ON	
H	L	*	*	L	*	ON	active		
				H		ON	off		
H	H	*	*	*	*	ON	active		

Notes

1. H: logical HIGH or analog switch (pins 1 and 13) to > 0.9 V
2. L: logical LOW or analog switch (pins 1 and 13) to < 0.4 V
3. *: H or L, no influence
4. ON: is the selected signal input

Table 2 Crosstalk

FSW1	FSW2	CROSSTALK	at 4 MHz maximum value (dB)	at 8 MHz maximum value (dB)	at 13 MHz maximum value (dB)
L	L	$RGB_1 \rightarrow$ Y, CD	–58	–55	–50
		$RGB_2 \rightarrow$ Y, CD	–58	–55	–50
L	H	Y, CD $\rightarrow RGB_1$	–51	–50	–47
		$RGB_2 \rightarrow RGB_1$	–58	–55	–50
L	H	Y, CD $\rightarrow RGB_2$	–51	–50	–47
		$RGB_1 \rightarrow RGB_2$	–58	–55	–50
H	H	Y, CD $\rightarrow RGB_2$	–51	–50	–47
		$RGB_1 \rightarrow RGB_2$	–58	–55	–50

Table 3 Subaddress byte and data byte format.

FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
brightness	00	0	0	A05	A04	A03	A02	A01	A00
saturation	01	0	0	A15	A14	A13	A12	A11	A10
contrast	02	0	0	A25	A24	A23	A22	A21	A20
hue	03	0	0	A35	A34	A33	A32	A31	A30
red gain	04	0	0	A45	A44	A43	A42	A41	A40
green gain	05	0	0	A55	A54	A53	A52	A51	A50
blue gain	06	0	0	A65	A64	A63	A62	A61	A60
red level reference	07	0	0	A75	A74	A73	A72	A71	A70
green level reference	08	0	0	A85	A84	A83	A82	A81	A80
blue level reference	09	0	0	A95	A94	A93	A92	A91	A90
peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0
gamma	0B	0	0	AB5	AB4	AB3	AB2	AB1	AB0
control register 1	0C	SC5	DELOF	BREN	X	NMEN	X	X	X
control register 2	0D	X	HDTV	FSBL	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
control register 3	0E	ADBL	YHI	MOD2	BLST	YEXH	RELC	TCPL	0

The least significant bit of an analog control alignment register is defined as AX0 (D0).
After power on reset (PONRES) all alignment registers are set to 01.
X means don’t care but for software compatibility with further video ICs with the same slave address, it is recommended to set all X to 0.

Table 4 RGB processor mode bits control register.

SYMBOL	PARAMETER	CONDITIONS
Control register 1		
SC5	sandcastle 5 V	0 = 3-level sandcastle pulse
		1 = 2-level sandcastle pulse
DELOF	delay of leading edge of clamping pulse switched off	0 = delay
		1 = no delay
BREN	buffer register enable	0 = new data are executed just after reception
		1 = data are hold in a latch (buffer register) and will be transferred to their destination register within the next vertical blanking interval; the device does not acknowledge any new data transfer until the internal transfer to the destination register has been completed
NMEN	NTSC - matrix enable	0 = PAL matrix
		1 = NTSC matrix
Control register 2		
HDTV	HDTV / progressive scan for ADBL line counter	0 = 272 (PAL), 224 (NTSC) lines
		1 = 544 (PAL), 448 (NTSC) lines
FSBL	full screen black level, e.g. for optical measurement	0 = normal mode
		1 = cut-off measurement level during full field brightness, inactive
BCOF	internal black level control off	0 = automatic cut-off control active
		1 = RGB outputs clamped to fixed DC levels
FSON2	fast switch 2 on	see Table 1
FSDIS1	fast switch 1 disable	
FSDIS2	fast switch 2 disable	
FSON1	fast switch 1 on	
Control register 3		
ADBL	adaptive black	0 = off
		1 = on
YHI	Y high level	0 = input = 0.315 $V_{(p-p)}$ (black-white)
		1 = input = 1.0 $V_{((p-p)}$ (black-white)
MOD2	modus 2	0 = inactive (BCOF = 0) AND (MOD2 = 1) is senseless; no output stabilization
		1 = output clamp without brightness adjust, brightness remains active e.g. for blue stretch
BLST	blue stretch	0 = off
		1 = on
YEXH	Y exclusive hue	0 = pin 26 is switched to hue adjust output
		1 = pin 26 is switched to Y output
RELC	relative to cut-off	0 = peak drive limit to absolute output
		1 = peak drive limit relative to cut-off
TCPL	time constant peak drive limiter	0 = 2 f_H
		1 = 1 f_H

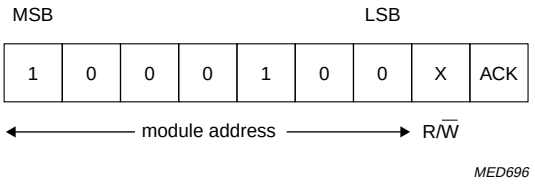


Fig.5 The module address byte.

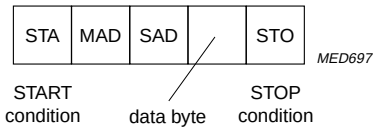


Fig.6 Data transmission without auto-increment (BREN = 0 or 1)

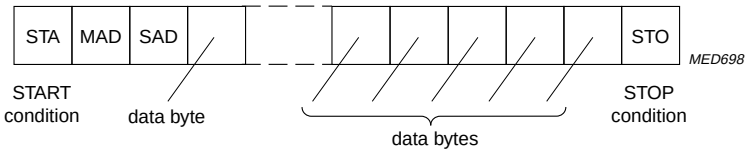


Fig.7 Data transmission with auto-increment (BREN = 0).

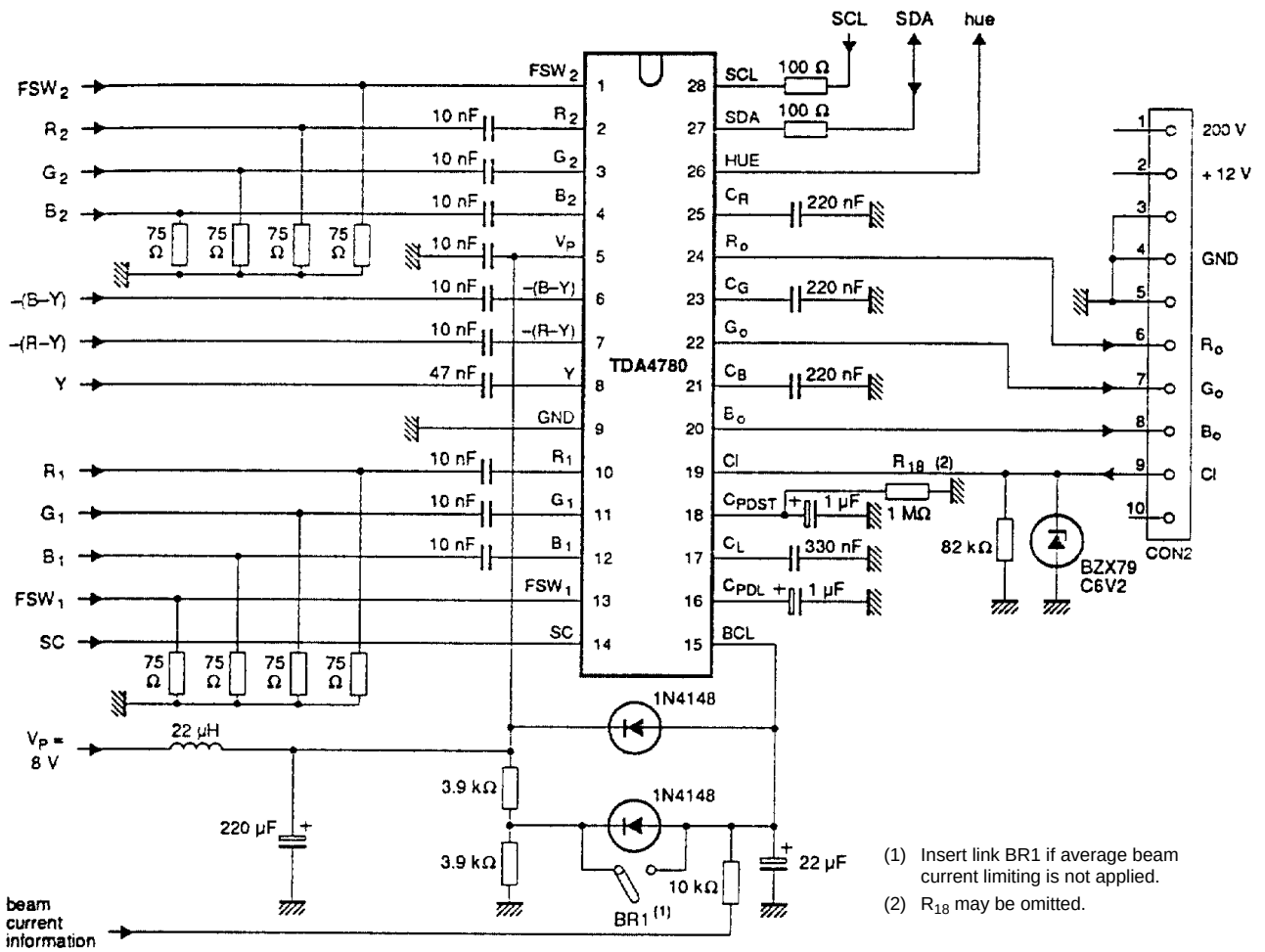


Fig.8 Test and application circuit.

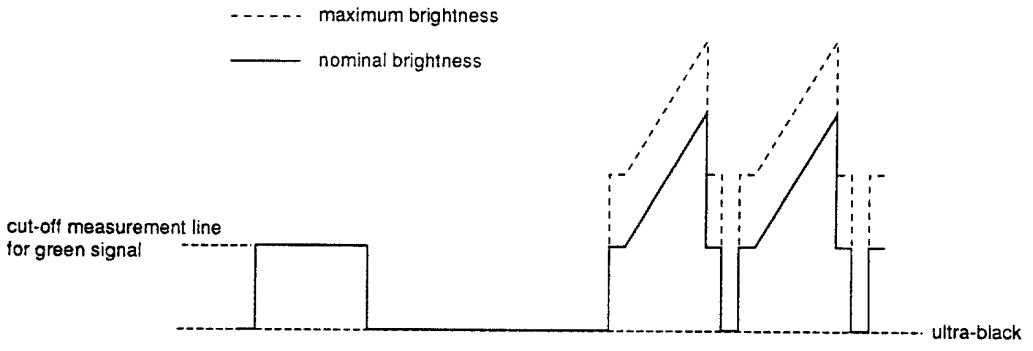


Fig.9 Cut-off measurement pulses

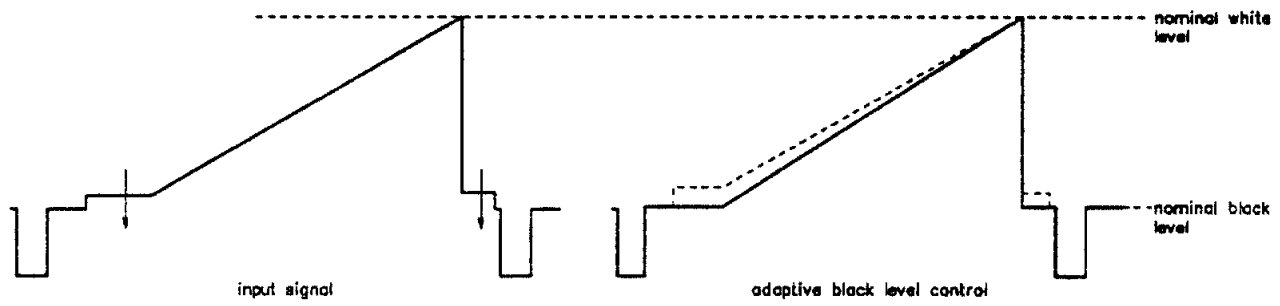


Fig.10 Principle of adaptive black control.

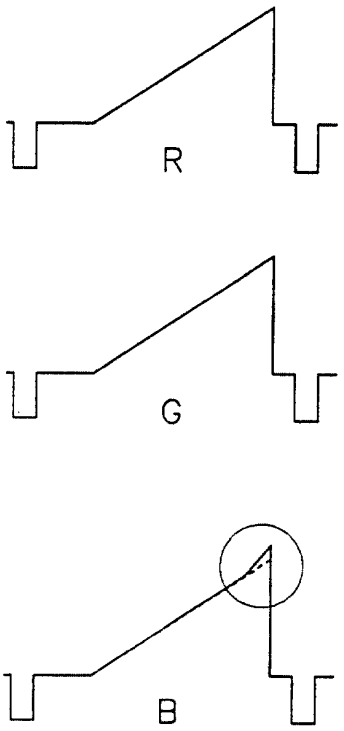
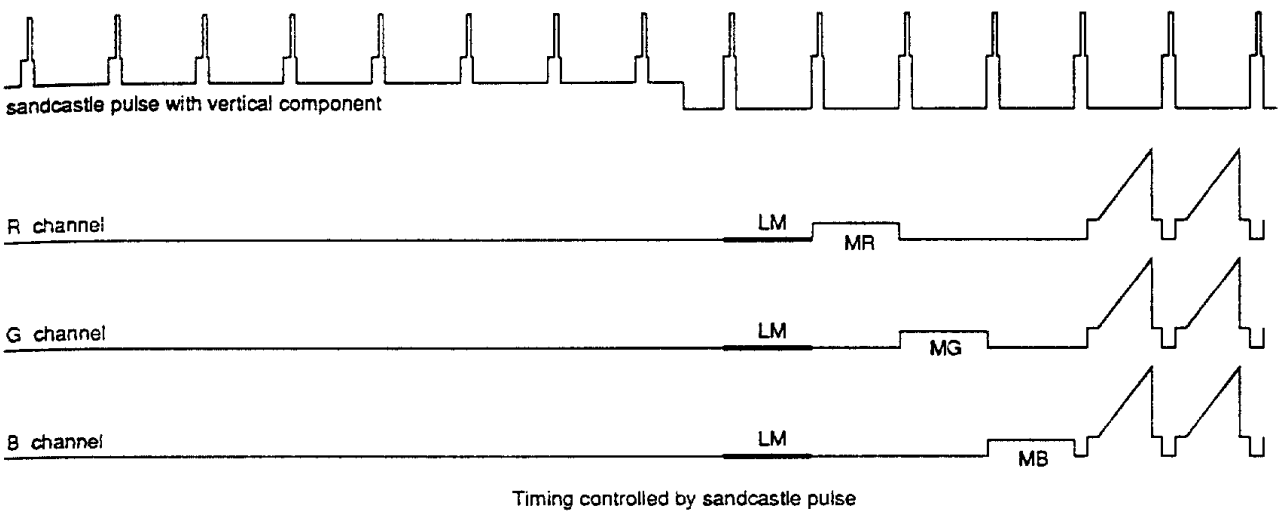


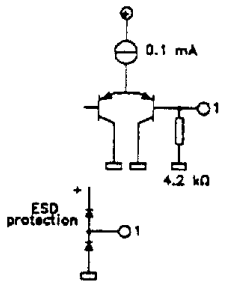
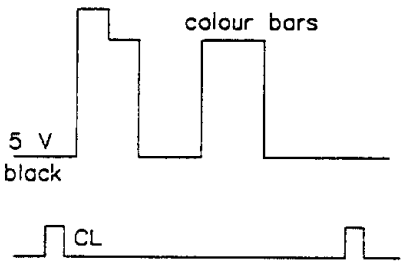
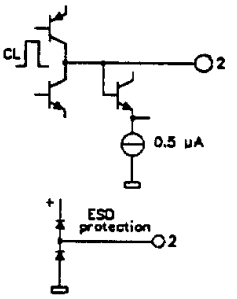
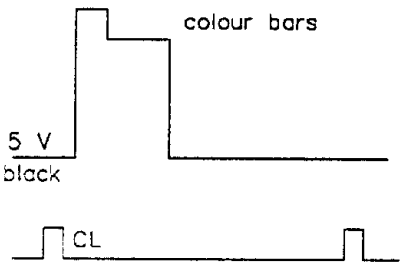
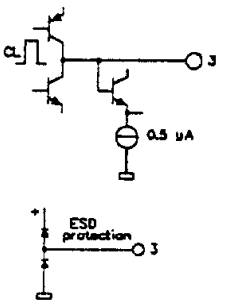
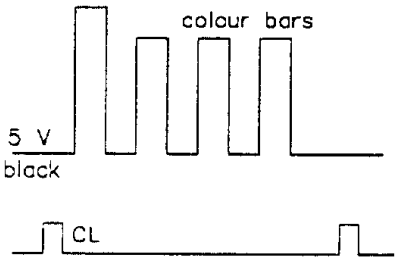
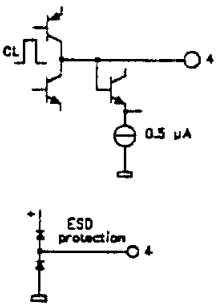
Fig.11 Principle of blue stretch.

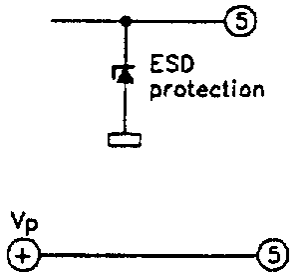
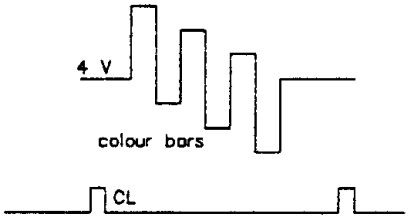
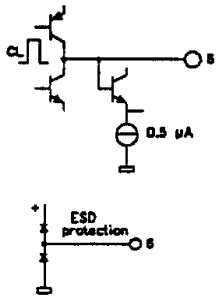
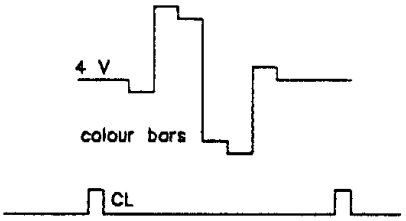
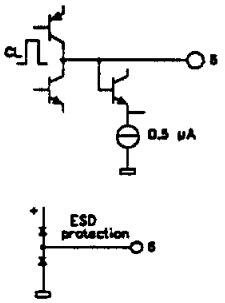
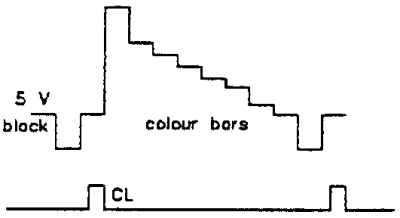
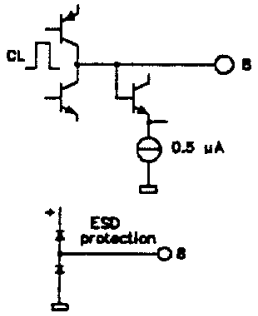


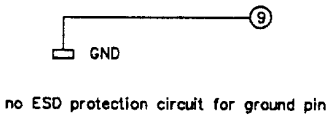
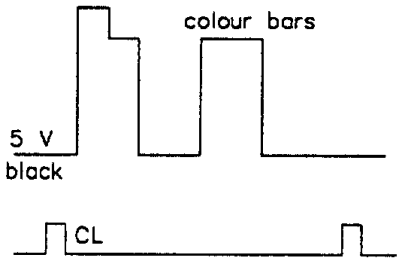
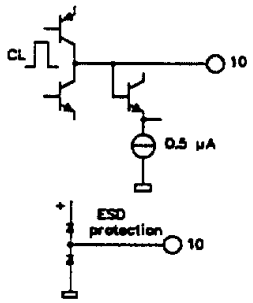
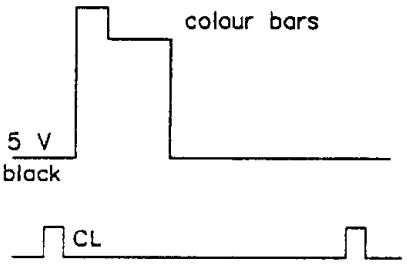
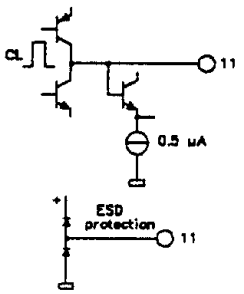
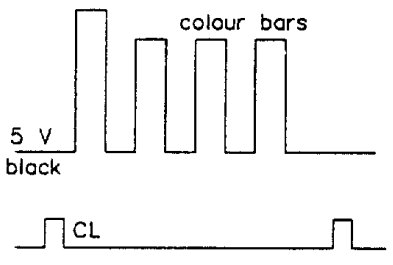
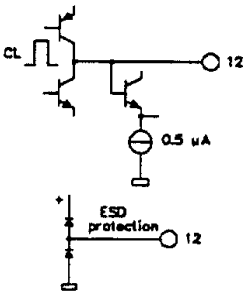
LM = leakage current measurement time
MR, MG, MB = R, G, B cut-off measurement pulses

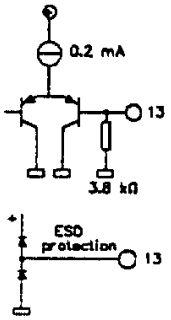
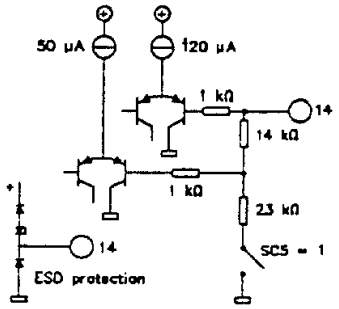
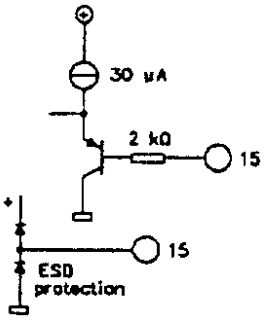
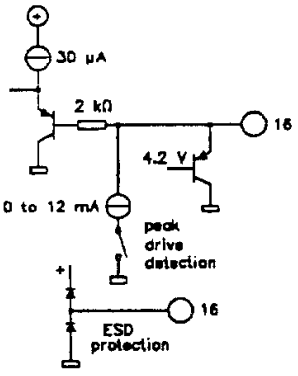
Fig.12 Leakage and cut-off current measurement timing diagram.

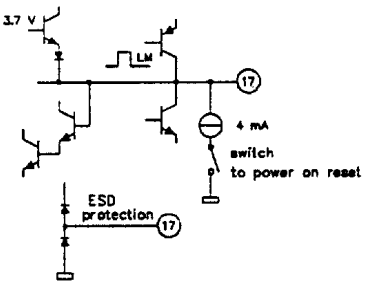
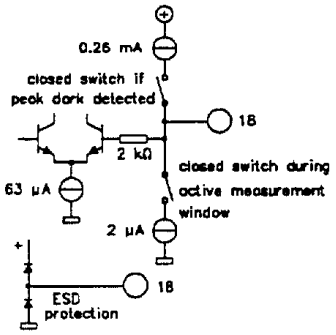
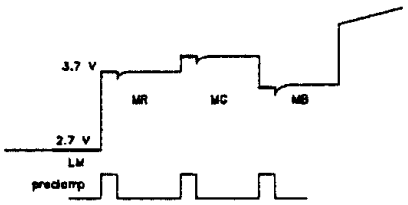
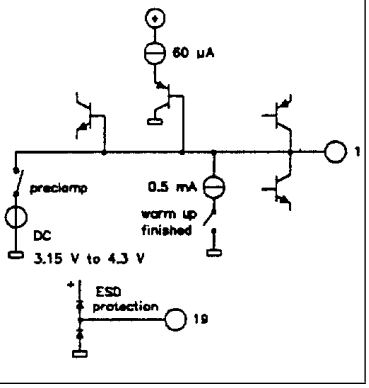
Table 5 internal circuitry (Abbreviations: OB: open base and CL: clamp pulse)**.**

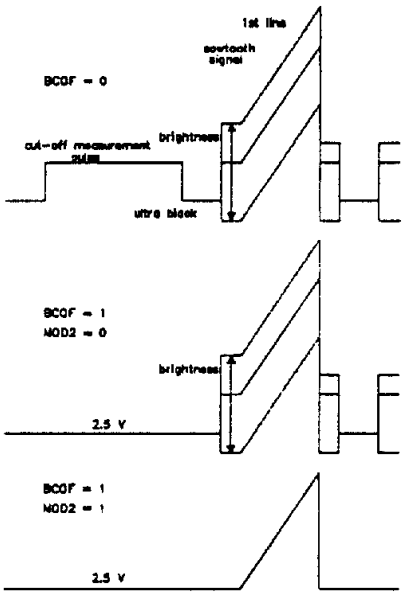
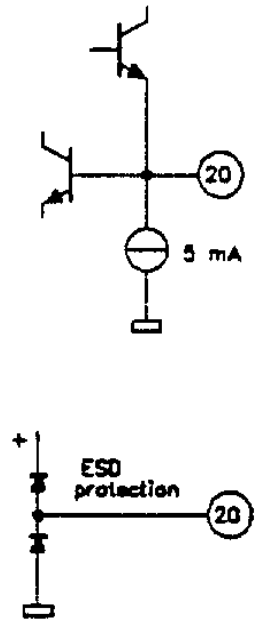
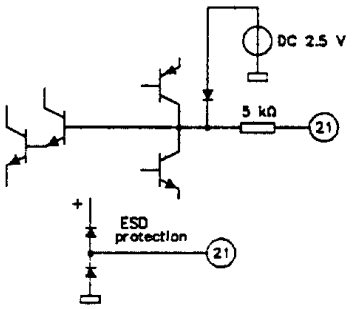
PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
1	fast switch 2			
2	R_2 input clamp		100 µA / OB	
3	G_2 input clamp		100 µA / OB	
4	B_2 input clamp		100 µA / OB	

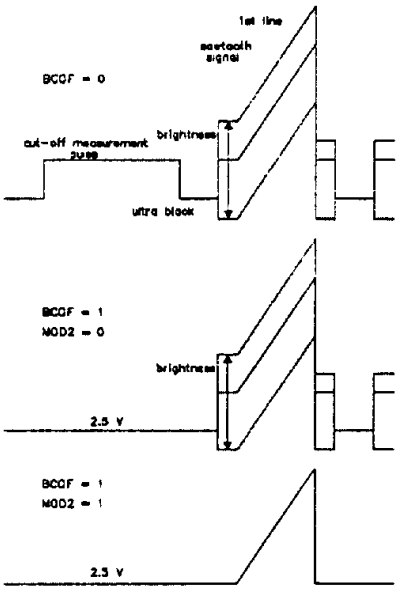
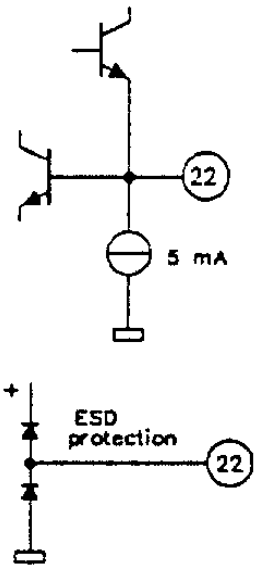
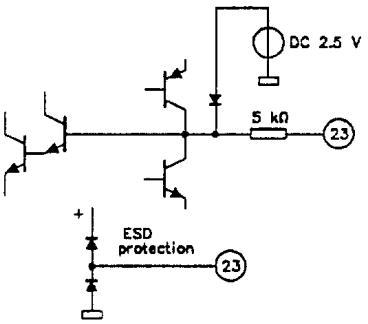
PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
5	supply voltage			
6	–(B–Y) input clamp		100 µA / OB	
7	–(R–Y) input clamp		100 µA / OB	
8	Y input clamp		100 µA / OB	

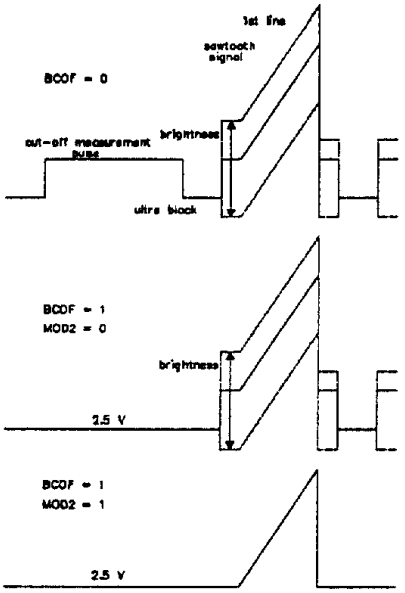
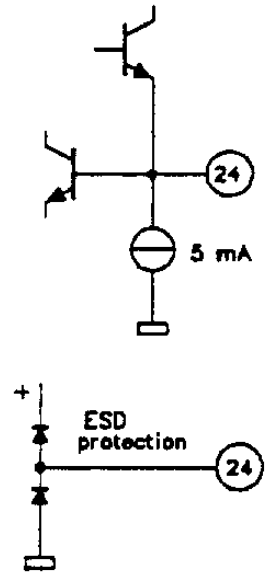
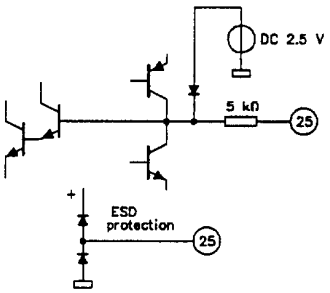
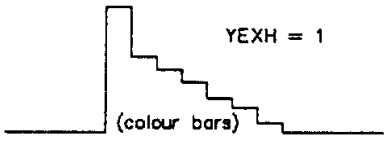
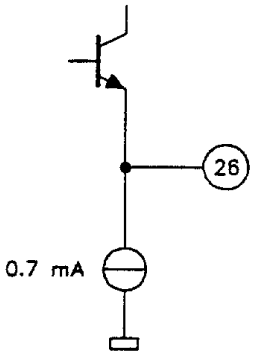
PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
9	ground			
10	R_1 input clamp		100 µA / OB	
11	G_1 input clamp		100 µA / OB	
12	B_1 input clamp		100 µA / OB	

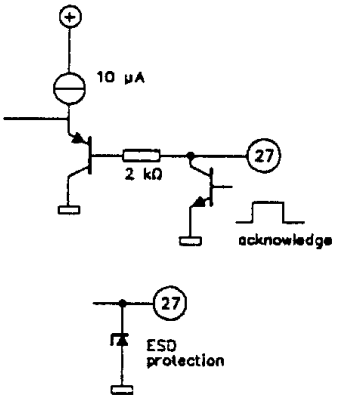
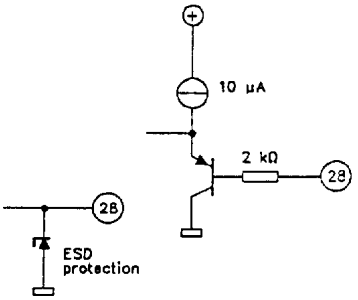
PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
13	fast switch 1			
14	sandcastle input	3-level sandcastle CL 5.5 V H 3.5 V V 1.5 V 2-level sandcastle CL 3.5 V HV 1.5 V	37 kΩ (SC5 = 0) OB (SC5 = 1)	
15	average beam current limiting input		OB	
16	storage capacitor for peak limiting input	outside peak drive during peak drive (RELC = 1) during peak drive (RELC = 0)	OB 0 to 12 mA 5 mA	

PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
17	storage capacitor for leakage current	outside leakage current measurement during leakage current measurement automatic switch to power on reset	OB –400 µA to +400 µA 4 mA	
18	peak dark storage		OB / 0.26 mA	
19	cut-off measurement input (beam current information input)		–180 µA to +180 µA	

PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
20	blue output		5 mA 5 mA 5 mA	
21	blue cut-off storage capacitor	during cut-off control or during output clamping	OB −300 µA to +300 µA	

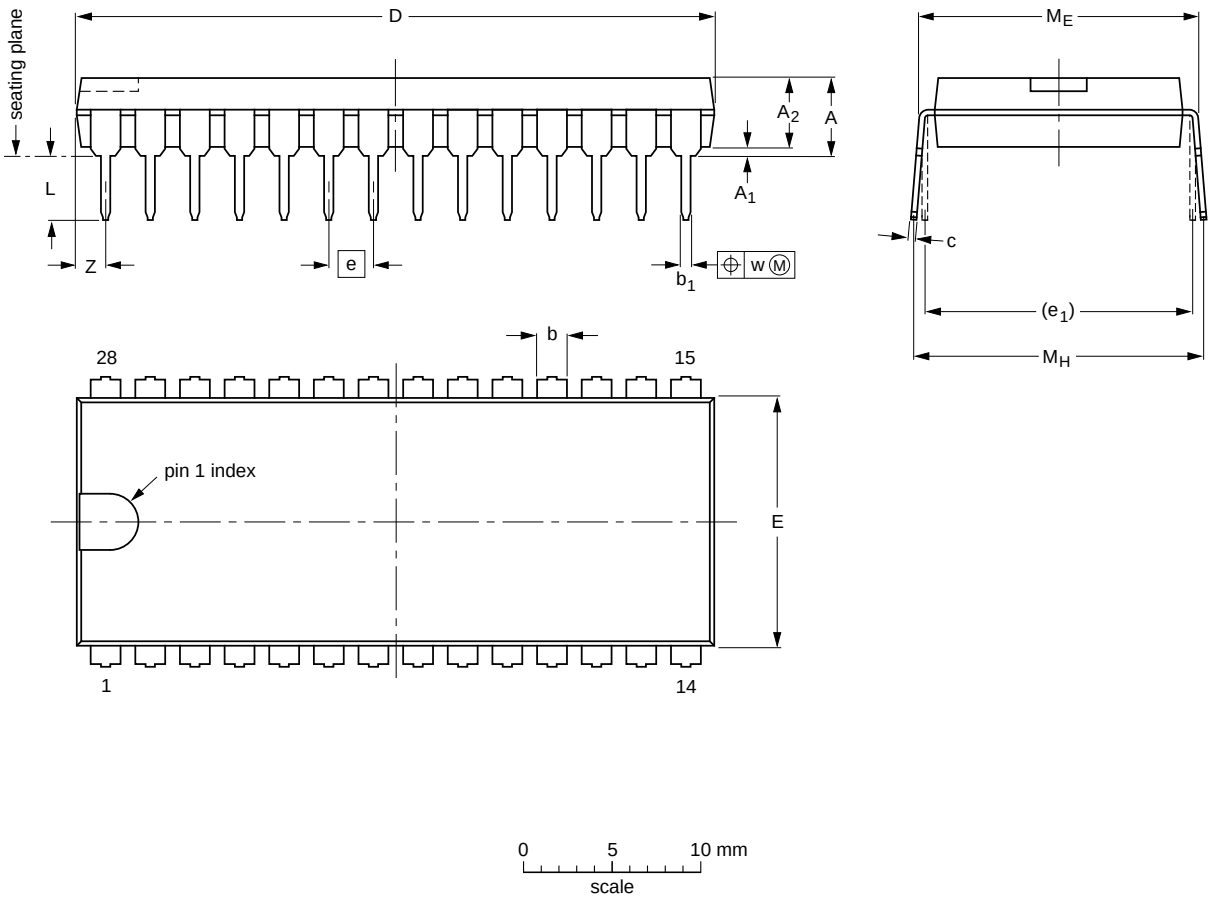
PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
22	green output		5 mA 5 mA 5 mA	
23	green cut-off storage capacitor	during cut-off control or during output clamping	OB –300 µA to +300 µA	

PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
24	red output		5 mA 5 mA 5 mA	
25	red cut-off storage capacitor	during cut-off control or during output clamping	OB –300 µA to +300 µA	
26	Y output hue adjust output	 YEXH = 0 DC 0.8 V to 5.0 V	0.7 mA 0.7 mA	

PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
27	I^2C-bus data input acknowledge output	outside acknowledge during acknowledge	OB less than 0.1 V up to 4 mA due to external pull-up resistor	
28	I^2C-bus serial clock input		OB	

PACKAGE OUTLINE

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.