DATA SHEET

SAA9740H
Advanced Auto Control Function (A2CF)

Product specification
Supersedes data of 1996 Jan 30
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

Advanced Auto Control Function (A2CF) SAA9740H

FEATURES

- One chip full digital Auto Focus (AF), Auto Exposure (AE) and Auto White Balance (AWB)
- Possible to use NTSC and PAL CCD with horizontal resolution of 510, 670, 720 or 768 pixels
- No manual adjustment
- One microprocessor system commonly used with CAMera Digital Signal Processor (CAMDSP) SAA9750H
- 8-bit parallel microprocessor interface
- LQFP64 package (0.5 mm pitch)
- Single 3 V power supply.

Auto Focus features

- Video AF system
- Two windows system (a small centre and large window)
- The window size and place are microprocessor controlled
- Including 5^{th} order IIR digital high-pass filter
- Line peak accumulation in the large window
- High-pass filter's output accumulation in one field.

Auto Exposure features

- 5 windows accumulation
- Calculation of white-clip by centre window
- Possible to control size and place of the centre windows by the light condition with microprocessor.

Auto White Balance features

- Mono colour detection
- Accumulation of UV data in the corresponding UV quadrant
- Green and Magenta elimination gate
- Luminance gate for detecting white
- UV limiter
- White-clip detection/counter.

GENERAL DESCRIPTION

The Advanced Auto Control Function (A2CF) is to be used for a colour CCD camera system. This IC can realize AWB, AF and AE with a microprocessor. This device consists of an input data selector, a parallel 8-bit microprocessor interface, a data accumulator, a window generator, a command decoder and AWB, AF, AE for each processing block.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage (pins 6, 18 and 47)	2.7	3.0	3.3	V
V_{IL}	LOW level digital input voltage	0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level digital input voltage	$0.7V_{DD}$	–	V_{DD}	V
V_{OL}	LOW level digital output voltage	–	–	0.5	V
V_{OH}	HIGH level digital output voltage	$V_{DD} - 0.5$	–	–	V
T_{amb}	operating ambient temperature	–20	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA9740H	LQFP64	plastic low profile quad flat package; 64 leads; body $10 \times 10 \times 1.4$ mm	SOT314-2

BLOCK DIAGRAM

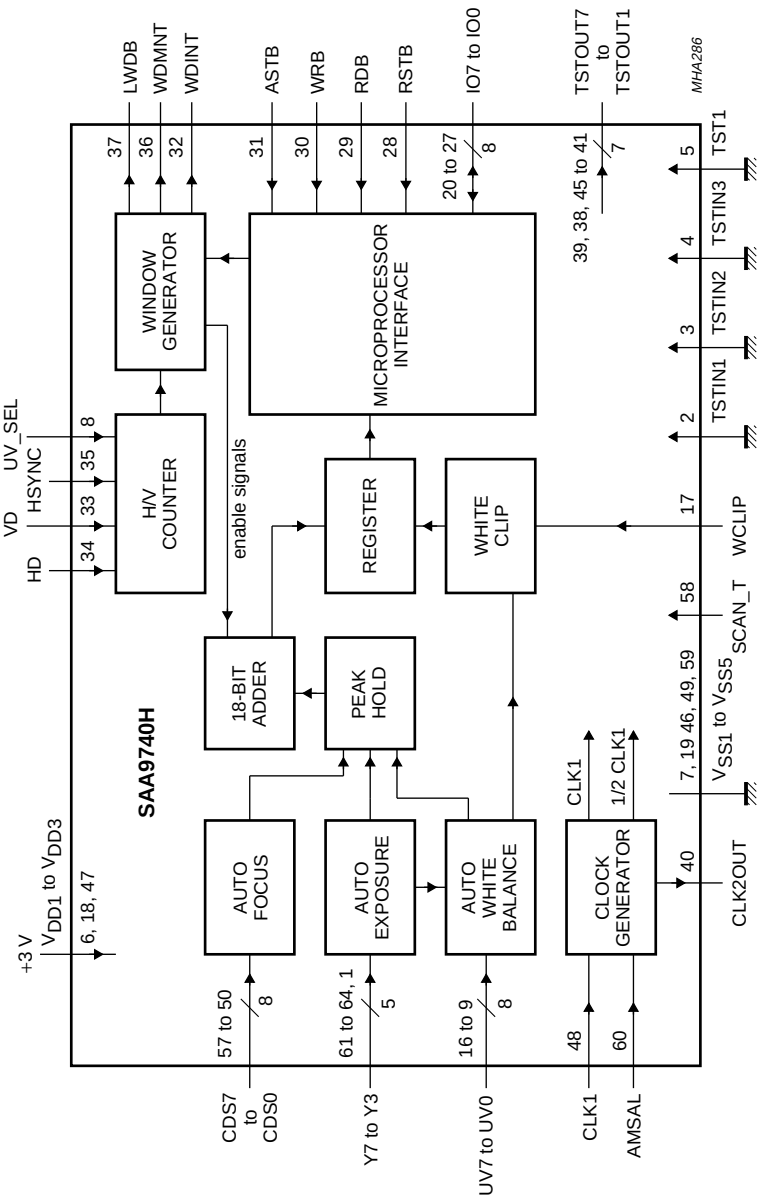


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
Y3	1	input	Y input from SAA9750H (CAMDSP) (LSB)
TSTIN1	2	input	input pin for test
TSTIN2	3	input	input pin for test
TSTIN3	4	input	input pin for test
TST1	5	input	input pin for test
V_{DD1}	6	–	digital supply voltage
V_{SS1}	7	–	ground
UV_SEL	8	input	UV select input from SAA9750H (CAMDSP)
UV0	9	input	UV input from SAA9750H (CAMDSP) (LSB)
UV1	10	input	UV input from SAA9750H (CAMDSP)
UV2	11	input	UV input from SAA9750H (CAMDSP)
UV3	12	input	UV input from SAA9750H (CAMDSP)
UV4	13	input	UV input from SAA9750H (CAMDSP)
UV5	14	input	UV input from SAA9750H (CAMDSP)
UV6	15	input	UV input from SAA9750H (CAMDSP)
UV7	16	input	UV input from SAA9750H (CAMDSP) (MSB)
WCLIP	17	input	white-clip input from SAA9750H (CAMDSP)
V_{DD2}	18	–	digital supply voltage
V_{SS2}	19	–	ground
IO7	20	bidirectional	microprocessor interface (MSB)
IO6	21	bidirectional	microprocessor interface
IO5	22	bidirectional	microprocessor interface
IO4	23	bidirectional	microprocessor interface
IO3	24	bidirectional	microprocessor interface
IO2	25	bidirectional	microprocessor interface
IO1	26	bidirectional	microprocessor interface
IO0	27	bidirectional	microprocessor interface (LSB)
RSTB	28	input	system reset
RDB	29	input	read control from microprocessor
WRB	30	input	write control from microprocessor
ASTB	31	input	address set from microprocessor
WDINT	32	output	window interrupt
VD	33	input	V-drive signal input
HD	34	input	H-drive signal input
HSYNC	35	input	HSYNC input
WDMNT	36	output	window monitor for test (open-drain)
LWDB	37	output	large window for test (open-drain)
TSTOUT6	38	output	output pin for test
TSTOUT7	39	output	output pin for test
CLK2OUT	40	output	output pin of internal clock (open-drain)

SYMBOL	PIN	TYPE	DESCRIPTION
TSTOUT1	41	output	output pin for test
TSTOUT2	42	output	output pin for test
TSTOUT3	43	output	output pin for test
TSTOUT4	44	output	output pin for test
TSTOUT5	45	output	output pin for test
V_{SS3}	46	–	ground
V_{DD3}	47	–	digital supply voltage
CLK1	48	input	clock
V_{SS4}	49	–	ground
CDS0	50	input	CDS input from ADC (LSB)
CDS1	51	input	CDS input from ADC
CDS2	52	input	CDS input from ADC
CDS3	53	input	CDS input from ADC
CDS4	54	input	CDS input from ADC
CDS5	55	input	CDS input from ADC
CDS6	56	input	CDS input from ADC
CDS7	57	input	CDS input from ADC (MSB)
SCAN_T	58	input	test control for scan test
V_{SS5}	59	–	ground
AMSAL	60	input	for testing
Y7	61	input	Y input from SAA9750H (CAMDSP) (MSB)
Y6	62	input	Y input from SAA9750H (CAMDSP)
Y5	63	input	Y input from SAA9750H (CAMDSP)
Y4	64	input	Y input from SAA9750H (CAMDSP)

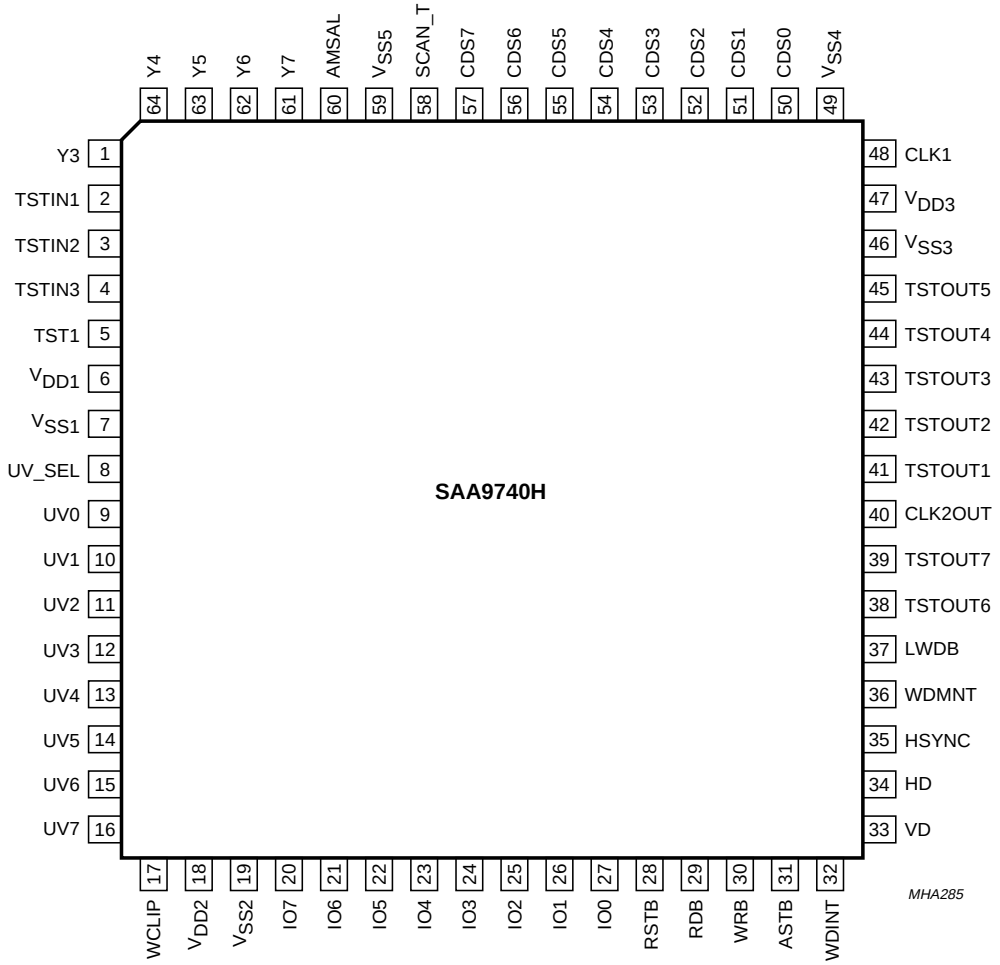


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The Advanced Auto Control Function (A2CF) will be used for colour CCD camera systems.

The input signals are CDS (AF data) from 8-bit ADC, Y (for AE, 5-bit) and UV (for AWB, 8-bit) data as the output of SAA9750H (CAMDSP) and they are fed into the A2CF. After being processed in the A2CF, corresponding data are led into the microprocessor.

Together with the zoom encoder and focus sensor output the microprocessor does the following control with the data of A2CF:

- Control focus motor
- Control iris, AGC (via DAC) and high speed shutter
- Send the control data to SAA9750H (CAMDSP) via serial bus.

CLK1 is depending on the CCD type. To cope with the different CCD clocks, some reference data have to be set by the microprocessor.

AF system

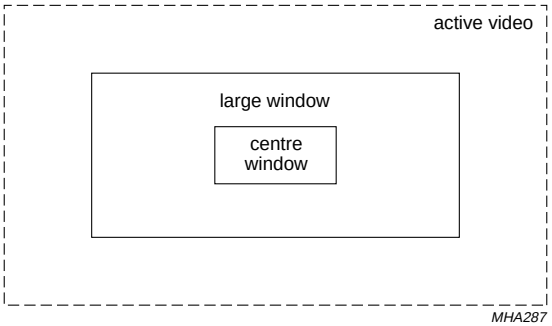


Fig.3 AF window.

Digital CDS signals CDS7 to CDS0 which come after AGC, gamma processing and ADC are fed into A2CF. This 8-bit data is shifted to the most suitable 6-bit data for AF processing by microprocessor. For example, when the MSB of them is ‘1’ then the 6-bit data is shifted by the microprocessor to CDS7 to CDS2 (not CDS6 to CDS1 or CDS5 to CDS0; see Table 4). After AF shifting the signals go through an LPF and they are down sampled. The down sampling is done by CLK2 (CLK1/2). In order to detect the high frequency component for AF processing, one HPF is added. This output is the focus value. Next peak hold block is for acquiring maximum focus value of every line in one field.

This maximum focus value is accumulated in the AF window (see Fig.3) by the 18-bit adder. The values in the large window are stored in REG2 (see Table 7) and those in the small window are stored in REG3 (see Table 7). Which data is used is dependent on the software (see Tables 6 and 7). Besides this accumulation, line peak accumulation is also done. This data is the maximum value in one field and is stored in REG0 (see Table 7).

AE system

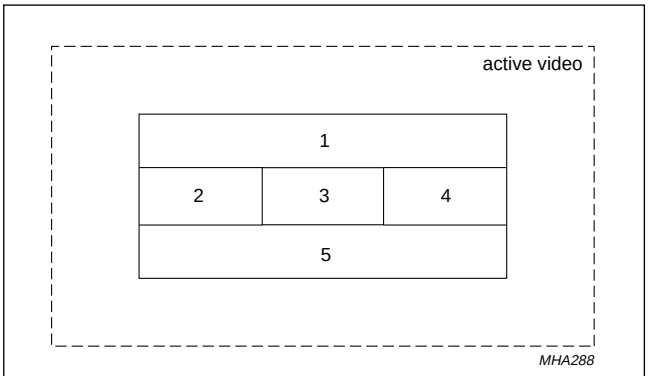


Fig.4 AE window.

5-bit Y signals Y7 to Y3 which come from SAA9750H are fed into A2CF for AE processing. This signal is internally extended to 6 bits by adding a ‘0’ as new MSB. Next they go through an LPF and they are down sampled in the same way as AF processing. In order to prevent overflow of the 18-bit adder block, 2 modes exist (see Table 4). The first is H decimation is **on** or **off**. If H decimation is **on**, then the data for AE processing is available in every other line. The second mode is that the data for AE processing is shifted to $\frac{1}{2}$ or not. If the data is shifted to $\frac{1}{2}$, it is done before down sampling and before the data going to the 18-bit adder becomes $\frac{1}{2}$. Both these modes are controlled by the microprocessor. In AE mode there are 5 windows as shown in Fig.4. These windows are controlled by the microprocessor. The accumulation data in window 1 to window 5 is respectively stored in REG1 to REG5 (see Table 7). The white-clip count data in the centre window is stored to the lower 5 bits of REG0 (see Table 7).
The upper 3 bits of REG0 is the overflow information in the 18-bit adder (see Table 7).

AWB system

8-bit UV signals UV[7] to UV[0] which come from the SAA9750H (CAMDSP) are fed into the A2CF for AWB processing. First the 8-bit data is limited to 6-bits because the necessary data for AWB processing is around the white colour signal. Then these signals go through an LPF and they are down sampled. They are separated to U and V signals by using UV_SEL coming from SAA9750H (CAMDSP). As shown in Table 1, in the large window these signals are compared with the threshold that is set by the microprocessor. If the conditions shown in Fig.8 are valid, the data is available for AWB processing. If the conditions aren't valid, the data is ignored. The available data in the first to the 4th quadrant are stored in respectively REG1 to REG4 (see Table 7). The AWB (Δ) mode (see Table 4) is for detecting whether the picture is mono colour or not. If the AWB (B – Y) or AWB (R – Y) or AWB (Δ) (see Table 4) mode is active and white-clip or AWB limited (as mentioned above), then the counts of them are stored in the lower 5 bits of REG0 (see Table 7). In the AWB Y mode the lower 4 bits of REG0 are contrast peak data in one field and the 4th bit is the overflow information of the AF (see Table 7).

Microprocessor interface

8-bit data bus and 3 control ports are prepared (WRB, RDB and ASTB) for microprocessor interface in A2CF for quick data access instead of serial bus. A2CF has 11 read commands and 13 write commands.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+5.0	V
P_{tot}	total power dissipation	–	83	mW
V_I	input voltage	–0.5	V_{DD} + 0.5	V
V_O	output voltage	–0.5	V_{DD} + 0.5	V
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	operating ambient temperature	–20	+70	°C
V_{es}	electrostatic handling; note 1	–2000	+2000	V
LTCH	latch-up protection	100	–	mA

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

T_{amb} = −20 to +70 °C; V_{DD} = 2.7 to 3.3 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DD}	supply current	note 1	–	12	25	mA
Input pins (TSTIN1 to TSTIN3, TST1, UV_SEL, UV0 to UV7, Y3 to Y7, WCLIP, RSTB, RDB, WRB, ASTB, VD, HD, HSYNC, CLK1, CDS0 to CDS7, SCAN_T and AMSAL)						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
I_{IH}	HIGH level input current	$V_{IH} = V_{DD}$	–	–	1	µA
I_{IL}	LOW level input current	$V_{IL} = V_{SS}$	–	–	–1	µA
Output pins (WDINT and TSTOUT1 to TSTOUT7; push pull output)						
V_{OH}	HIGH level output voltage	I_{OH} = –20 µA	$V_{DD} – 0.1$	–	–	V
		I_{OH} = –4 mA	$V_{DD} – 0.5$	–	–	V
V_{OL}	LOW level output voltage	I_{OL} = +20 µA	–	–	0.1	V
		I_{OL} = +4 mA	–	–	0.5	V
Output pins (WDMNT, LWDB and CLK2OUT; open-drain)						
V_{OL}	LOW level output voltage	I_{OL} = +20 µA	–	–	0.1	V
		I_{OL} = +4 mA	–	–	0.5	V
I_{OZ}	3-state leakage current	$V_O = V_{DD}$	–	–	5	µA
Bidirectional pins (IO0 to IO7)						
V_{OH}	HIGH level output voltage	I_{OH} = –20 µA	$V_{DD} – 0.1$	–	–	V
		I_{OH} = –8 mA	$V_{DD} – 0.5$	–	–	V
V_{OL}	LOW level output voltage	I_{OL} = +20 µA	–	–	0.1	V
		I_{OL} = +8 mA	–	–	0.5	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
I_{IH}	HIGH level input current	$V_{IH} = V_{DD}$	–	–	1	µA
I_{IL}	LOW level input current	$V_{IL} = V_{SS}$	–	–	–1	µA
I_{OZ}	3-state leakage current	$V_O = V_{DD}$ or V_{SS}	–	–	±5	µA

Note

1. 510H PAL; V_{DD} = 3 V; all modes active.

AC CHARACTERISTICS

Microprocessor interface

T_{amb} = –20 to +70 °C; V_{DD} = 2.7 to 3.3 V; V_{IL} = 0 V; V_{IH} = V_{DD}; V_{ref} = 0.5V_{DD}; input t_r and t_f = 30 ns; see Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{suAD}	address setup time		0.4	–	–	µs
t_{hAD}	address hold time		0.4	–	–	µs
t_{AR}	ASTB to RDB time		0.5	–	–	µs
$t_{W\,R}$	RDB width		1.0	–	–	µs
t_{RRD}	RDB to read data	R_L = 1 kΩ	–	–	0.8	µs
t_{hRRD}	RDB to read data hold time	R_L = 1 kΩ	–	–	0.1	µs
t_{AW}	ASTB to WRB time		0.5	–	–	µs
$t_{W\,W}$	WRB width		1.0	–	–	µs
t_{suW}	WRB setup time		0.4	–	–	µs
t_{hW}	WRB hold time		0.4	–	–	µs

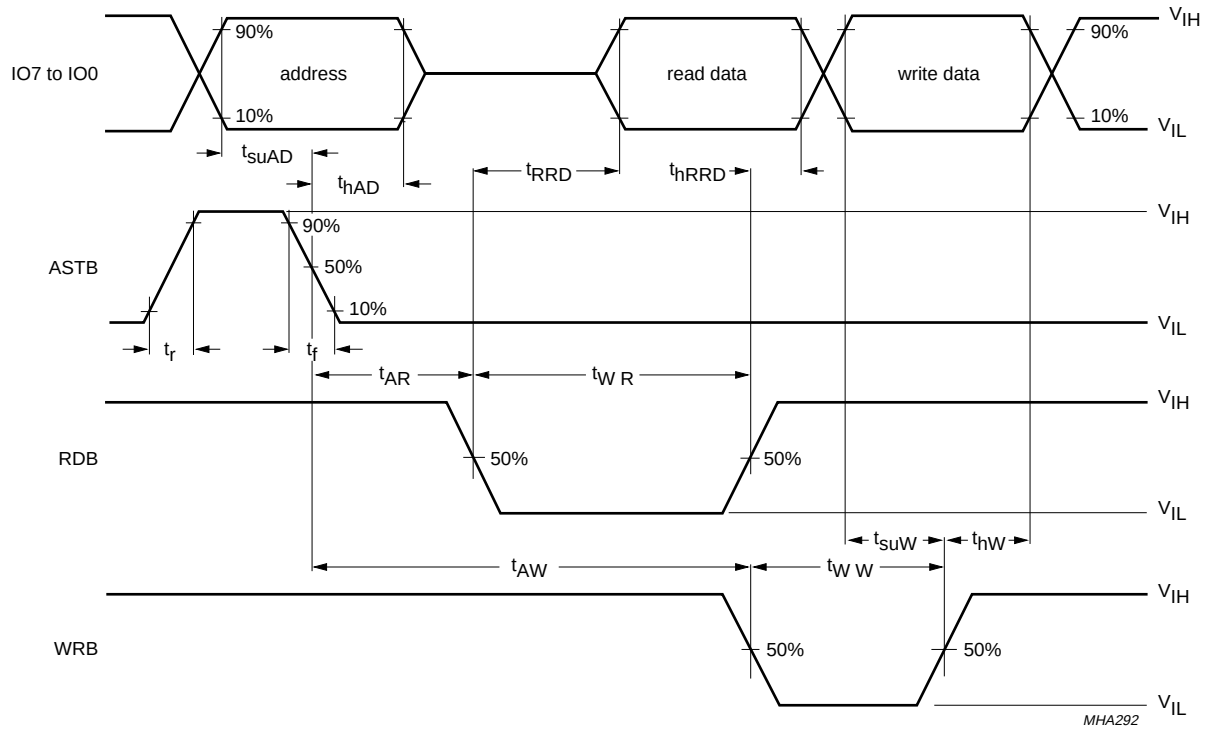


Fig.5 Microprocessor interface timing.

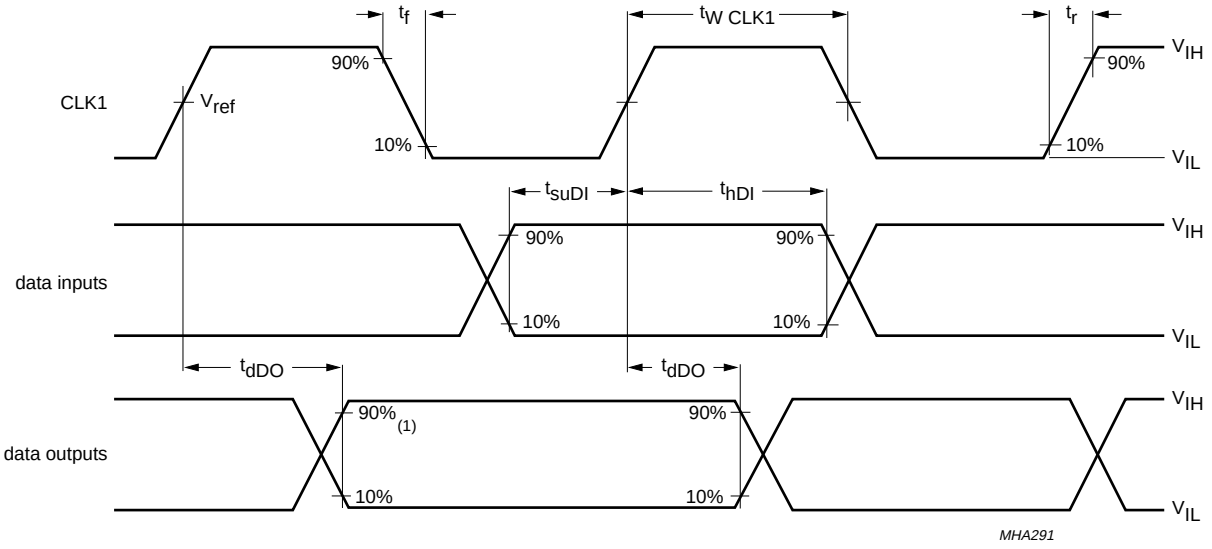
Data input/output timing (CLK1)

T_{amb} = −20 to +70 °C; V_{DD} = 2.7 to 3.3 V; V_{IL} = 0 V; V_{IH} = V_{DD}; V_{ref} = 0.5V_{DD}; t_r and t_f = 6 ns; output load capacitance = 20 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{suDI}	data input setup time	note 1	5	–	–	ns
t_{hDI}	data input hold time	note 1	8	–	–	ns
t_{dDO}	data output delay time	notes 2 and 3	–	–	60	ns
t_{hDO}	data output hold time	notes 2 and 3	–	–	60	ns
$t_{W\ CLK1}$	width of CLK1		–	50	–	%

Notes

1. Data inputs: UV0 to UV7, Y3 to Y7, AD0 to AD7, UV_SEL, HSYNC, HD, VD and WCLIP.
2. Data outputs: WDINT, CLK2OUT, WDMNT and LWDB (open-drain outputs with 1 kΩ output load resistor).
3. T_{amb} = 25 °C; V_{DD} = 3.0 V.



(1) 50% for open-drain outputs.

Fig.6 Data input/output timing (CLK1).

MICROPROCESSOR COMMANDS

Table 1 Write commands; note 1

COMMAND	DATA								FUNCTION
	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	
81H(2)	X	X	X1[5]	X1[4]	X1[3]	X1[2]	X1[1]	X1[0]	X1 address
82H(2)	X	X	X2[5]	X2[4]	X2[3]	X2[2]	X2[1]	X2[0]	X2 address
83H(2)	X	X	X3[5]	X3[4]	X3[3]	X3[2]	X3[1]	X3[0]	X3 address
84H(2)	X	X	X4[5]	X4[4]	X4[3]	X4[2]	X4[1]	X4[0]	X4 address
85H(2)	X	X	Y1[5]	Y1[4]	Y1[3]	Y1[2]	Y1[1]	Y1[0]	Y1 address
86H(2)	X	X	Y2[5]	Y2[4]	Y2[3]	Y2[2]	Y2[1]	Y2[0]	Y2 address
87H(2)	X	X	Y3[5]	Y3[4]	Y3[3]	Y3[2]	Y3[1]	Y3[0]	Y3 address
88H(2)	X	X	Y4[5]	Y4[4]	Y4[3]	Y4[2]	Y4[1]	Y4[0]	Y4 address
8BH	X	TEST2	TEST1	TEST0	X	IIRC2	IIRC1	IIRC0	IIRC
8CH	THB[3]	THB[2]	THB[1]	THB[0]	THA[3]	THA[2]	THA[1]	THA[0]	TH1
8DH	X	X	X	X	THC[3]	THC[2]	THC[1]	THC[0]	TH2
8EH	SFTY	SFT1	SFT0	X	HON	MODE2	MODE1	MODE0	MODE
8FH	X	SIZE	MWD1	MWD0	X	PHS	PHD	PVD	SET

Notes

1. X = don't care.
2. For auto exposure processing different windows in the active video field are taken with different weighting factors. The coordinates of the five windows are set according to Fig.7. The resolution is 1 bit ≡ 16 pixel in x-direction and 1 bit ≡ 8 lines in y-direction.

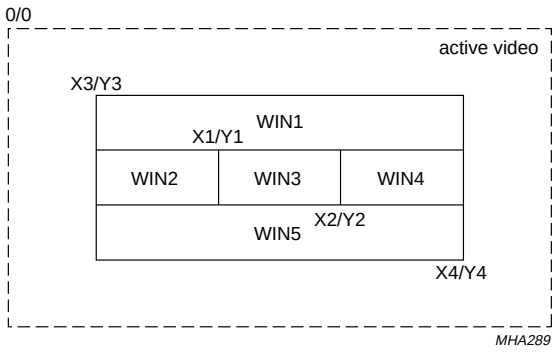


Fig.7 Window size control for AE processing (see WRITE command 81H to 88H).

Address 8BH

Table 2 IIRC (IO[2] to IO[0])

IIRC2	IIRC1	IIRC0	FUNCTION
0	0	0	1 MHz HPF select for auto focus processing
0	0	1	700 kHz HPF select for auto focus processing
0	1	0	220 kHz HPF select for auto focus processing
0	1	1	bypass HPF for auto focus processing
1	1	0	110 kHz select for auto focus processing

Table 3 IIRC 9IO[6] to 9IO[4]; note 1

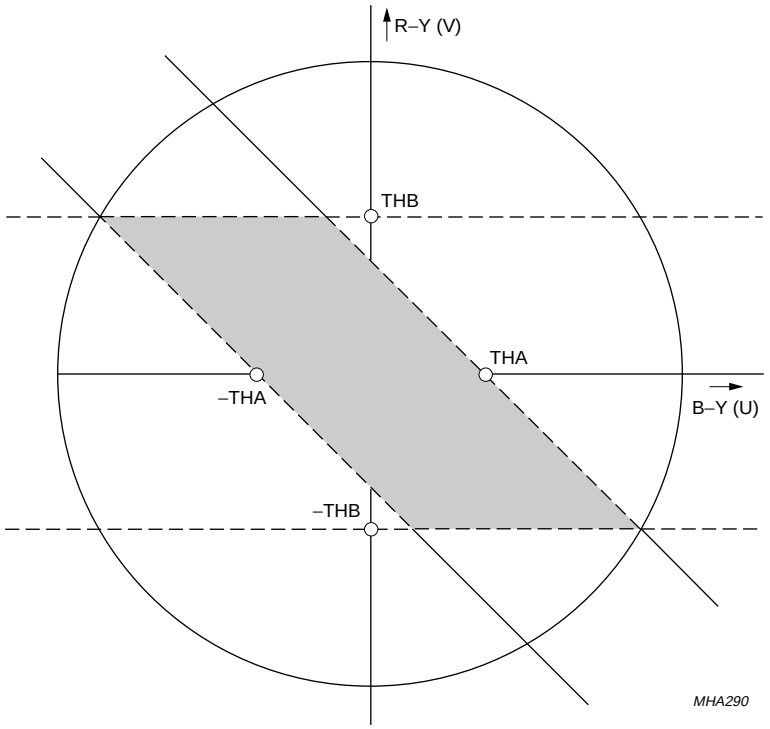
TEST2	TEST1	TEST0	FUNCTION
X	X	X	only for test purposes

Note

1. X = don't care.

Address 8CH and 8DH

Address 8CH and 8DH are used to define the active range that is taken for auto white balance processing. The calculation of active area can be seen in Fig.8.



Conditions:
(1) |U + V| < THA.
(2) |V| < THB.
(3) Y > THC.
Threshold values can be set with 4-bit resolution.

Fig.8 Set threshold values for Auto White Balance (AWB) mode.

Address 8EH

By applying address 8EH and setting the MODE bits it is possible to read the values that are stored in the registers corresponding to the selected mode. The selection which register will be read is then defined by READ address 70H to 7BH (see Tables 6 and 7).

Table 4 MODE and shift definition (see WRITE command 8EH); note 1

IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	MODE	FUNCTION
SFTY	SFT1	SFT0	–	HON	MODE	MODE	MODE		
X	X	X	X	X	0	0	0	AE	set mode: read AE values
X	X	X	X	X	0	0	1	AF	set mode: read AF values
X	X	X	X	X	0	1	1	AWB (B – Y)	set mode: read AWB (B – Y) values
X	X	X	X	X	1	0	0	AWB (R – Y)	set mode: read AWB (R – Y) values
X	X	X	X	X	1	0	1	AWB Δ	set mode: read AWB Δ values
X	X	X	X	X	1	1	0	AWB Y	set mode: read AWB Y values
X	X	X	X	0	0	0	0	H dec	decimation for 1H **off**
X	X	X	X	1	0	0	0	H dec	decimation for 1H **on**
X	0	0	X	X	0	0	1	AF shift	select CDS5 to CDS0 for AF processing
X	0	1	X	X	0	0	1	AF shift	select CDS6 to CDS1 for AF processing
X	1	X	X	X	0	0	1	AF shift	select CDS7 to CDS2 for AF processing
0	X	X	X	X	0	0	0	AE shift	take AE[5] to AE[0] for internal AE processing (see Chapter “Functional description”)
1	X	X	X	X	0	0	0	AE shift	take AE[5] to AE[1] for internal AE processing (see Chapter “Functional description”)

Note

1. X = don’t care.

Address 8FH

To apply several types of CCDs it is possible to set polarity VD, HD and HSYNC by PVD, PHD and PHS.

The modes set by MWD and SIZE bit are only used for system evaluation. During normal application mode they can have any value.

Table 5 Settings (see WRITE command 8FH); note 1

IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	MODE	FUNCTION
–	SIZE	MWD1	MWD0	–	PHS	PHD	PVD		
X	X	X	X	X	X	X	0	PVD	VD ‘H’ active
X	X	X	X	X	X	X	1	PVD	VD ‘L’ active
X	X	X	X	X	X	0	X	PHD	HD ‘H’ active
X	X	X	X	X	X	1	X	PHD	HD ‘L’ active
X	X	X	X	X	0	X	X	PHSYNC	HSYNC ‘H’ active
X	X	X	X	X	1	X	X	PHSYNC	HSYNC ‘L’ active
X	X	0	0	X	X	X	X	MWD AE	monitor AE window
X	X	0	1	X	X	X	X	MWD AF	monitor AF window
X	X	1	0	X	X	X	X	MWD AWB	monitor AWB window
X	X	1	1	X	X	X	X	MWD ALL	monitor all windows
X	0	X	X	X	X	X	X	MWD SMALL	monitor small window
X	1	X	X	X	X	X	X	MWD LARGE	monitor large window

Note

1. X = don’t care.

READ commands

The values of the internal registers can be read as follows:

1. Set mode AF, AE or AWB by WRITE command 8EH according to Table 4.
2. Select register by READ command 70H to 7BH according to Table 6.

Table 6 Read command

COMMAND	DATA								FUNCTION
	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	
70H	O[15]	O[14]	O[13]	O[12]	O[11]	O[10]	O[9]	O[8]	REG1
71H	O[7]	O[6]	O[5]	O[4]	O[3]	O[2]	O[1]	O[0]	
72H	O[15]	O[14]	O[13]	O[12]	O[11]	O[10]	O[9]	O[8]	REG2
73H	O[7]	O[6]	O[5]	O[4]	O[3]	O[2]	O[1]	O[0]	
74H	O[15]	O[14]	O[13]	O[12]	O[11]	O[10]	O[9]	O[8]	REG3
75H	O[7]	O[6]	O[5]	O[4]	O[3]	O[2]	O[1]	O[0]	
76H	O[15]	O[14]	O[13]	O[12]	O[11]	O[10]	O[9]	O[8]	REG4
77H	O[7]	O[6]	O[5]	O[4]	O[3]	O[2]	O[1]	O[0]	
78H	O[15]	O[14]	O[13]	O[12]	O[11]	O[10]	O[9]	O[8]	REG5
79H	O[7]	O[6]	O[5]	O[4]	O[3]	O[2]	O[1]	O[0]	
7BH	O[7]	O[6]	O[5]	O[4]	O[3]	O[2]	O[1]	O[0]	REG0

Register assignment

For the different modes (AF, AE and AWB) the contents of the registers are assigned according to Table 7.

Table 7 Register assignment

MODE	REGISTER	DATA	FUNCTION
AF	REG0 (8-bit)	O[7] to O[5]	n.a.
		O[4]	overflow information of AF block
		O[3] to O[0]	contrast peak within one field
	REG1 (18-bit)	O[15] to O[0]	n.a.
	REG2 (18-bit)	O[15] to O[0]	accumulated data in the large window
	REG3 (18-bit)	O[15] to O[0]	accumulated data in the centre window
	REG4 (18-bit)	O[15] to O[0]	accumulated data of the large window minus the data of the centre window
	REG5 (18-bit)	O[15] to O[0]	n.a.
AE	REG0 (8-bit)	O[7] to O[5]	18-bit adder overflow information
		O[4] to O[0]	white-clip counter output
	REG1 (18-bit)	O[15] to O[0]	accumulated data in WIN1; REG1[18] to REG1[3]
	REG2 (18-bit)	O[15] to O[0]	accumulated data in WIN2; REG2[18] to REG2[3]
	REG3 (18-bit)	O[15] to O[0]	accumulated data in WIN3; REG3[18] to REG3[3]
	REG4 (18-bit)	O[15] to O[0]	accumulated data in WIN4; REG4[18] to REG4[3]
	REG5 (18-bit)	O[15] to O[0]	accumulated data in WIN5; REG5[18] to REG5[3]
AWB (B – Y)	REG0 (8-bit)	O[7] to O[5]	n.a.
		O[4] to O[0]	white-clip or AWB limiter count
	REG1 (18-bit)	O[15] to O[0]	accumulated B – Y data of 1st quadrant; REG1[18] to REG1[3]
	REG2 (18-bit)	O[15] to O[0]	accumulated B – Y data of 2nd quadrant; REG2[18] to REG2[3]
	REG3 (18-bit)	O[15] to O[0]	accumulated B – Y data of 3rd quadrant; REG3[18] to REG3[3]
	REG4 (18-bit)	O[15] to O[0]	accumulated B – Y data of 4th quadrant; REG4[18] to REG4[3]
	REG5 (18-bit)	O[15] to O[0]	n.a.
AWB (R – Y)	REG0 (8-bit)	O[7] to O[5]	n.a.
		O[4] to O[0]	white-clip or AWB limiter count
	REG1 (18-bit)	O[15] to O[0]	accumulated R – Y data of 1st quadrant; REG1[18] to REG1[3]
	REG2 (18-bit)	O[15] to O[0]	accumulated R – Y data of 2nd quadrant; REG2[18] to REG2[3]
	REG3 (18-bit)	O[15] to O[0]	accumulated R – Y data of 3rd quadrant; REG3[18] to REG3[3]
	REG4 (18-bit)	O[15] to O[0]	accumulated R – Y data of 4th quadrant; REG4[18] to REG4[3]
	REG5 (18-bit)	O[15] to O[0]	n.a.
AWB (Δ)	REG0 (8-bit)	O[7] to O[5]	n.a.
		O[4] to O[0]	white-clip or AWB limiter count
	REG1 (18-bit)	O[15] to O[0]	accumulated Δ(R – Y) data of WIN1 to WIN5; REG1[18] to REG1[3]
	REG2 (18-bit)	O[15] to O[0]	accumulated Δ(B – Y) data of WIN1 to WIN5; REG2[18] to REG2[3]
	REG3 (18-bit)	O[15] to O[0]	accumulated Δ(R – Y) data of WIN3; REG3[18] to REG3[3]
	REG4 (18-bit)	O[15] to O[0]	accumulated Δ(B – Y) data of WIN3; REG4[18] to REG4[3]
	REG5 (18-bit)	O[15] to O[0]	n.a.

MODE	REGISTER	DATA	FUNCTION
AWB (Y)	REG0 (8-bit)	O[7] to O[5]	n.a.
		O[4]	overflow information of auto focus block
		O[3] to O[0]	contrast peak within one field
	REG1 (18-bit)	O[15] to O[0]	accumulated R – Y data of 1st quadrant; REG1[18] to REG1[3]
	REG2 (18-bit)	O[15] to O[0]	accumulated R – Y data of 2nd quadrant; REG2[18] to REG2[3]
	REG3 (18-bit)	O[15] to O[0]	accumulated R – Y data of 3rd quadrant; REG3[18] to REG3[3]
	REG4 (18-bit)	O[15] to O[0]	accumulated R – Y data of 4th quadrant; REG4[18] to REG4[3]
	REG5 (18-bit)	O[15] to O[0]	n.a.

APPLICATION INFORMATION

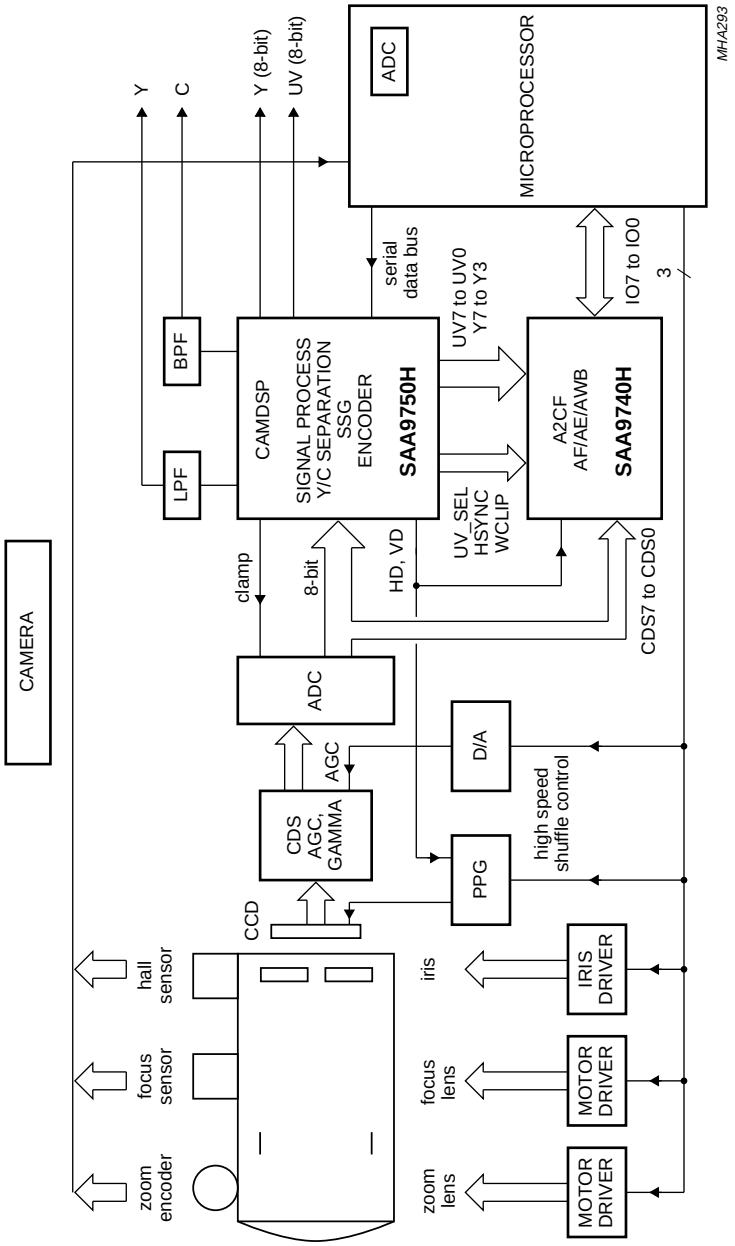
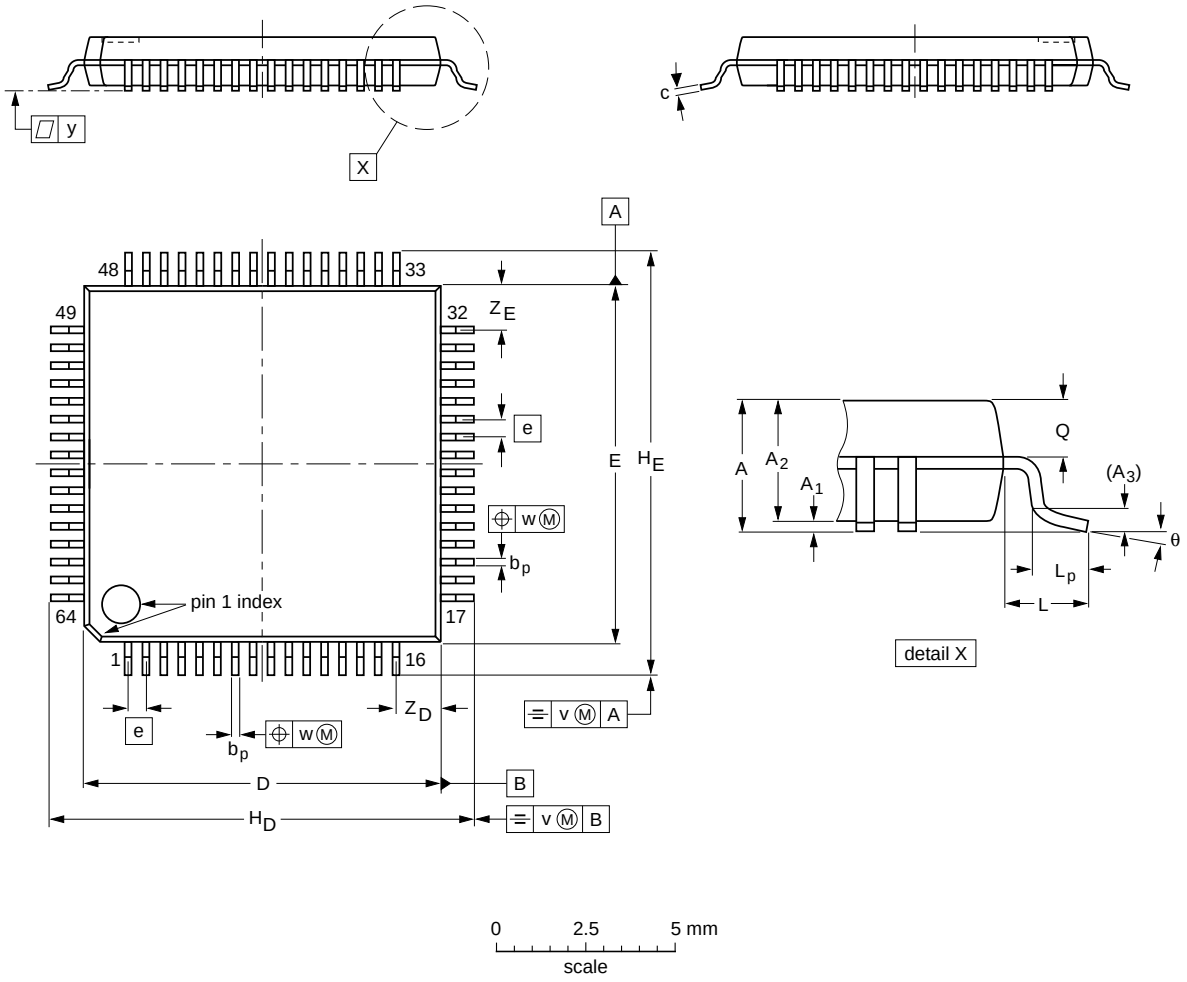


Fig.9 Camera block diagram (SAA9750H and SAA9740H).

PACKAGE OUTLINE

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						~~94-01-07~~ 95-12-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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