DATA SHEET

SAA7165
Video Enhancement and Digital-to-Analog processor (VEDA2)

Product specification
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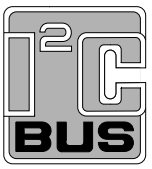
SAA7165

FEATURES



- CMOS circuit to enhance video data and to convert luminance and colour-difference signals from digital-to-analog
- Digital Colour Transient Improvement block (DCTI) to increase the sharpness of colour transitions. The improved pin-compatible SAA7165 can supersede the SAA9065
- 16-bit parallel input for 4 : 1 : 1 and 4 : 2 : 2 YUV data
- Data clock input LLC (Line-Locked Clock) for a data rate up to 36 MHz
- 8-bit luminance and 8-bit multiplexed colour-difference formats (7-bit formats optional)
- MC input to support various clock and pixel rates
- Formatting YUV input data; 4 : 2 : 2 format, 4 : 1 : 1 format and filter characteristics selectable
- HREF input to determine the active line (number of pixels)
- Controllable peaking of luminance signal
- Coring stage with controllable threshold to eliminate noise in luminance signal
- Interpolation filter suitable for both formats to increase the data rate in chrominance path
- Polarity of colour-difference signals selectable
- All functions controlled via I^2C-bus
- Separate digital-to-analog converters (9-bit resolution for Y; 8-bit for colour-difference signals)
- 1 V (p-p)/75 Ω outputs realized by two resistors
- No external adjustments.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	5	5.5	V
V_{DDA}	analog supply voltage	4.75	5	5.25	V
$I_{DD(tot)}$	total supply current	–	tbf	–	mA
V_{IL}	LOW-level input voltage on YUV-bus	–0.5	–	+0.8	V
V_{IH}	HIGH-level input voltage on YUV-bus	2	–	V_{DDD} + 0.5	V
f_{LLC}	input data rate	–	–	36	MHz
$V_{o(p-p)}$	output signals Y, (R – Y) and (B – Y) (peak-to-peak value)	–	2	–	V
R_L	output load resistance	125	–	–	Ω
ILE	DC integral linearity error in output signal (8-bit data)	–	–	1	LSB
DLE	DC differential error in output signal (8-bit data)	–	–	0.5	LSB
T_{amb}	operating ambient temperature range	0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7165WP	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2

BLOCK DIAGRAM

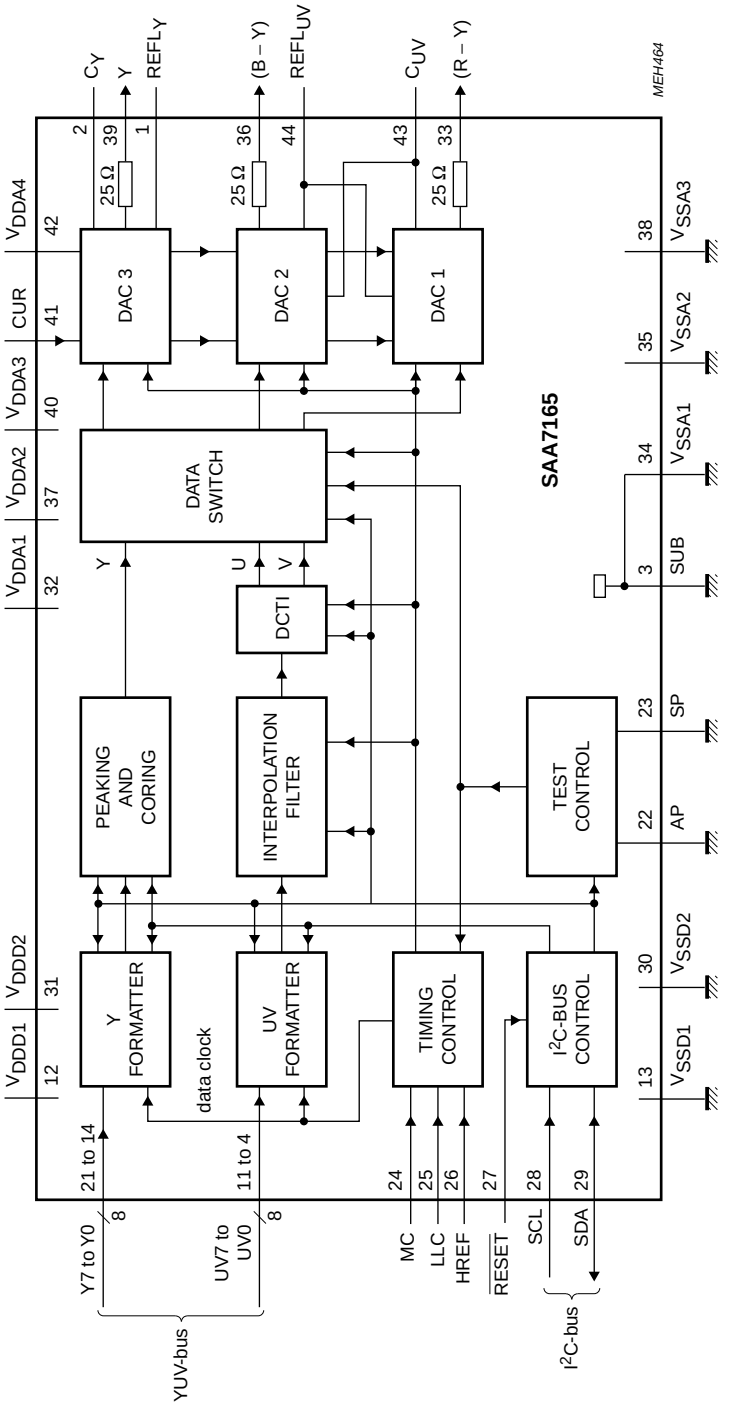


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$REFL_Y$	1	low reference of luminance DAC (connected to V_{SSA1})
C_Y	2	capacitor for luminance DAC (high reference)
SUB	3	substrate (connected to V_{SSA1})
UV0	4	UV signal input bit UV7 (digital colour-difference signal)
UV1	5	UV signal input bit UV6 (digital colour-difference signal)
UV2	6	UV signal input bit UV5 (digital colour-difference signal)
UV3	7	UV signal input bit UV4 (digital colour-difference signal)
UV4	8	UV signal input bit UV3 (digital colour-difference signal)
UV5	9	UV signal input bit UV2 (digital colour-difference signal)
UV6	10	UV signal input bit UV1 (digital colour-difference signal)
UV7	11	UV signal input bit UV0 (digital colour-difference signal)
V_{DDD1}	12	+5 V digital supply voltage 1
V_{SSD1}	13	digital ground 1 (0 V)
Y0	14	Y signal input bit Y7 (digital luminance signal)
Y1	15	Y signal input bit Y6 (digital luminance signal)
Y2	16	Y signal input bit Y5 (digital luminance signal)
Y3	17	Y signal input bit Y4 (digital luminance signal)
Y4	18	Y signal input bit Y3 (digital luminance signal)
Y5	19	Y signal input bit Y2 (digital luminance signal)
Y6	20	Y signal input bit Y1 (digital luminance signal)
Y7	21	Y signal input bit Y0 (digital luminance signal)
AP	22	connected to ground (action pin for testing)
SP	23	connected to ground (shift pin for testing)
MC	24	data clock CREF (e.g. 13.5 MHz); at MC = HIGH, the LLC divider-by-two is inactive
LLC	25	line-locked clock signal (LL27 = 27 MHz)
HREF	26	data clock for YUV data inputs (for active line 768Y or 640Y long)
$\overline{RESET}$	27	reset input (active LOW)
SCL	28	I^2C-bus clock line
SDA	29	I^2C-bus data line
V_{SSD2}	30	digital ground 2 (0 V)
V_{DDD2}	31	+5 V digital supply voltage 2
V_{DDA1}	32	+5 V analog supply voltage for buffer of DAC 1
(R – Y)	33	±(R – Y) output signal (analog signal)
V_{SSA1}	34	analog ground 1 (0 V)
V_{SSA2}	35	analog ground 2 (0 V)
(B – Y)	36	±(B – Y) output signal (analog colour-difference signal)
V_{DDA2}	37	+5 V analog supply voltage for buffer of DAC 2
V_{SSA3}	38	analog ground 3 (0 V)
Y	39	Y output signal (analog luminance signal)
V_{DDA3}	40	+5 V analog supply voltage for buffer of DAC 3

SYMBOL	PIN	DESCRIPTION
CUR	41	current input for analog output buffers
V_{DDA4}	42	supply and reference voltage for the three DACs
C_{UV}	43	capacitor for chrominance DACs (high reference)
$REFL_{UV}$	44	low reference of chrominance DACs (connected to V_{SSA1})

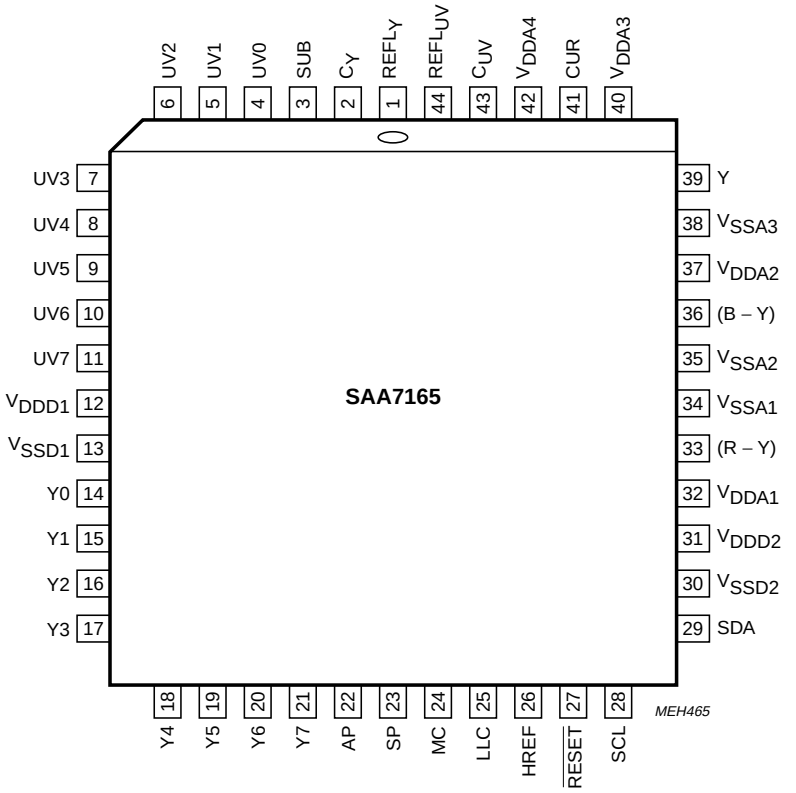


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The CMOS circuit SAA7165 processes digital YUV-bus data up to a data rate of 36 MHz. The data inputs Y7 to Y0 and UV7 to UV0 (see Fig.1) are provided with 8-bit data. The data of digital colour-difference signals U and V are in a multiplexed state (serial in 4 : 2 : 2 or 4 : 1 : 1 format; Tables 2 and 3).

Data is read with the rising edge of LLC (Line-Locked Clock) to achieve a data rate of LLC at MC = HIGH only. If MC is supplied with the frequency CREF (½LLC for example), data is read only at every second rising edge (see Fig.3).

The 7-bit YUV input data are also supported by means of bit R78 (R78 = 0). Additionally, the luminance data format is converted for internal use into a two´s complement format by inverting the MSB. The Y input byte (bits Y7 to Y0) represents luminance information; the UV input byte (bits UV7 to UV0) represents one of the two digital colour-difference signals in 4 : 2 : 2 format (Table 2).

The HREF input signal (HREF = HIGH) determines the start and the end of an active line (see Fig.3) and the number of pixels respectively. The analog output Y is blanked at HREF = LOW, the (B – Y) and (R – Y) outputs are in a colourless state. The blanking level can be set with bit BLV. The SAA7165 is controllable via the I²C-bus.

Formatting Y and UV

The input data formats are formatted into the internally used processing formats (separate for 4 : 2 : 2 and 4 : 1 : 1 formats). The IFF, IFC and IFL bits control the input data format and determine the right interpolation filter (see Figs 10 to 13).

Peaking and coring

Peaking is applied to the Y signal to compensate several bandwidth reductions of the external pre-processing. Y signals can be improved to obtain a better sharpness. There are the two switchable bandpass filters BF1 and BF2 controlled via the I²C-bus by the bits BP1, BP0 and BFB. Thus, a frequency response is achieved in combination with the peaking factor K (Figs 5 to 9; K is determined by the bits BFB, WG1 and WG0).

The coring stage with controllable threshold (4 states controlled by CO1 and CO0 bits) reduces noise disturbances (generated by the bandpass gain) by suppressing the amplitude of small high-frequent signal components. The remaining high-frequent peaking component is available for a weighted addition after coring.

Table 1 LLC and MC configuration modes in DMSD applications (note 1)

PIN	INPUT SIGNAL	DESCRIPTION
LLC	LLC (LL27)	The data rate on YUV-bus is half the clock rate on pin LLC, e.g. in SAA7151B, SAA7191 and SAA7191B single scan operation.
MC	CREF	
LLC	LLC (LL27)	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e.g. in double scan applications.
MC	MC = HIGH	
LLC	LLC (LL27)	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e.g. SAA9051 single scan operation.
MC	MC = HIGH	

Note

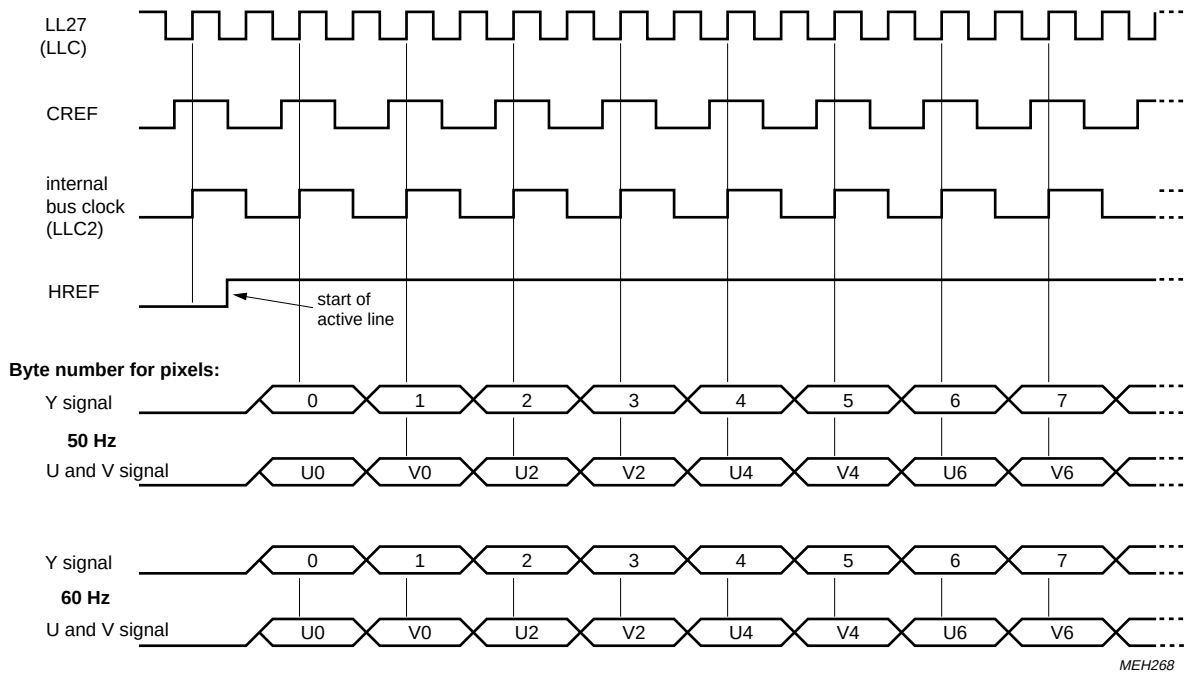
1. YUV data are only latched with the rising edge of LCC at MC = HIGH.

Table 2 Data format 4 : 2 : 2

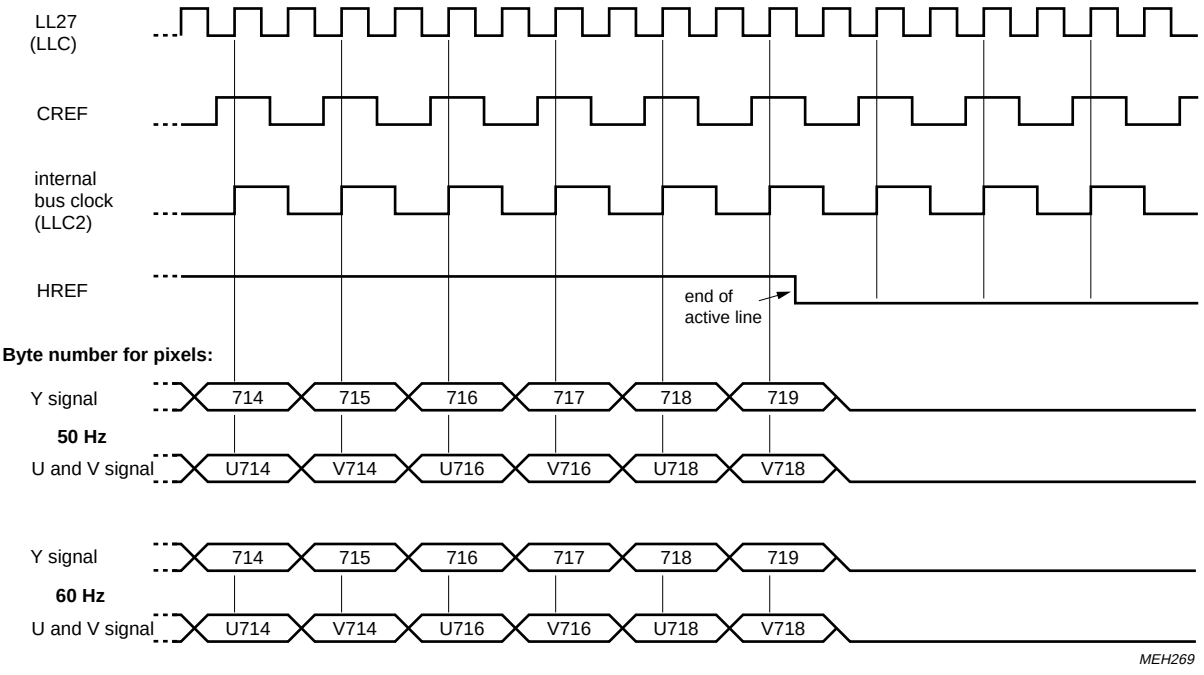
INPUT	PIXEL BYTE SEQUENCE (4 : 2 : 2 FORMAT)					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7 (MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Table 3 Data format 4 : 1 : 1

INPUT	PIXEL BYTE SEQUENCE (4 : 1 : 1 FORMAT)							
Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			



a. Start of active line.



b. End of active line.

Fig.3 Line control by HREF for 4 : 2 : 2 format, CREF = 13.5 MHz; HREF = 720 pixel; 50 and 60 Hz field.

Interpolation

The chrominance interpolation filter consists of various filter stages, multiplexers and de-multiplexers to increase the data rate of the colour-difference signals by a factor of 2 or 4. The switching of the filters by the bits IFF, IFC and IFL is described previously. Additional signal samples with significant amplitudes between two consecutive signal samples of the low data rate are generated.
The time-multiplexed U and V samples are stored in parallel for converting.

Data switch

The digital signals are adapted to the conversation range. U and V data have 8-bit formats again; Y can have 9 bits dependent on peaking. Blanking and switching to colourless level is applied here. Bits can be inverted by INV-bit to change the polarity of colour-difference output signals.

Digital Colour Transient Improvement (DCTI)

The DCTI circuit improves the transition behaviour of the UV colour-difference signals. As the CVBS signal allows for a 4 : 1 : 1 bandwidth representation only, the DCTI improves the transients to the same performance as signals coming from a 4 : 2 : 2 source, or even more.

In order to obtain the point of inflection, the second derivative of the signal is calculated. The improved transition is centred with respect to the point of inflection of the original signal. Thus, there is no horizontal shift of the resulting signal.

The transition area length to be improved is controlled via I^{2}C-bus by the bits LI1 and LI0 (Table 5); the sensitivity of the DCTI block is controlled by the bits GA1 and GA0. The CMO bit controls the colour detail sensitivity. It should be set to logic 1 (ON) if the video signal contains fine colour details (recommended operation mode).

Digital-to-Analog Converters (DACs)

Conversion is separate for Y, U and V. The converters use resistor chains with low-impedance output buffers.
The minimum output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V floating.
An application for 1 V/75 Ω on outputs is shown in Fig.14.

Each digital-to-analog converter has its own supply and ground pins suitable for decoupling. The reference voltage, supplying the resistor chain of all three DACs, is the supply voltage V_{DDA4}. The current into pin 41 is 0.3 mA; a larger current improves the bandwidth but increases the integral non-linearity.

I^{2}C-bus format

Table 4 I^{2}C-bus format; see notes 1 to 7

S	slave address	A	subaddress	A	data 0	A	...	data n	A	P

Notes

1. S = START condition.
2. Slave address = 1011 111X.
3. A = acknowledge; generated by the slave.
4. Subaddress = subaddress byte (Table 5);
   If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.
5. Data = data byte (Table 5).
6. P = STOP condition.
7. X = R/$\overline{W}$ control bit:
   a) X = 0; order to write (the circuit is slave receiver).
   b) X = 1; order to read (the circuit is slave transmitter).

Table 5 I^2C-bus transmission

SUBADDRESS	FUNCTION	DATA BITS							
		D7	D6	D5	D4	D3	D2	D1	D0
01	peaking and coring	AFB	CO1	CO0	BP1	BP0	BFB	WG1	WG0
02	input formats; interpolation	IFF	IFC	IFL	CMO	LI1	LI0	GA1	GA0
03	input/output setting	0	0	DC1	DC0	DRP	BLV	R78	INV

Table 6 Bit functions in data bytes

BIT	DESCRIPTION
CO1 and CO0	control of coring threshold; see Table 7
AFB, BP1, BP0, BFB	bandpass filter selection; see Table 8
BFB, WG1 and WG0	peaking factor K; see Table 9
IFF, IFC and IFL	input format and filter control at 13.5 MHz data rate; see Table 10
CMO	choice modification; 0 = modification off; 1 = modification on.
LI1 and LI0	DCTI timing range; see Table 11
GA1 and GA0	DCTI gain factor; see Table 12
DC1 and DC0	delay compensation of luminance signal; see Table 13
DRP	UV input data code; 0 = two's complement; 1 = offset binary
BLV	blanking level on Y output; 0 = 16 LSB; 1 = 0 LSB
R78	YUV input data solution; 0 = 7-bit data; 1 = 8-bit data
INV	polarity of colour-difference output signals: 0 = normal polarity equal to input signal 1 = inverted polarity

Table 7 Logic levels and function of CO1 and CO0

DATA BITS		FUNCTION
CO1	CO0	
0	0	coring off
0	1	small noise reduction
1	0	medium noise reduction
1	1	high noise reduction

Table 8 Logic levels and function of AFB, BP1, BP0 and BFB

DATA BITS				FUNCTION
AFB	BP1	BP0	BFB	
X	0	0	0	characteristic (see Fig.5)
X	0	1	0	characteristic (see Fig.6)
X	1	0	0	characteristic (see Fig.7)
X	1	1	0	characteristic (see Fig.8)
0	X	X	1	BF1 filter bypassed (see Fig.9a)
1	X	X	1	BF1 filter bypassed (see Fig.9b)

Table 9 Logic levels and function of BFB, WG1 and WG0

DATA BITS			FUNCTION
BFB	WG1	WG0	
0	0	0	K = 1/8; minimum peaking
0	0	1	K = 1/4
0	1	0	K = 1/2
0	1	1	K = 1; maximum peaking
1	0	0	K = 0; peaking off
1	0	1	K = 1/4; minimum peaking
1	1	0	K = 1/2
1	1	1	K = 1; maximum peaking

Table 10 Logic levels and function of IFF, IFC and IFL

DATA BITS			FUNCTION
IFF	IFC	IFL	
0	0	0	4 : 1 : 1 format; –3 dB attenuation at 1.6 MHz video frequency; (see Fig.10)
0	0	1	4 : 1 : 1 format; –3 dB attenuation at 600 kHz video frequency; (see Fig.11)
0	1	X	4 : 1 : 1 format; –3 dB attenuation at 1.2 MHz video frequency; (see Fig.12)
1	0	0	4 : 2 : 2 format; –3 dB attenuation at 1.6 MHz video frequency; (see Fig.10)
1	0	1	4 : 2 : 2 format; –3 dB attenuation at 600 kHz video frequency; (see Fig.11)
1	1	X	4 : 2 : 2 format; –3 dB attenuation at 2.5 MHz video frequency; (see Fig.13)

Table 11 Logic levels and function of LI1 and LI0

DATA BITS		RANGE
LI1	LI0	
0	0	+4 to –4
0	1	+6 to –6
1	0	+8 to –8
1	1	+12 to –12

Table 12 Logic levels and function of GA1 and GA0

DATA BITS		FACTOR
GA1	GA0	
0	0	off
0	1	1/4
1	0	1/2
1	1	1

Table 13 Logic levels and function of DC1 and DC0

DATA BITS		DELAYED CLOCK CYCLES
DC1	DC0	
0	0	0
0	1	+1
1	0	–2
1	1	–1

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD1}	digital supply voltage 1 (pin 12)	–0.3	+7	V
V_{DDD2}	digital supply voltage 2 (pin 31)	–0.3	+7	V
V_{DDA1}	analog supply voltage 1 (pin 32)	–0.3	+7	V
V_{DDA2}	analog supply voltage 2 (pin 37)	–0.3	+7	V
V_{DDA3}	analog supply voltage 3 (pin 40)	–0.3	+7	V
V_{DDA4}	analog supply voltage 4 (pin 42)	–0.3	+7	V
V_{DDD}	digital supply voltage	–0.5	+7	V
ΔV_{GND}	difference voltage $V_{SSD} - V_{SSA}$	–	±100	mV
V_I	voltage on all input pins 4 to 11, 14 to 27 and 41	–0.3	V_{DDD}	V
V_O	voltage on analog output pins 33, 36 and 39	–0.3	V_{DDD}	V
V_{ESD}	electrostatic handling for all pins	±2000	–	V
P_{tot}	total power dissipation	0	tbf	mW
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	0	70	°C

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	46	K/W

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; LLC = LL27; MC = CREF = 13.5 MHz; T_{amb} = 0 to 70 °C; measurements taken in Fig.14; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD1}	supply voltage range (pin 12)	for digital part	4.5	5	5.5	V
V_{DDD2}	supply voltage range (pin 31)	for digital part	4.5	5	5.5	V
V_{DDA1}	supply voltage range (pin 32)	for buffer of DAC 1	4.75	5	5.25	V
V_{DDA2}	supply voltage range (pin 37)	for buffer of DAC 2	4.75	5	5.25	V
V_{DDA3}	supply voltage range (pin 40)	for buffer of DAC 3	4.75	5	5.25	V
V_{DDA4}	supply voltage range (pin 42)	DAC reference voltage	4.75	5	5.25	V
I_{DDD}	supply current (I_{DDD1} + I_{DDD2})	for digital part	–	tbf	tbf	mA
I_{DDA}	supply current (I_{DDA1} + I_{DDA4})	for DACs and buffers	–	tbf	tbf	mA
YUV-bus inputs (pins 4 to 11 and 14 to 21) (see Figs 3 and 4)						
V_{IL}	LOW-level input voltage		–0.5	–	+0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DDD} + 0.5	V
C_I	input capacitance	V_I = HIGH	–	–	10	pF
I_{LI}	input leakage current		–	–	4.5	µA
Inputs AP, SP, MC, LLC, HREF and $\overline{\text{RESET}}$ (pins 22 to 27)						
V_{IL}	LOW-level input voltage		–0.5	–	+0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DDD} + 0.5	V
C_I	input capacitance	V_I = HIGH	–	–	10	pF
I_{LI}	input leakage current		–	–	4.5	µA
V_{24}	MC input voltage for LL27	27 MHz data rate	2.0	–	V_{DDD} + 0.5	V
	CREF signal on MC input	CREF data rate; note 1	–	–	–	V
I²C-bus SCL and SDA (pins 28 and 29)						
V_{IL}	LOW-level input voltage		–0.5	–	+1.5	V
V_{IH}	HIGH-level input voltage		3.0	–	V_{DDD} + 0.5	V
I_I	input current	V_I = LOW or HIGH	–	–	±10	µA
V_{ACK}	output voltage at acknowledge (pin 29)	I_{29} = 3 mA	–	–	0.4	V
I_{29}	output current	during acknowledge	3	–	–	mA
Digital-to-analog converters (pins 1, 2, 41, 42, 43 and 44)						
V_{DAC}	input reference voltage for internal resistor chains (pin 42)		4.75	5	5.25	V
I_{CUR}	input current (pin 41)	$R_{41\text{-}42}$ = 15 kΩ	–	300	–	µA
$V_{1,44}$	reference voltage LOW	pin connected to V_{SSA1}	–	0	–	V
C_L	external blocking capacitor to V_{SSA1} for reference voltage HIGH (pins 2 and 43)		–	0.1	–	µF
f_{LLC}	data conversation rate (clock)	Fig.3	–	–	36	MHz

RES_{DAC}	resolution	luminance DAC	–	9	–	bits
		chrominance DACs	–	8	–	bits
ILE	DC integral linearity error	8-bit data	–	–	1.0	LSB
DLE	DC differential error	8-bit data	–	–	0.5	LSB
Y, (R – Y) and (B – Y) analog outputs (pins 33, 36 and 39)						
$V_{o(p-p)}$	output signal voltage (peak to peak value)	without load	–	2	–	V
$V_{33,36,39}$	output voltage range	without load; note 2	0.2	–	2.2	V
V_{39}	output blanking level	Y output; note 3	–	16	–	LSB
$V_{33,36}$	output no-colour level	±(R – Y), ±(B – Y); note 4	–	128	–	LSB
$R_{33,36,39}$	internal serial output resistance		–	25	–	Ω
$R_{L33,36,39}$	output load resistance	external load	125	–	–	Ω
B	output signal bandwidth	–3 dB	20	–	–	MHz
t_d	signal delay from input to Y output		–	tbf	–	ns
LCC timing (pin 25) (see Fig.3)						
T_{LLC}	cycle time		27.7	37	41	ns
$t_{p\,H}$	pulse width		40	50	60	%
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	6	ns
YUV-bus timing (pins 4 to 11 and 14 to 21) (see Fig.5)						
$t_{SU;DAT}$	input data set-up time		10	–	–	ns
$t_{HD;DAT}$	input data hold time		3	–	–	ns
MC timing (pin 24) (see Fig.5)						
$t_{SU;DAT}$	input data set-up time		10	–	–	ns
$t_{HD;DAT}$	input data hold time		3	–	–	ns
$\overline{\text{RESET}}$ timing (pin 27)						
t_{SU}	set-up time after power-on or failure	active LOW; note 5	$4 \times t_{LLC}$	–	–	ns

Notes

1. YUV-bus data is read at MC = HIGH (pin 24) clocked with LLC (see Fig.5); data is read only with every second rising edge of LLC when CREF = ½LLC on pin 24.
2. 0.2 to 2.2 V output voltage range at 8-bit DAC input data; the data word can increase to 9-bit dependent on peaking factor.
3. The luminance signal is set to the digital black level: 16 LSB for BLV-bit = 0; 0 LSB for BLV-bit = 1.
4. The chrominance amplitudes are set to the digital colourless level of 128 LSB.
5. The circuit is prepared for a new data initialization.

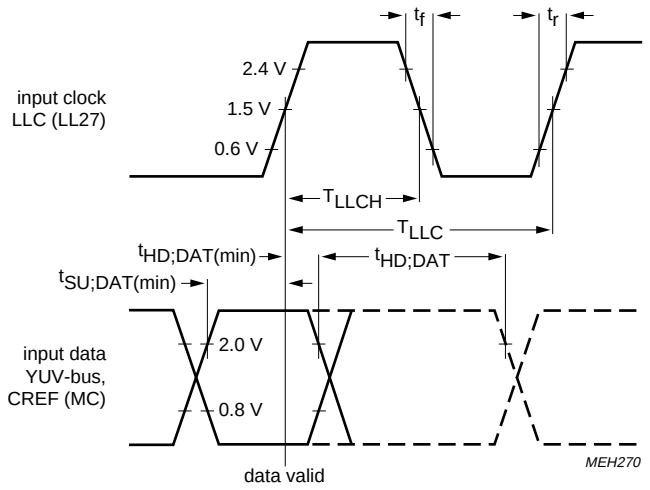
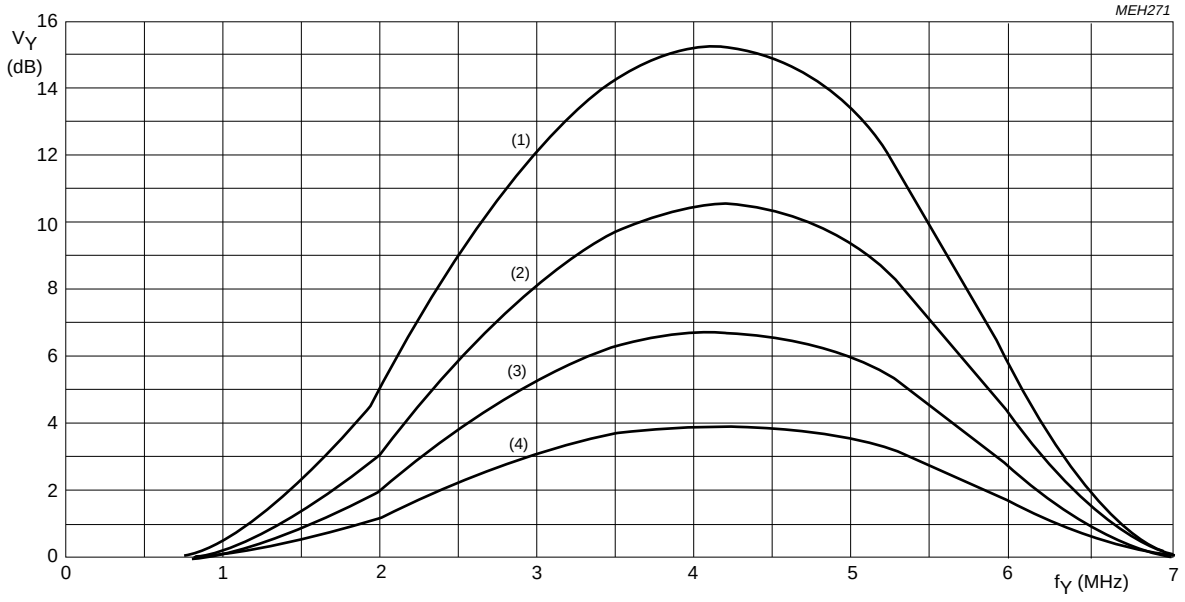


Fig.4 YUV-bus data and CREF timing.

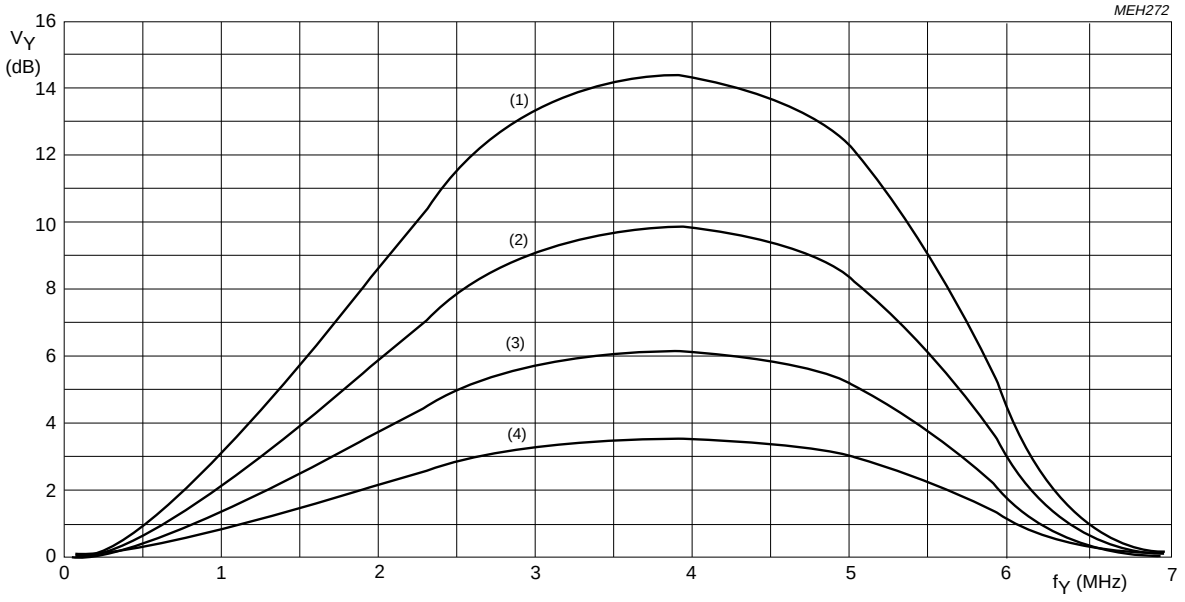
Table 14 YUV-bus data processing delay

PROCESSING DELAY	LLC CYCLES	REMARKS
YUV digital input	66	at MC = 1
YUV analog output	132	at MC = ½LLC



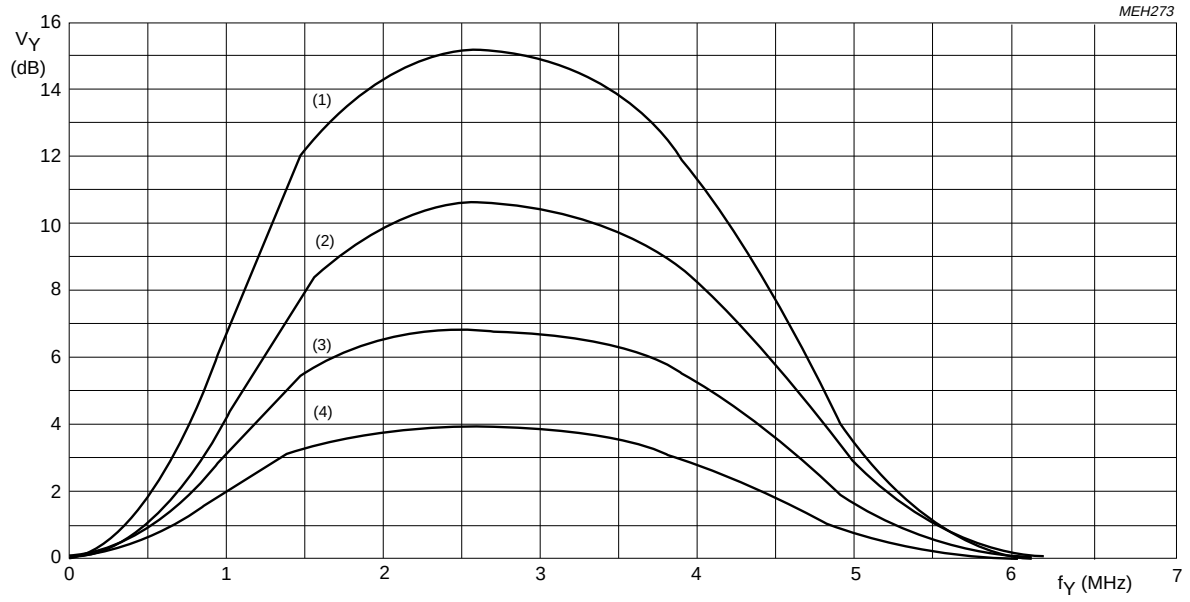
(1) K = 1
(2) K = ½
(3) K = ¼
(4) K = ⅛

Fig.5 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 0 and BFB = 0.



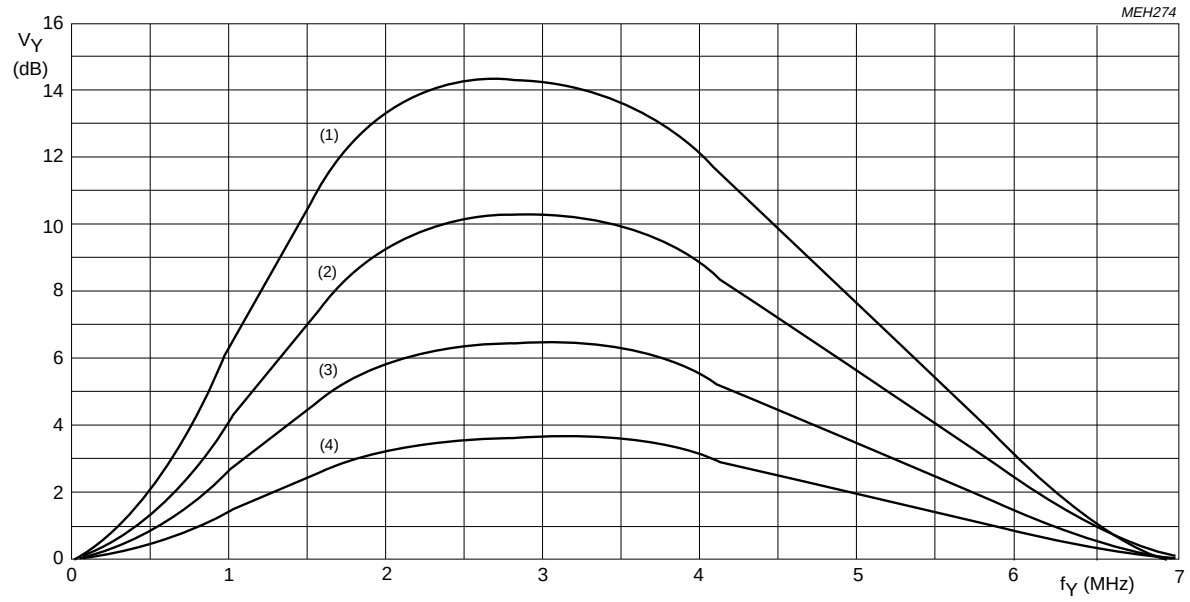
(1) K = 1
(2) K = ½
(3) K = ¼
(4) K = ⅛

Fig.6 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 1 and BFB = 0.



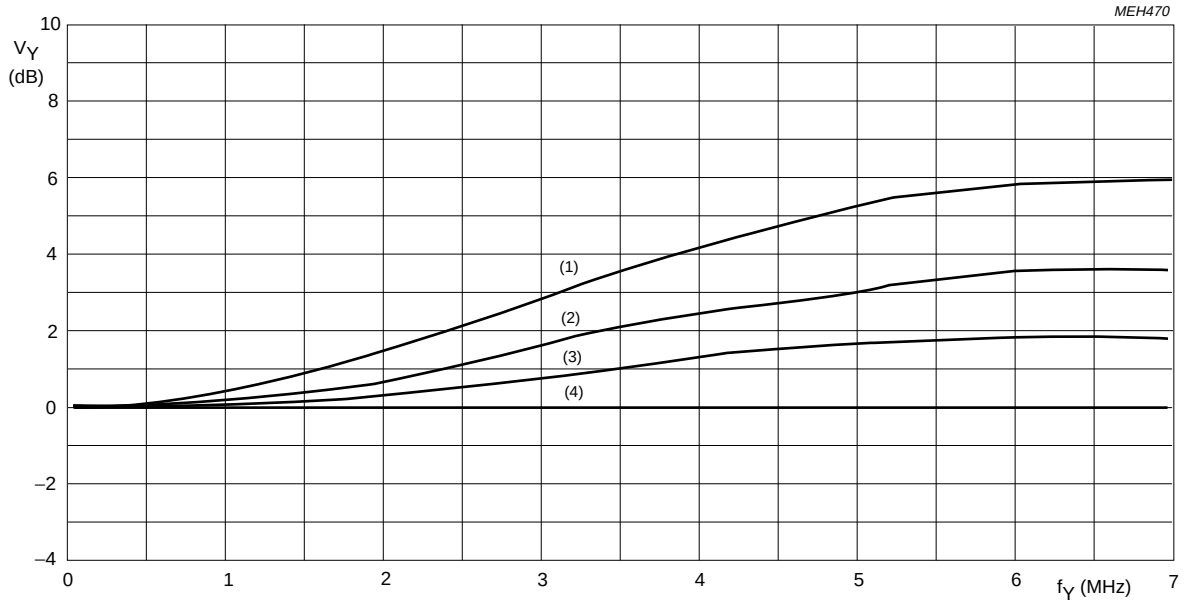
(1) K = 1
(2) K = ½
(3) K = ¼
(4) K = ⅛

Fig.7 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 0 and BFB = 0.

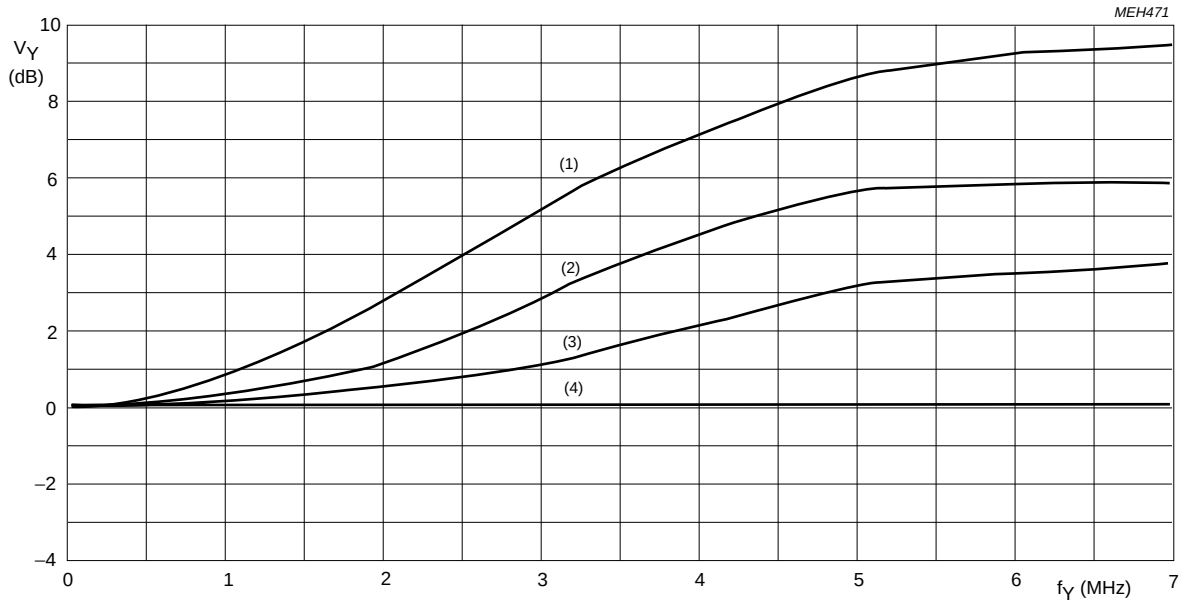


(1) K = 1
(2) K = ½
(3) K = ¼
(4) K = ⅛

Fig.8 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 1 and BFB = 0.



a. AFB = 0.



b. AFB = 1.

(1) K = 1
(2) K = ½
(3) K = ¼
(4) K = 0

Fig.9 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 0 and BFB = 1; bandpass filter BF1 bypassed and peaking off.

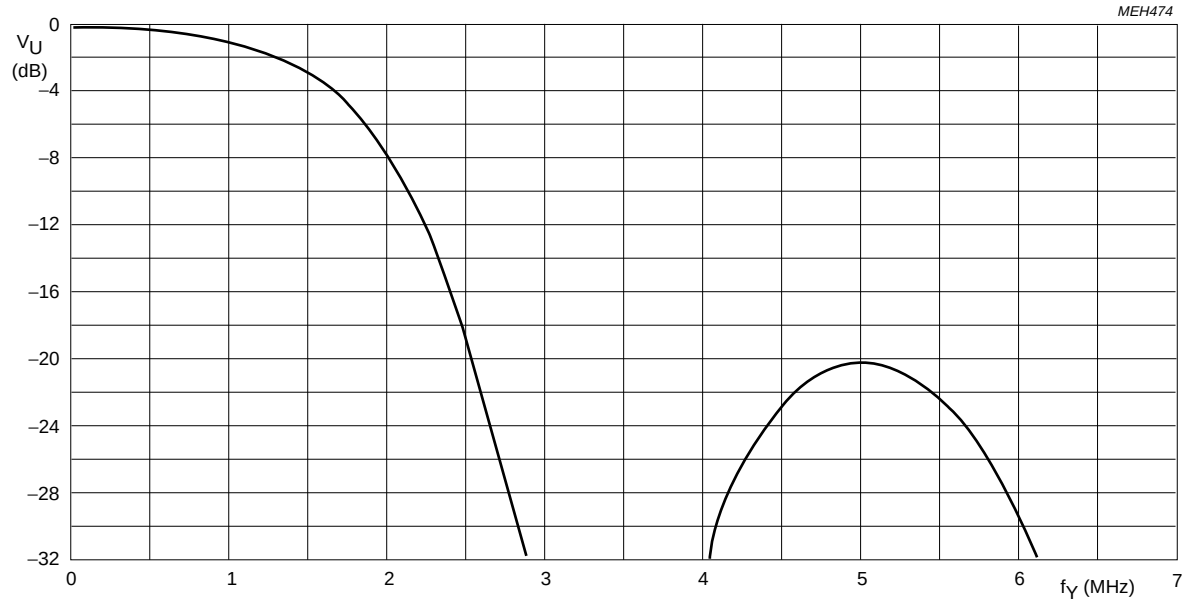


Fig.10 Interpolation filter at DCTI off with I²C-bus control bits IFF = 0; IFC = 0 and IFL = 0 in 4 : 1 : 1 format and control bits IFF = 1; IFC = 0 and IFL = 0 in 4 : 2 : 2 format; 13.5 MHz data rate.

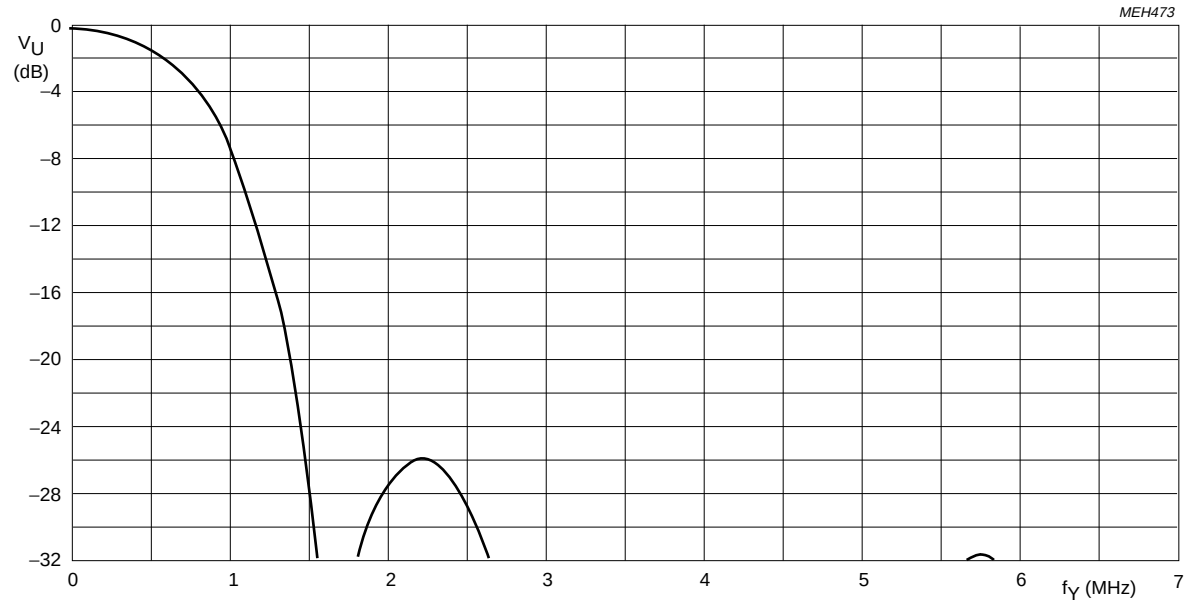


Fig.11 Interpolation filter at DCTI off with I²C-bus control bits IFF = 0; IFC = 0 and IFL = 1 in 4 : 1 : 1 format and control bits IFF = 1; IFC = 0 and IFL = 1 in 4 : 2 : 2 format; 13.5 MHz data rate.

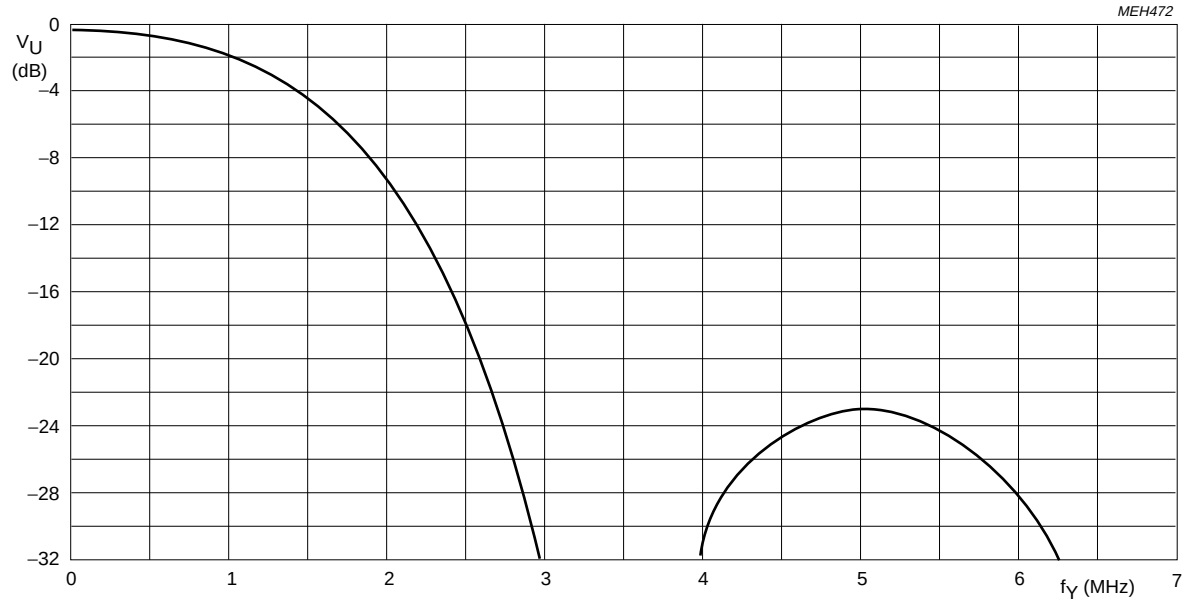


Fig.12 Interpolation filter at DCTI off with I²C-bus control bits IFF = 0; IFC = 1 and IFL = 0 in 4 : 1 : 1 format; 13.5 MHz data rate.

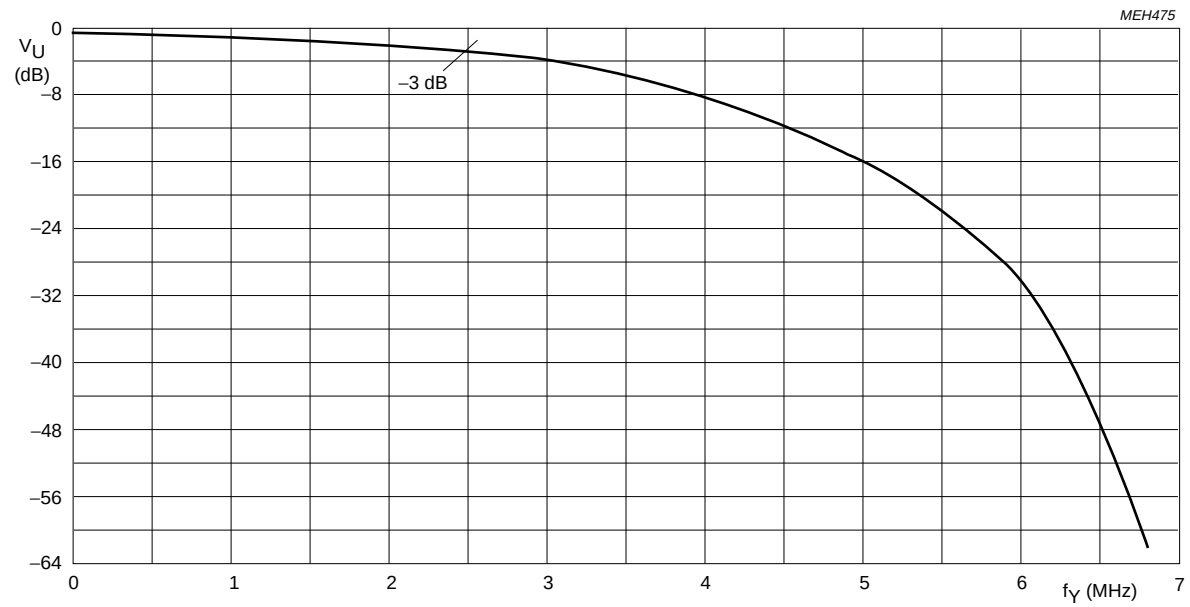


Fig.13 Interpolation filter with I²C-bus control bits IFF = 1; IFC = 1 and IFL = X in 4 : 2 : 2 format; 13.5 MHz data rate.

APPLICATION INFORMATION

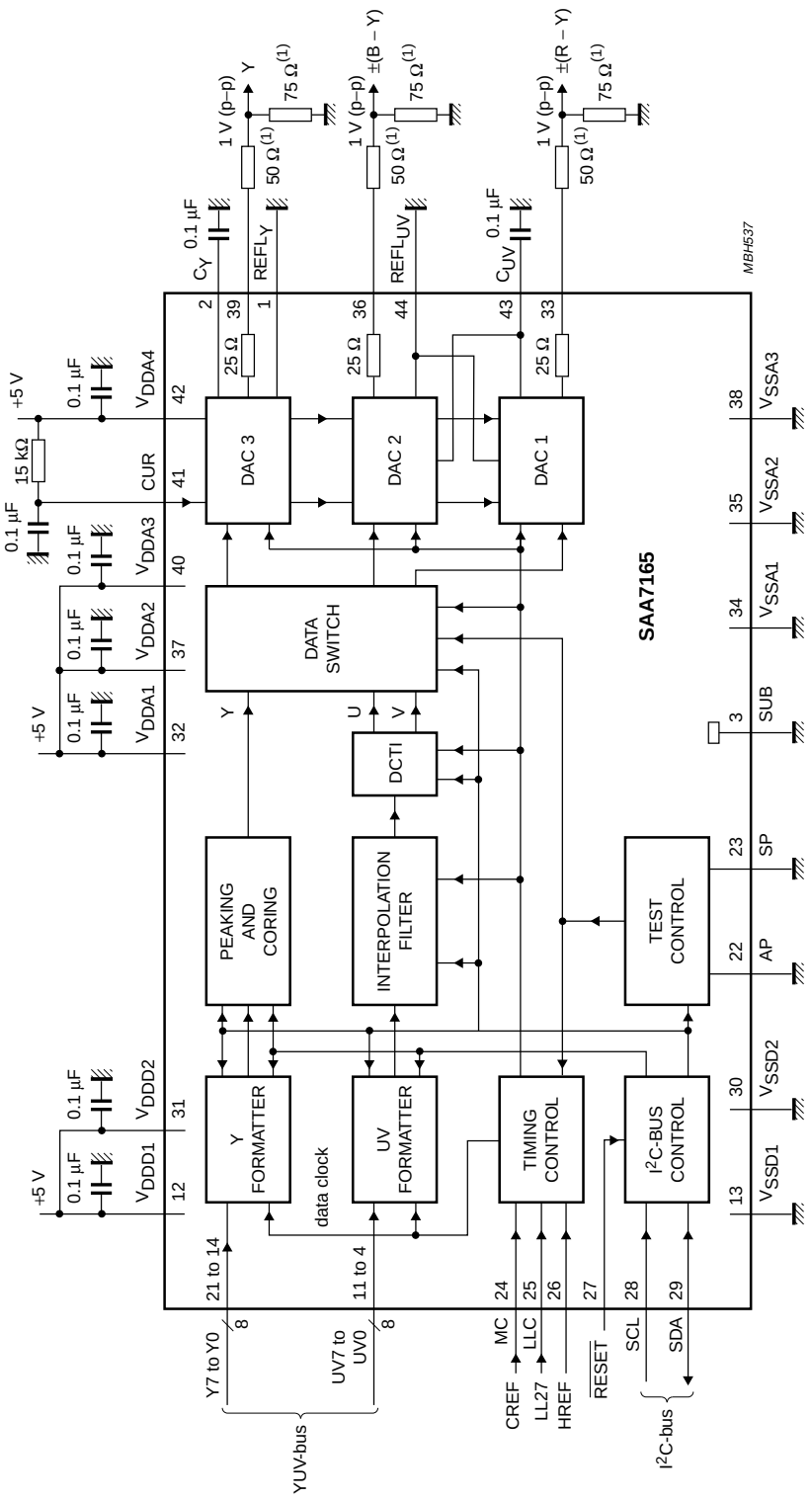
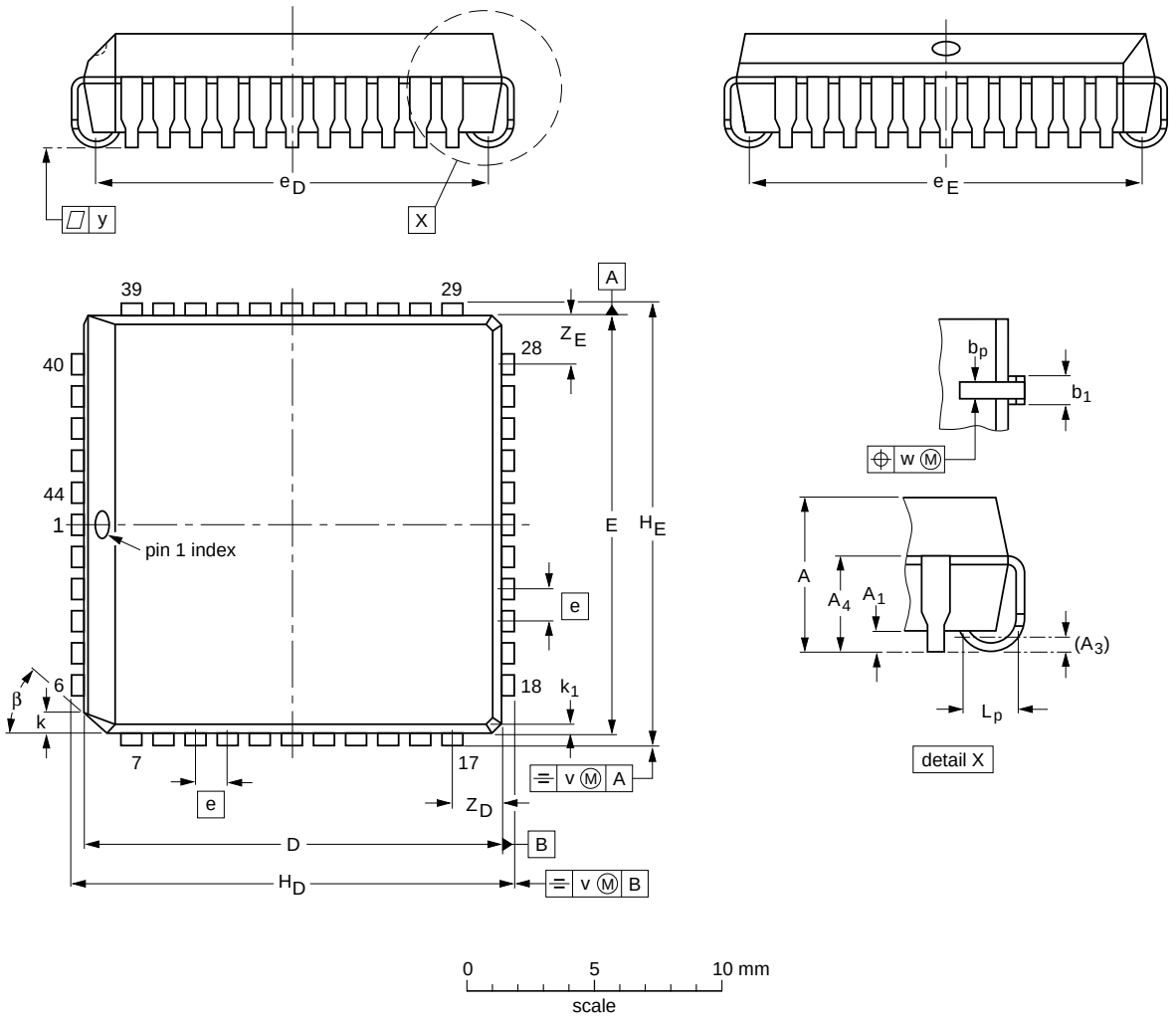


Fig.14 Application diagram.

(1) output amplitude determined by resistors (R_L > 125 Ω).

PACKAGE OUTLINE

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				~~92-11-17~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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