DATA SHEET

SAA7151B
Digital multistandard colour decoder with SCART interface (DMSD2-SCART)

Product specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

Digital multistandard colour decoder with SCART interface (DMSD2-SCART)

SAA7151B

FEATURES

- 8-bit performance on chip for luminance and chrominance signal processing for PAL, NTSC and SECAM standards
- Separate 8-bit luminance and 8-bit chrominance input signals from Y/C, CVBS, S-Video (S-VHS or Hi8) sources
- SCART signal insertion by means of RGB/YUV convertion; fast switch handling
- Horizontal and vertical sync detection for all standards
- Real time control output RTCO
- Fast sync recovery of vertical blanking for VCR signals (bottom flutter compensation)
- Controls via the I^2C-bus
- User programmable aperture correction (horizontal peaking)
- Cross-colour reduction by chrominance comb-filtering (NTSC) or by special cross-colour cancellation (SECAM)
- 8-bit quantization of output signals in 4:1:1 or 4:2:2 formats
- 720 active samples per line
- The YUV bus supports a data rate of 13.5 MHz (CCIR 601).
  - $(864 \times f_H)$ for 50 Hz
  - $(858 \times f_H)$ for 60 Hz
- Compatible with memory-based features (line-locked clock)
- One 24.576 MHz crystal oscillator for all standards

GENERAL DESCRIPTION

The SAA7151B is a digital multistandard colour-decoder having two 8-bit input channels, one for CVBS or Y, the other for chrominance or time-multiplexed colour-difference signals.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 18, 28, 37 and 52)	4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37 and 52)	–	100	250	mA
V_I	input levels	TTL-compatible			
V_O	output levels	TTL-compatible			
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7151B	68	mini-pack PLCC	plastic	SOT188(1)

Note

1. SOT188-2; 1996 December 16.

BLOCK DIAGRAM

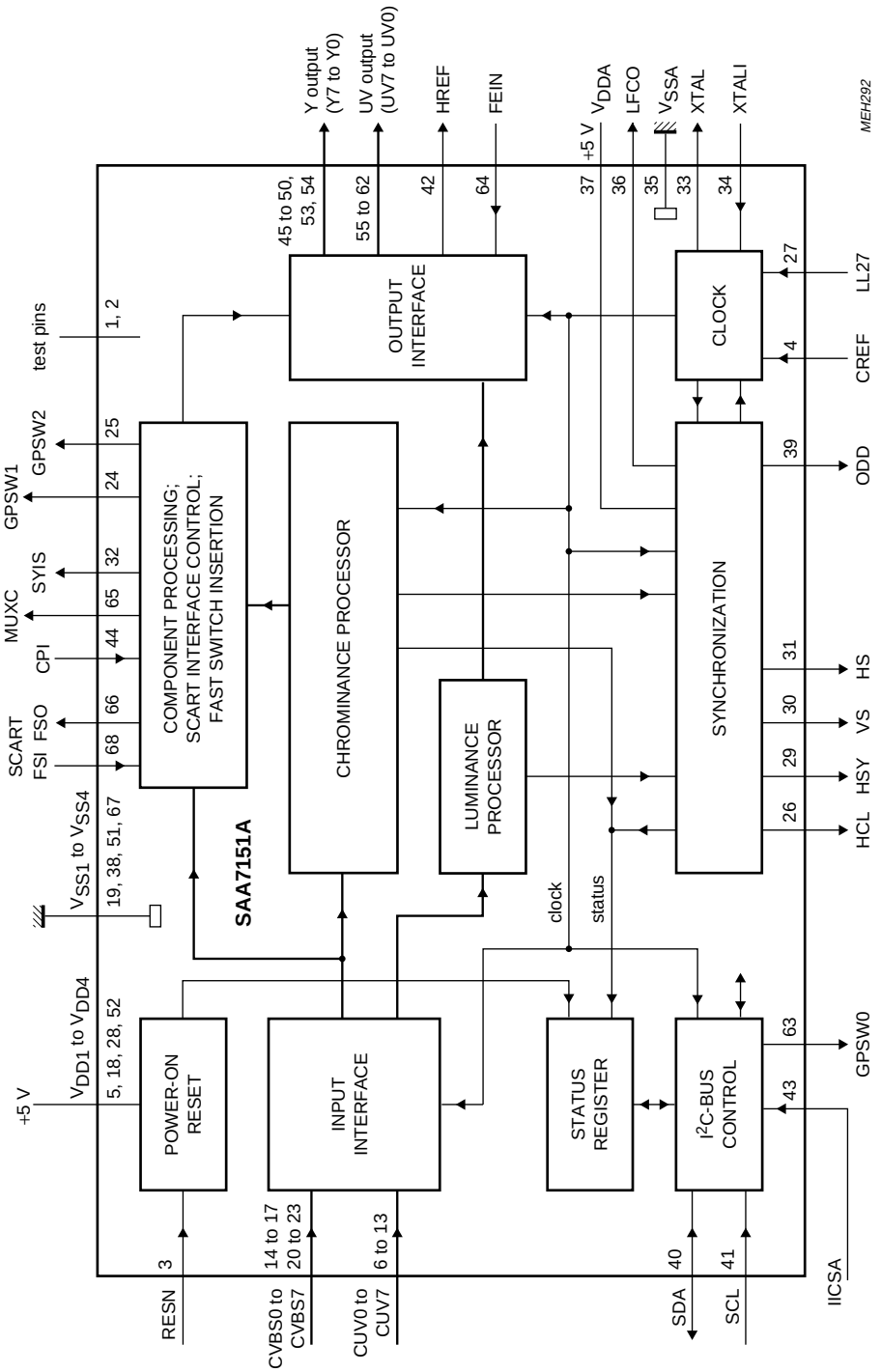


Fig.1 Block diagram (application circuits see Figs 17, 18 and 19).

PINNING

SYMBOL	PIN	DESCRIPTION
SP	1	connected to ground (shift pin for testing)
AP	2	connected to ground (action pin for testing)
RESN	3	reset, active-LOW
CREF	4	clock reference, sync from external to ensure in-phase signals on the Y-, CUV- and YUV-bus
V_{DD1}	5	+5 V supply input 1
CUV0	6	chrominance input data bits CUV7 to CUV0 (digitized chrominance signals in two's complement format from a S-Video source (S-VHS, Hi8) or time-multiplexed colour-difference signals from a YUV(RGB) source or both in combination)
CUV1	7	
CUV2	8	
CUV3	9	
CUV4	10	
CUV5	11	
CUV6	12	
CUV7	13	
CVBS0	14	CVBS lower input data bits CVBS3 to CVBS0 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS1	15	
CVBS2	16	
CVBS3	17	
V_{DD2}	18	+5 V supply input 2
V_{SS1}	19	ground 1 (0 V)
CVBS4	20	CVBS upper input data bits CVBS7 to CVBS4 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS5	21	
CVBS6	22	
CVBS7	23	
GPSW1	24	status bit output FSST0 or port 1 output for general purpose (programmable by subaddress 0C)
GPSW2	25	status bit output FSST1 or port 2 output for general purpose (programmable by subaddress 0C)
HCL	26	black level clamp pulse output (begin and stop programmable), e.g. for TDA8708A (ADC)
LL27	27	line-locked system clock input signal (27 MHz)
V_{DD3}	28	+5 V supply input 3
HSY	29	hor. sync pulse reference output (begin and stop programmable), e.g. for gain adj.TDA8708A (ADC)
VS	30	vertical sync output signal (Fig.11)
HS	31	horizontal sync output signal (Fig.16; start point programmable)
RTCO	32	real time control output; serial increments of HPLL and FSCPLL and status PAL or SECAM sequence (Fig.10)
XTAL	33	24.576 MHz clock output (open-circuit for use with external oscillator)
XTALI	34	24.576 MHz connection for crystal or external oscillator (TTL compatible squarewave)
V_{SSA}	35	analog ground
LFCO	36	line frequency control output signal, multiple of horizontal frequency (nominal 6.75 MHz)
V_{DDA}	37	+5 V supply input for analog part
V_{SS2}	38	ground 2 (0 V)

SYMBOL	PIN	DESCRIPTION
ODD	39	odd/even field identification output (odd = HIGH)
SDA	40	I^2C-bus data line
SCL	41	I^2C-bus clock line
HREF	42	horizontal reference for YUV data outputs (for active line 720Y samples long)
IICSA	43	set module address input of I^2C-bus (LOW = 1000 101X; HIGH = 1000 111X)
CPI	44	clamping pulse input (digital clamping of external UV signals)
Y7	45	Y signal output bits Y7 to Y2 (luminance), part of the digital YUV-bus
Y6	46	
Y5	47	
Y4	48	
Y3	49	
Y2	50	
V_{SS3}	51	ground 3 (0 V)
V_{DD4}	52	+5 V supply input 4
Y1	53	Y signal output bits Y1 to Y0 (luminance), part of the digital YUV-bus
Y0	54	
UV7	55	UV signal output bits UV7 to UV0, part of the digital YUV-bus
UV6	56	
UV5	57	
UV4	58	
UV3	59	
UV2	60	
UV1	61	
UV0	62	
GPSW0	63	port output for general purpose (programmable by subaddress 0D)
FEIN	64	fast enable input (active-LOW to control fast switching due to YUV data; HIGH = YUV high-Z
MUXC	65	multiplexer control output; source select signal for external ADC (UV signal multiplexing)
FSO	66	fast switch and sync insertion output; gated FS signal from FSI or sync insertion pulse in full screen RGB mode
V_{SS4}	67	ground 4 (0 V)
FSI	68	fast switch input signal fed from SCART/peri-TV connector (indicates fast insertion of RGB signals)

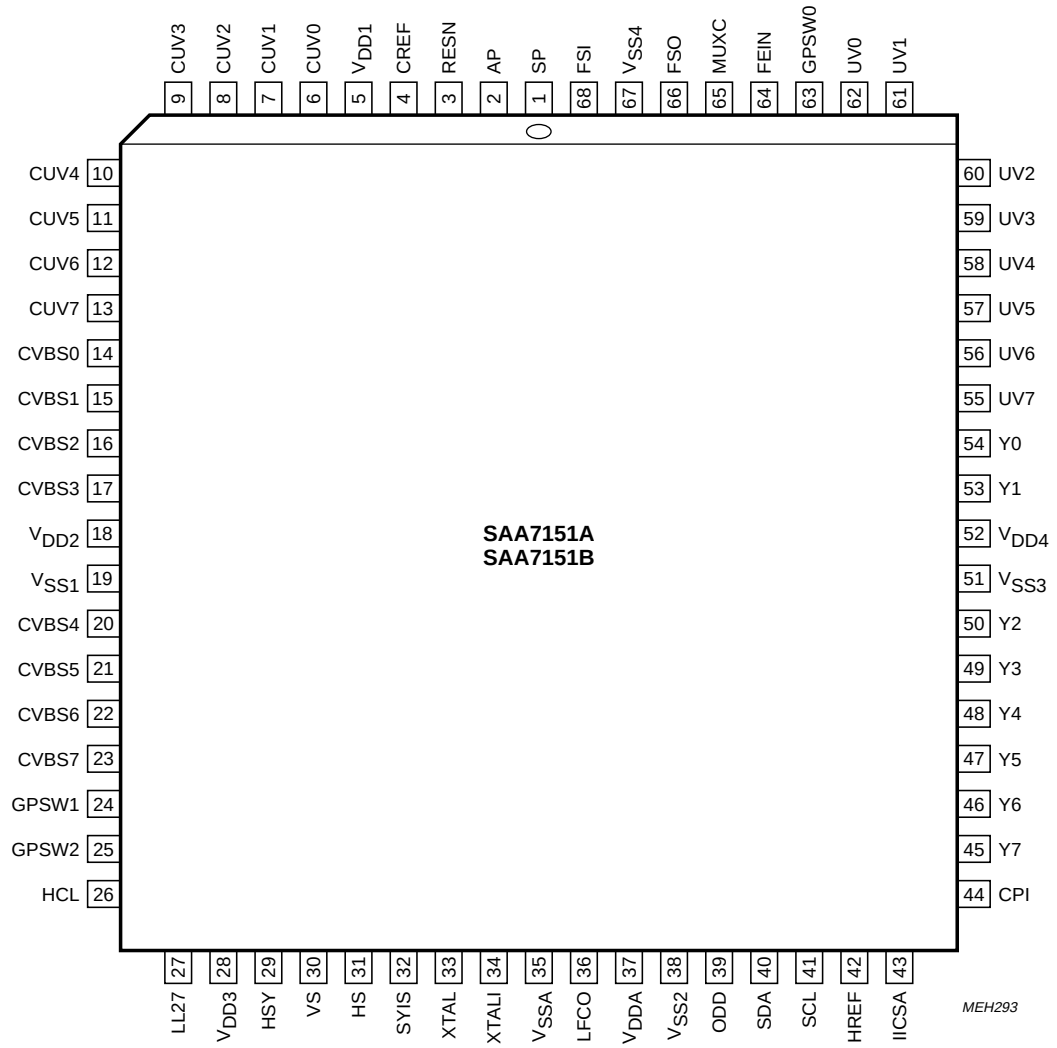


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

System configuration

The SAA7151B system processes digital TV signals with line-locked clock in PAL, SECAM and NTSC standards (CVBS or S-Video) as well as RGB signals coming from a SCART/peri-TV connector. The different source signals are switched, if necessary matrixed and converted (Fig.3 and Table 1).

8-bit CVBS data (digitized composite video) and 8-bit UV data (digitized chrominance and /or time-multiplexed colour-difference signals) are fed to the SAA7151B. The data rate is 27 MHz.

Chrominance processing

The 8-bit chrominance input signal (signal “C” out of CVBS or Y/C in Fig.4) is fed via the input interface to a bandpass filter for eliminating the DC component, then to the quadrature demodulator. Subcarrier signals from the local oscillator (DTO1) with 90 degree phase shift are applied to its multiplier inputs. The frequency depends on set TV standard.

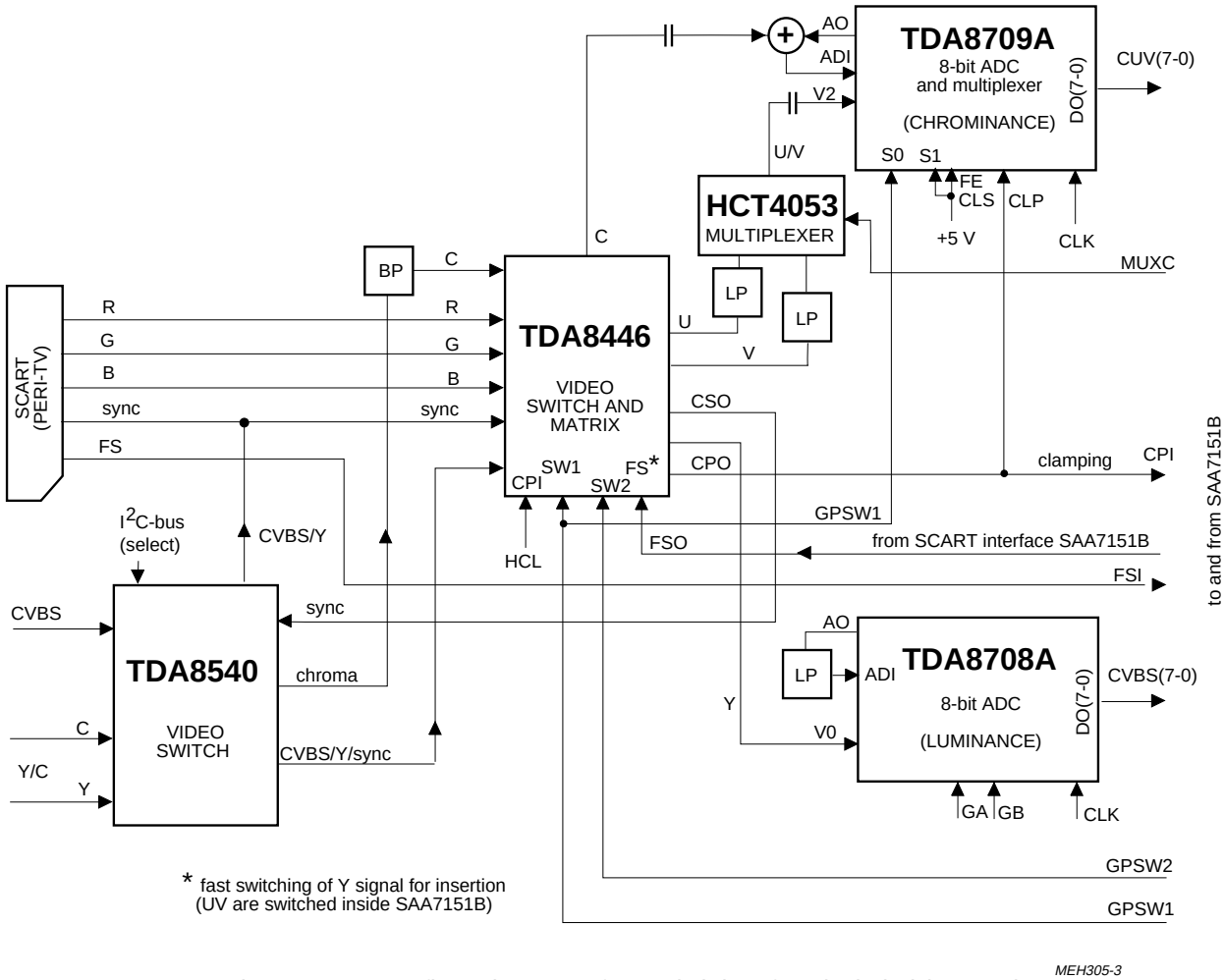


Fig.3 System configuration, RGB fast switch interface included (SCART).

The multipliers operate as a quadrature demodulator for all PAL and NTSC signals; it operates as a frequency down-mixer for SECAM signals.
The two multiplier output signals are converted to a serial UV data stream and applied to two low-pass filter stages, then to a gain controlled amplifier. A final multiplexed low-pass filter achieves, together with the preceding stages, the required bandwidth performance. The from PAL and NTSC originated signals are applied to a comb-filter. The signals, originated from SECAM, are fed through a cloche filter (0 Hz centre frequency), a phase demodulator and a differentiator to obtain frequency-demodulated colour-difference signals.

The SECAM signals are fed after de-emphasis to a cross-over switch, to provide the both serial-transmitted colour-difference signals. These signals are finally fed via the fast switch to the output formatter stages and to the output interface.
Chrominance signals are output in parallel (4:2:2) on the YUV-bus. The data rate of Y signal (pixel rate) is 13.5 MHz. UV signals have a data rate of 13.5 MHz/2 for the 4:2.2 format (Table 2) respectively 13.5 MHz/4 for the 4:1.1 format (Table 3).

Component processing and SCART interface control

The 8-bit multiplexed colour-difference input signal (signal CUV, Fig.1, out of matrixed RGB in Fig.3) is fed via the input interface to a chrominance stop filter (UV signal only can pass through; Figures 22 to 24). Here it is clamped and fed to the offset compensation which can be enabled or disabled via the I^{2}C-bus.

For matrixed RGB signals - the full screen SCART mode and the fast insertion mode (blanking/switching) are selectable. The chrominance stop filter is automatically bypassed in full screen SCART mode.

Full screen RGB mode (SCART):

The CUV digital input signal (7-0) consists of time-multiplexed samples for U and V. An offset correction for both signals is applied to correct external clamping errors. An internal timing correction compensates for slight differences in timing during sampling. The U and V signals are delay-compensated and fed to the output formatter. The format 4:2:2 or 4:1:1 is generated by a switchable filter.
The control signals for the front end (Figures 3 and 20) MUXC, status bits FSST1, FSST0 (outputs GPSW2, GPSW1) and FSO are generated by the SAA7151B.

Table 1 SCART interface control (Fig.3)

MODE	CONNECTION				chroma output of TDA8446 to TDA8709A	TDA8709A		luminance fast switch TDA8446	input selector (via I²C-bus) TDA8540
	FSO	GPSW 2	GPSW 1	MUXC		selected input	CUV (7-0)		
RGB only	0 0	0 0	0 0	0 1	high-Z	VIN2	U/V	sync (RGB)	sync (RGB)
Y/C or CVBS only	0 0	0 0	1 1	0 1	C	VIN1	C	Y (Y/C) or CVBS	Y (Y/C) or CVBS
Fast switch	0 0	1 1	0 0	0 1	C	VIN2	0.5(C+U)/ 0.5(C+V)	Y (Y/C) or CVBS	Y (Y/C) or CVBS
	0 0	1 1	1 1	0 1	not used				
RGB only	1 1	0 0	0 0	0 1	high-Z	VIN2	U/V	Y (RGB)	sync (RGB)
	1 1	0 0	1 1	0 1	not used				
Fast switch	1 1	1 1	0 0	0 1	C	VIN2	0.5(C+U)/ 0.5(C+V)	Y (RGB)	Y (Y/C) or CVBS
	1 1	1 1	1 1	0 1	not used				

Fast insertion mode:

Fast insertion is applied by FSI pulse to ensure correct timing. The RGB source signal is matrixed into UV and inserted into the CVBS or Y/C source signal after two field periods if FSI pulses are received. The output FSO is set to HIGH during a determined insertion window (screen plain minus 6 % of horizontal and vertical deflection). Switch over depends on the phase of FSI in relation to the valid pixel sequence depending on the phase-different weighting factors. They are applied to the original and the inserted UV data (Figures 6 and 7)
The control signals for the front end (Table 1) MUXC, FSO, status bits FSST1 and FSST0 (outputs GPSW2 and GPSW1) are generated by the SAA7151B.

The amplitude of chrominance and colour-difference signals are scaled down by factor 2 to avoid overloading of the chrominance analog-to-digital converter. The amplitudes are reduced in the TDA8446 by signals on lines GPSW2 and GPSW1.

Luminance processing

The luminance input signal, a digital CVBS format or an 8-bit luminance format (S-Video), is fed through a sample rate converter to reduce the data rate to 13.5 MHz (Fig.5).

Sample rate is converted by means of a switchable pre-filter. High frequency components are emphasized to compensate for loss in the following chrominance trap filter. This chrominance trap filter (f_o = 4.43 MHz or f_o = 3.58 MHz centre frequency selectable) eliminates the most of the colour carrier signal, therefore, it must be bypassed for S-Video signals.

The high frequency components of the luminance signal can be “peaked” in two bandpass filters with selectable transfer characteristic. A coring circuit (±1 LSB) can improve the signal, this signal is then added to the original signal. A switchable amplifier achieves a common DC amplification, because the DC gains are different in both chrominance trap modes. Additionally, a cut-off sync pulse is generated for the original signal in both modes.

Synchronization

The luminance output signal is fed to the synchronization stage. Its bandwidth is reduced to 1 MHz in a low-pass filter (sync pre-filter). The sync pulses are sliced and fed to the phase detectors to be compared with the sub-divided clock frequency. The resulting output signal is applied to the loop filter to accumulate all phase deviations. There are three groups of output timing signals:

a. signals related to data output signals (HREF)
b. signals related to the input signals (HSY, and HCL)
c. signals related to the internal sync phase

All horizontal timings are derived from the main counter, which represents the internal sync phase. The HREF signal only with its critical timing is phase-compensated in relationship to the data output signal. Future circuit improvements could slightly influence the processing delays of some internal stages to achieve a changed timing due to the timing groups b and c.
The HREF signal only controls the data multiplexer phase and the data output signals.
All timings of the following diagrams are measured with nominal input signals, for example coming from a pattern generator. Processing delay times are taken between input and data output, respectively between internal sync reference (main counter = 0) and the rising edge of HREF.

Line locked clock frequency

LFCO is required in an external PLL (SAA7157) to generate the line-locked clock frequency LL27 and CREF.

YUV-bus, digital outputs

The 16-bit YUV-bus transfers digital data from the output interfaces to a feature box, or to the digital-to-analog converter (DAC). Outputs are controlled via the I^2C-bus in normal selections, or they are controlled by output enable chain (FEIN, pin 64). The YUV-bus data rate 13.5 MHz. Timing is achieved by marking each second positive rising edge of the clock LL27 synchronized by CREF.

YUV-bus formats

4 : 2 : 2 and 4 : 1 : 1

The output signals Y7 to Y0 are the bits of the digital luminance signal. The output signals UV7 to UV0 are the bits of the digital colour-difference signal. The frames in the Tables 2 and 3 are the time to transfer a full set of samples. In case of 4 : 2 : 2 format two luminance samples are transmitted in comparison to one U and one V sample within one frame. The time frames are controlled by the HREF signal, which determines the correct UV data phase. The YUV data outputs can be enabled or set to 3-state position by means of the FEIN signal. FEIN = LOW enables the output; HIGH on this pin forces the Y and U/V outputs to a high-impedance state (Fig.6).

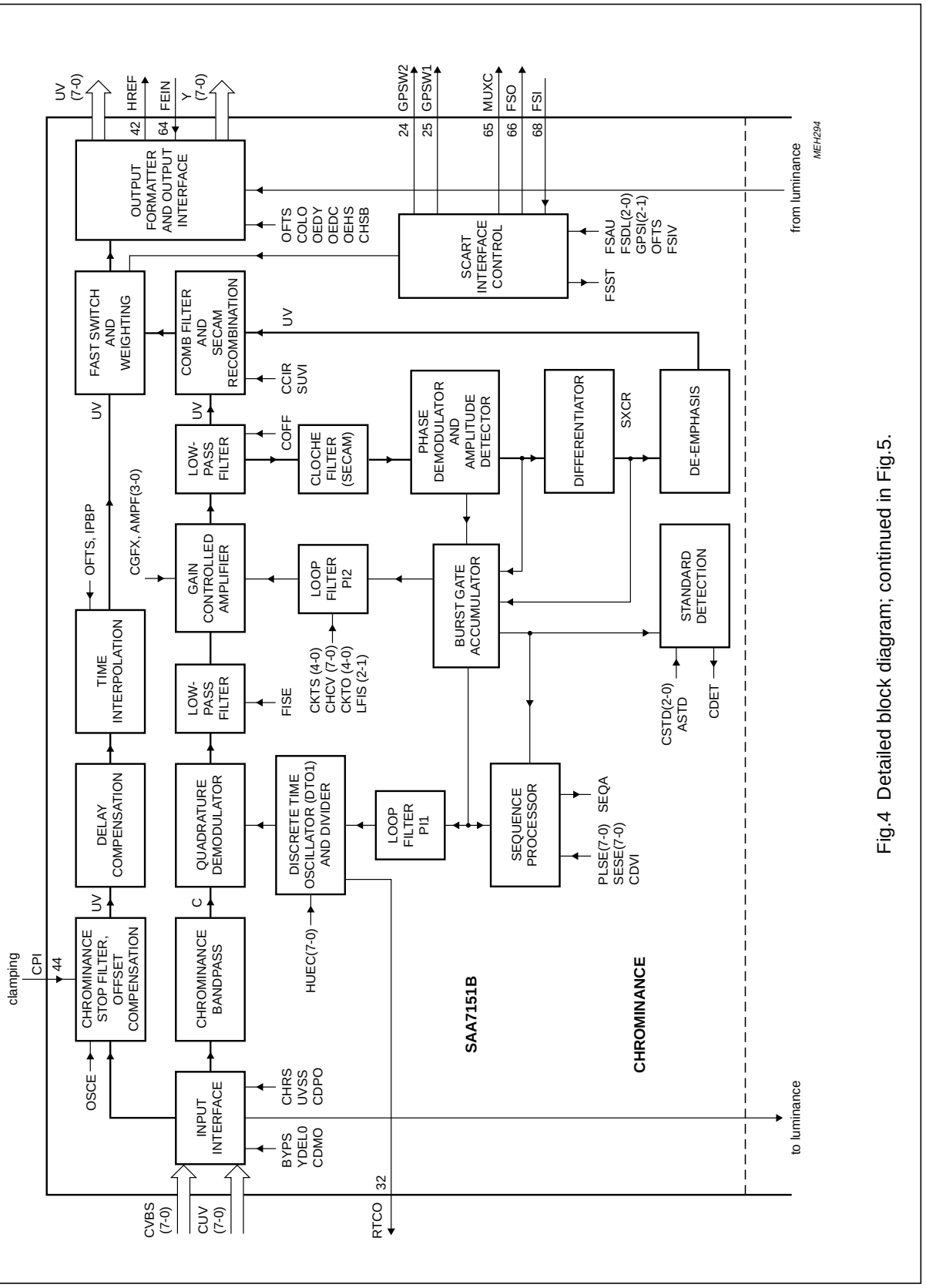


Fig.4 Detailed block diagram; continued in Fig.5.

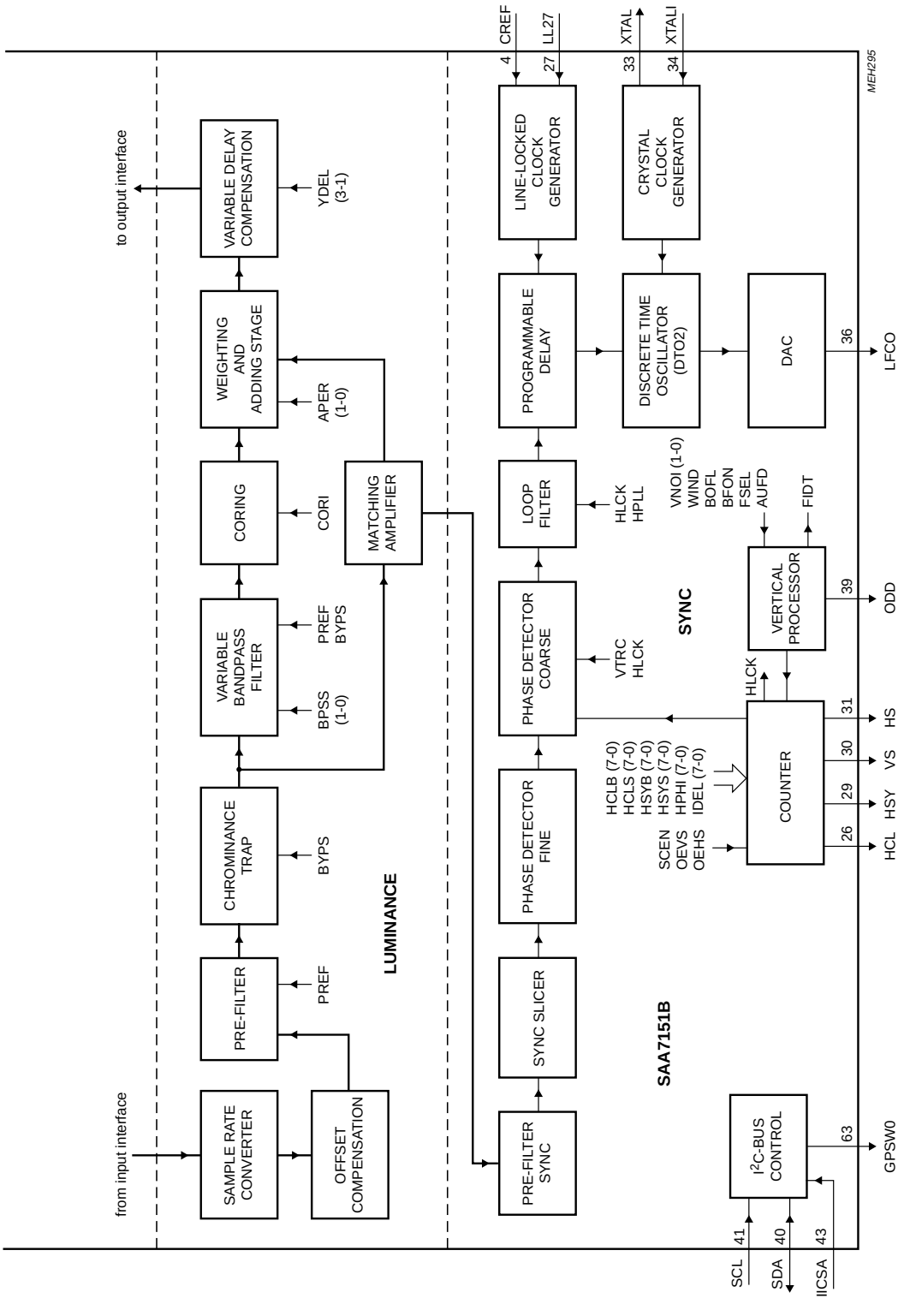


Fig.5 Detailed block diagram; continued from Fig.4.

Table 2 for the 4 : 2 : 2 format (720 pixels per line). The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

OUTPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7 (MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Table 3 for the 4 : 1 : 1 format (720 pixels per line). The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

OUTPUT	PIXEL BYTE SEQUENCE							
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7 (MSB)	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			

Signal levels (Figures 12, 13 and 14)

The nominal input and output signal levels are defined by a colour bar signal with 75 % colour, 100 % saturation and 100 % luminance amplitude (EBU colour bar).

CUV-bus input format

The CUV-bus transfers the digital chrominance/colour-difference signals from the ADC to the SAA7151B (Fig.6; Table 1):

- normal mode for digital chrominance transmission.
- UV colour-difference mode for colour-difference signals UV (out of matrixed RGB signals)
- FS mode (fast switch mode; UV inserted into chrominance signal C with addition of the two signal spectra).

RTCO output

The RTCO output signal (Fig.10) contains serialized information about actual clock frequency, subcarrier frequency and PAL/SECAM sequence. This signal may preferably be used with the frequency-locked digital video encoder SAA7199B.

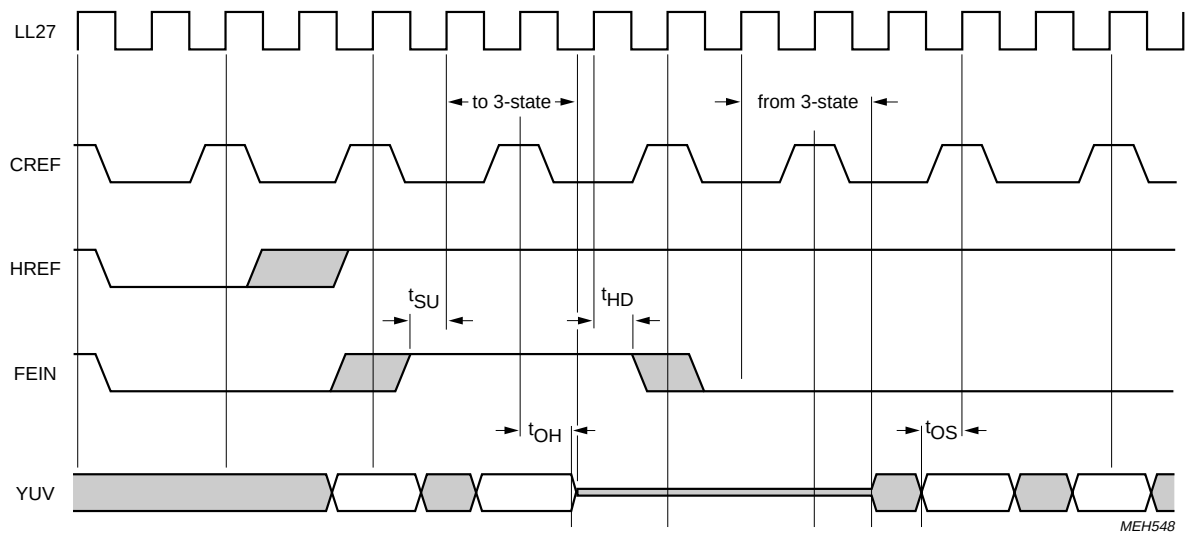


Fig.6 Timing example of fast enable input (FEIN).

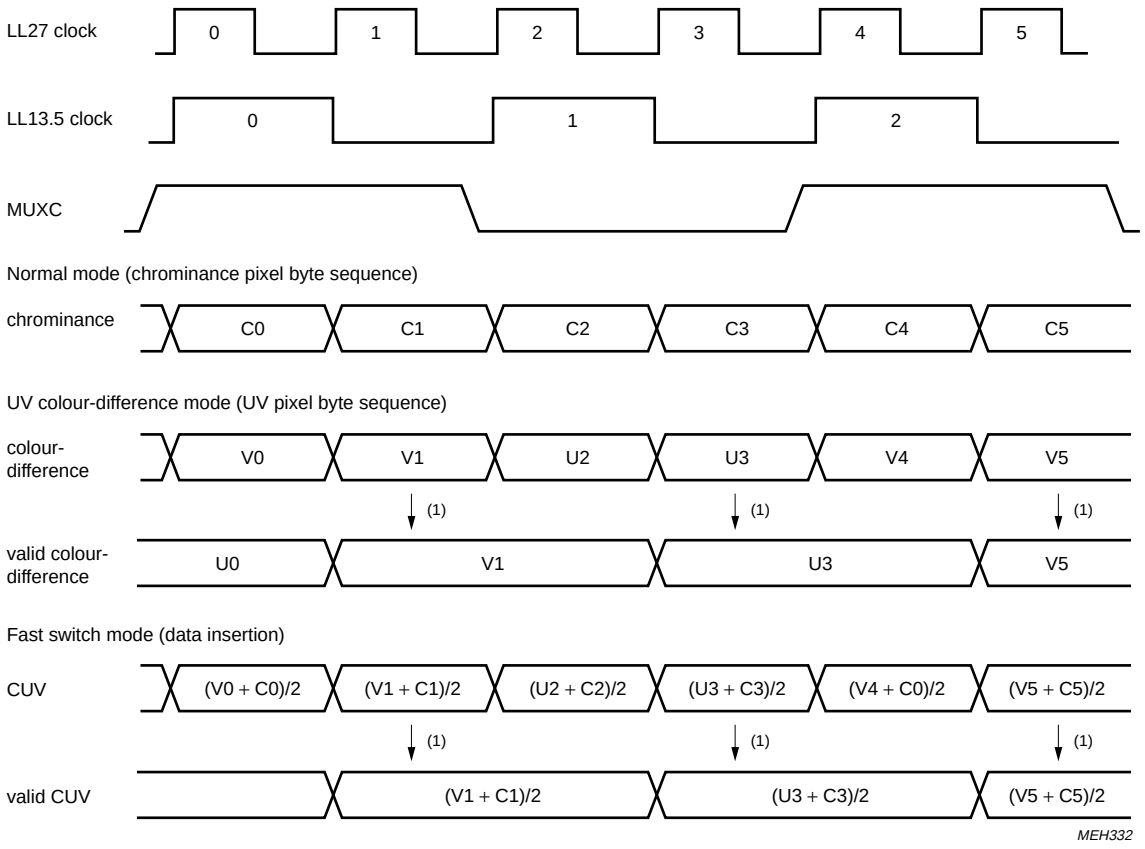


Fig.7 CUV input formats.
(1) each second sample only after a MUXC change is taken for down-sampling to 13.5 MHz to reduce cross-talk components between U and V signals.

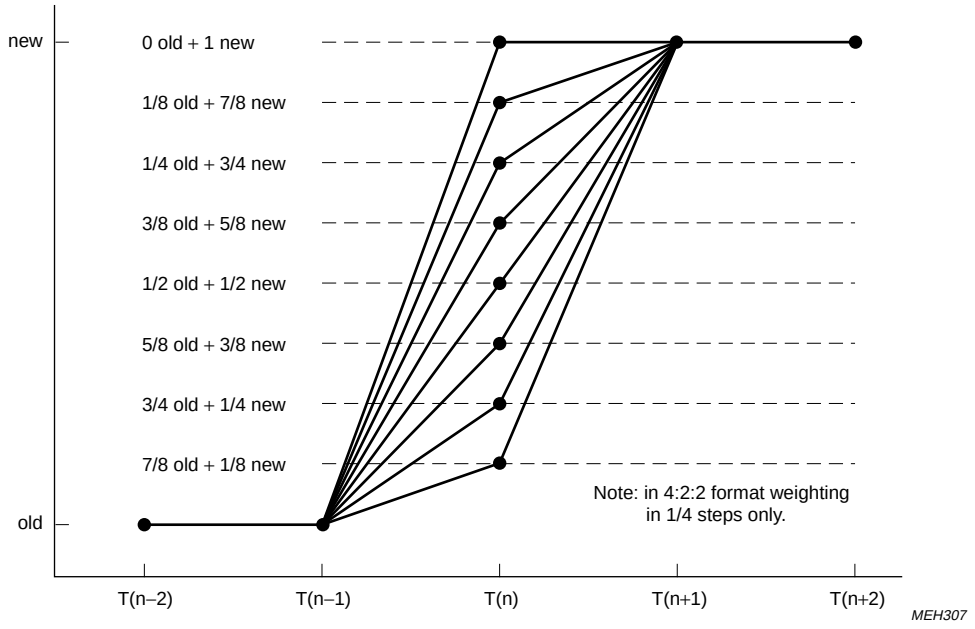


Fig.8 Addition of weighted components.

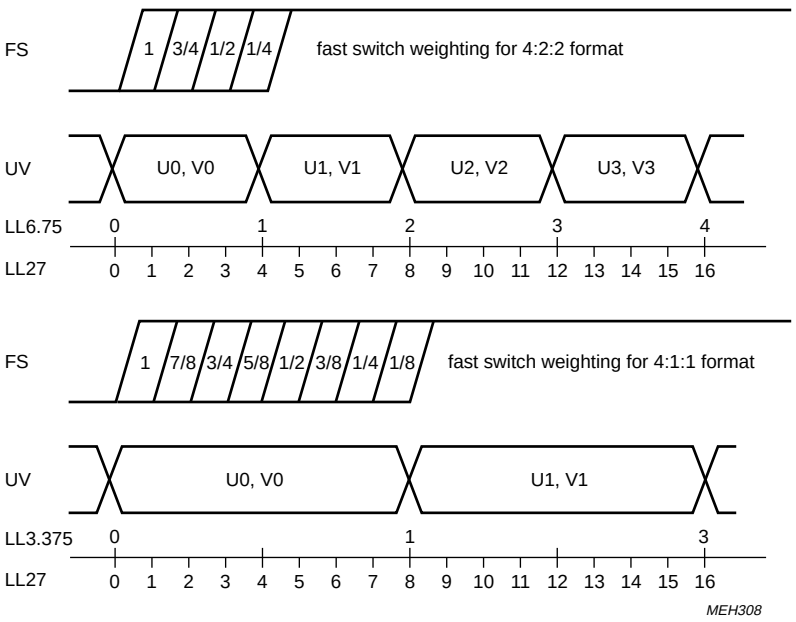


Fig.9 Weighting factors of fast switching for 4:2:2 and 4:1:1 formats.

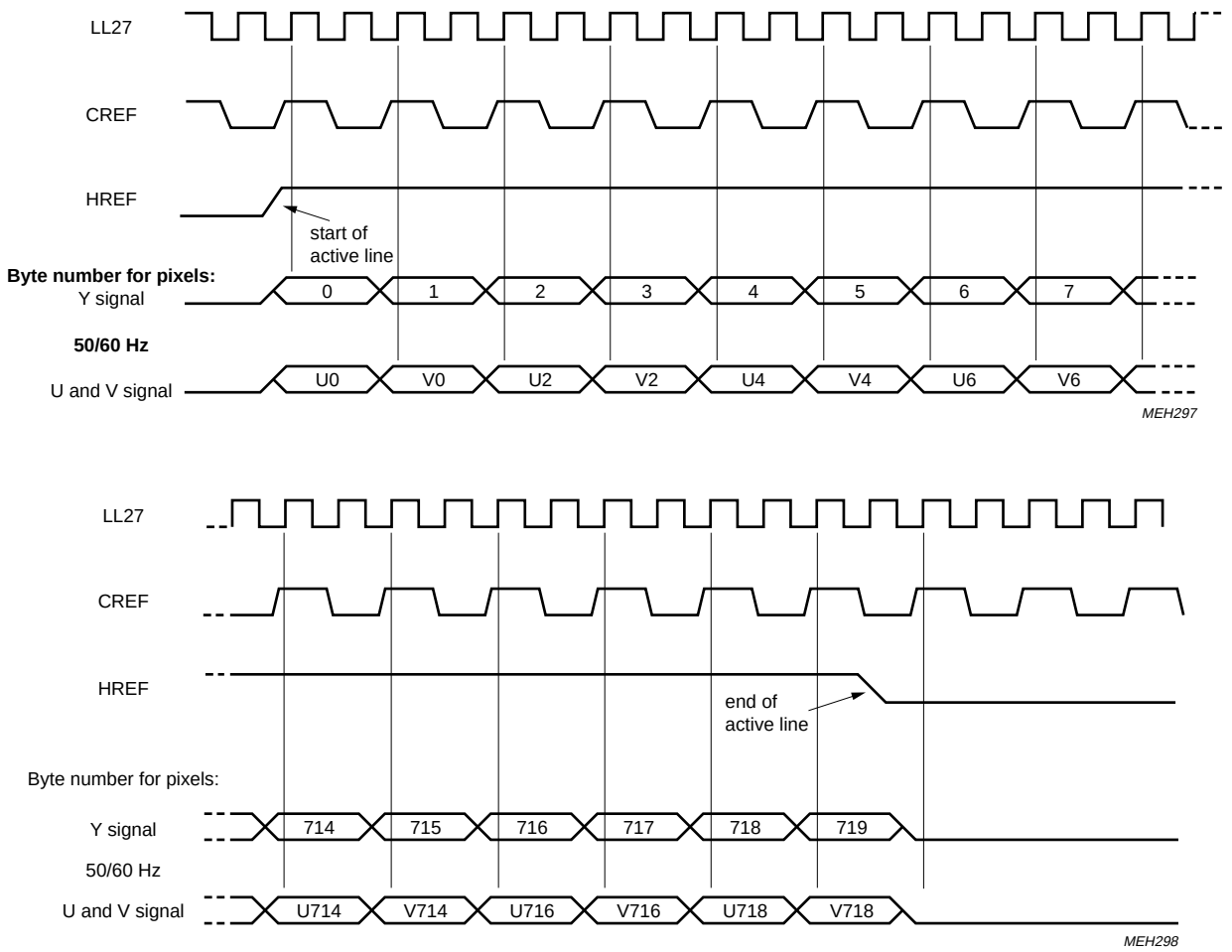
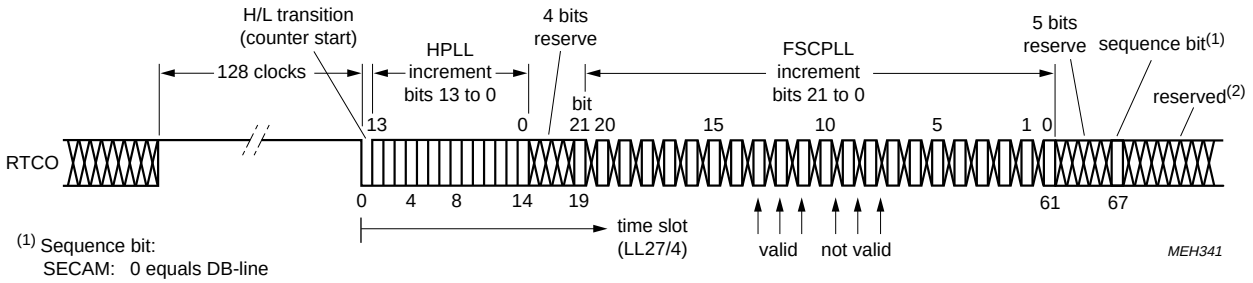


Fig.10 Line control by HREF in 4:2:2 format for 50 Hz and 60 Hz systems.



(1) Sequence bit:
SECAM: 0 equals DB-line
1 equals DR-line
PAL: 0 equals (R-Y) line normal
1 equals (R-Y) line inverted
NTSC: 0 (no change)

(2) Reserve bits: 236 for 50 Hz systems; 233 for 60 Hz systems

Fig.11 RTCO timing.

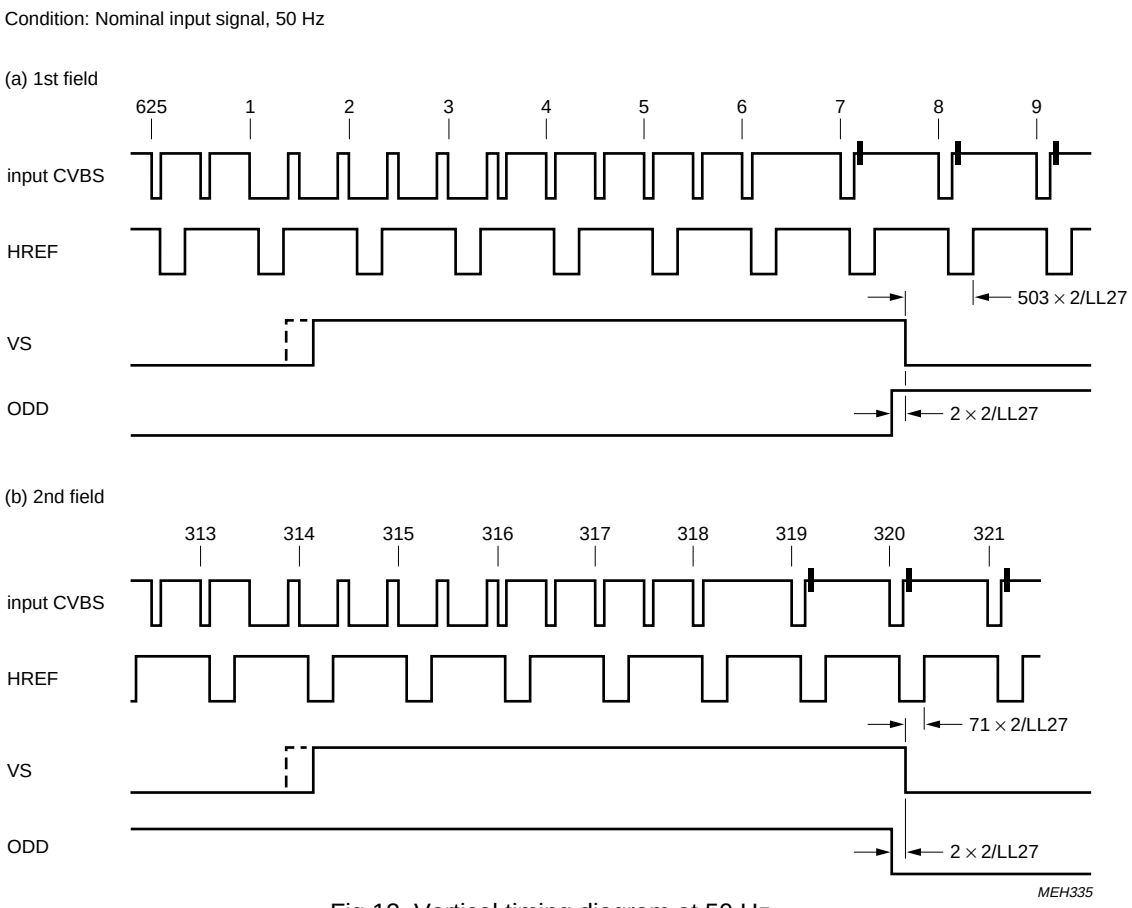


Fig.12 Vertical timing diagram at 50 Hz.

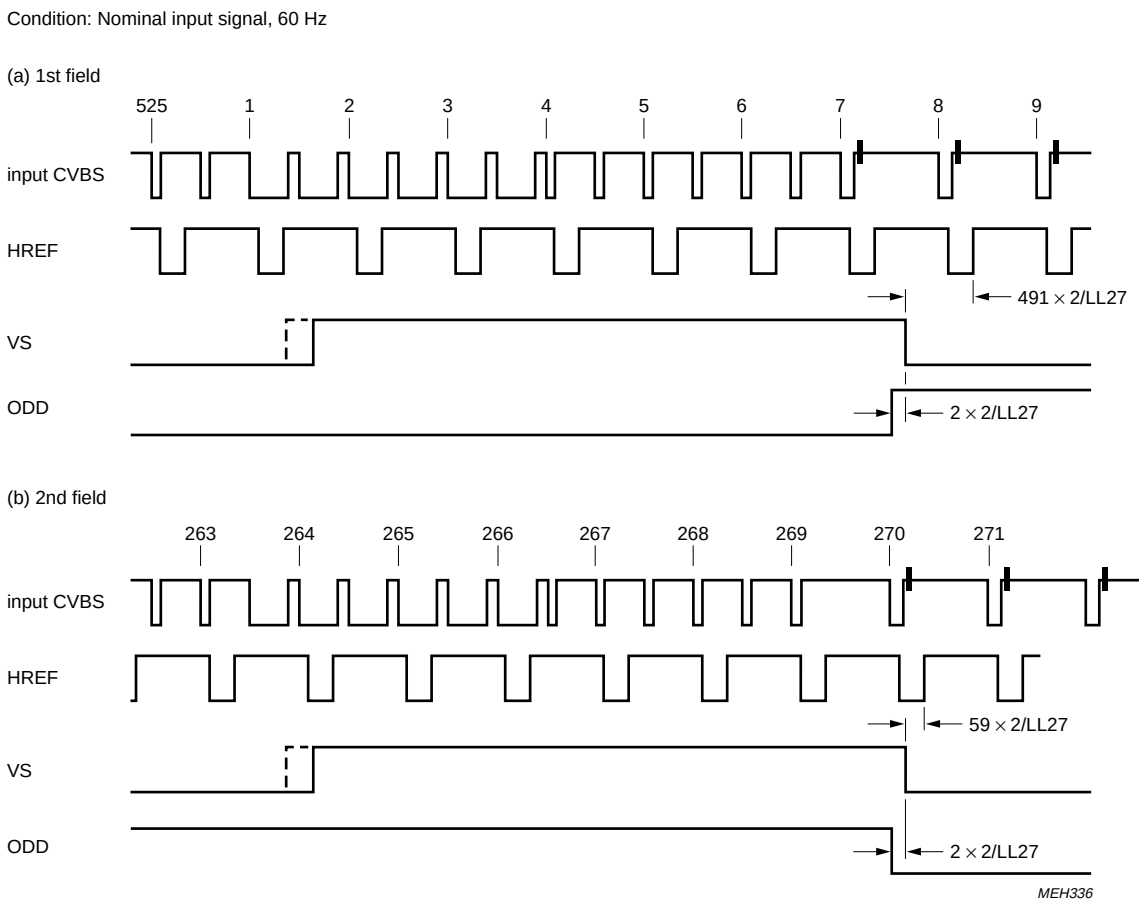
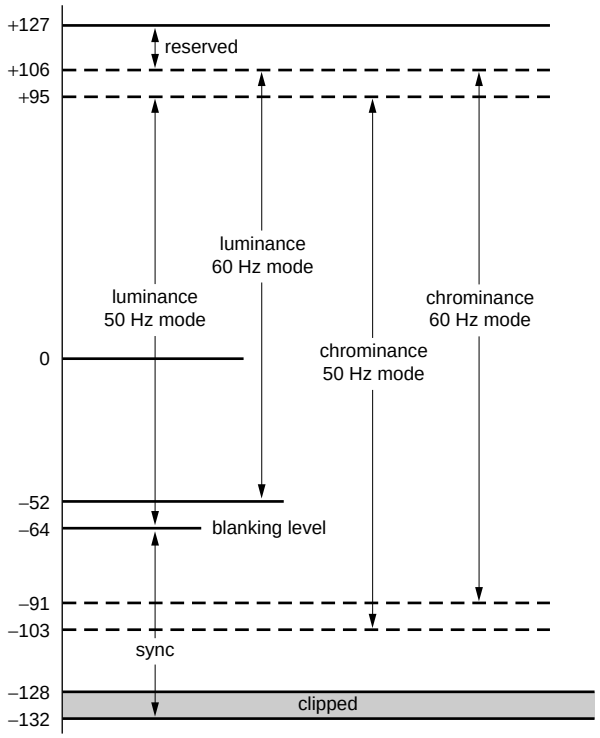
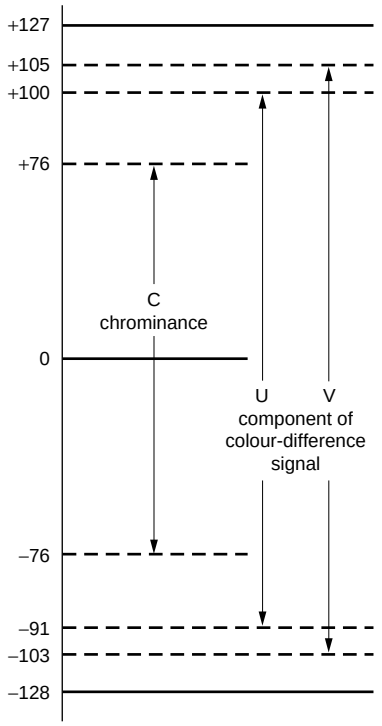


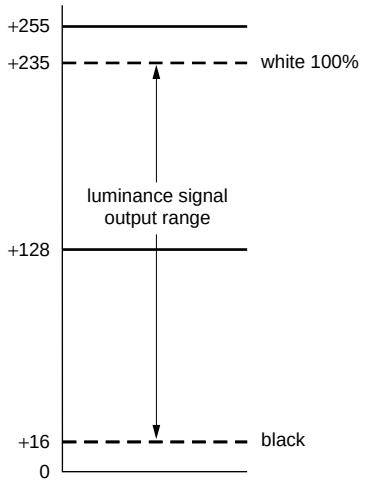
Fig.13 Vertical timing diagram at 60 Hz.



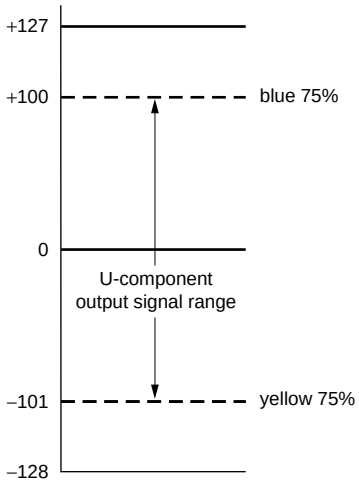
(a) CVBS input signal range.



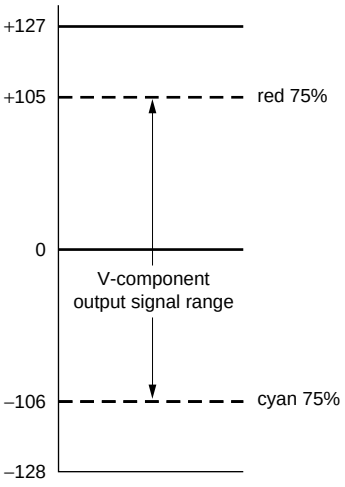
(b) CUV input signal range (U and V out of RGB; in FS mode ranges × 0.5).



(c) Y output signal range.



(d) U output signal range (B - Y).

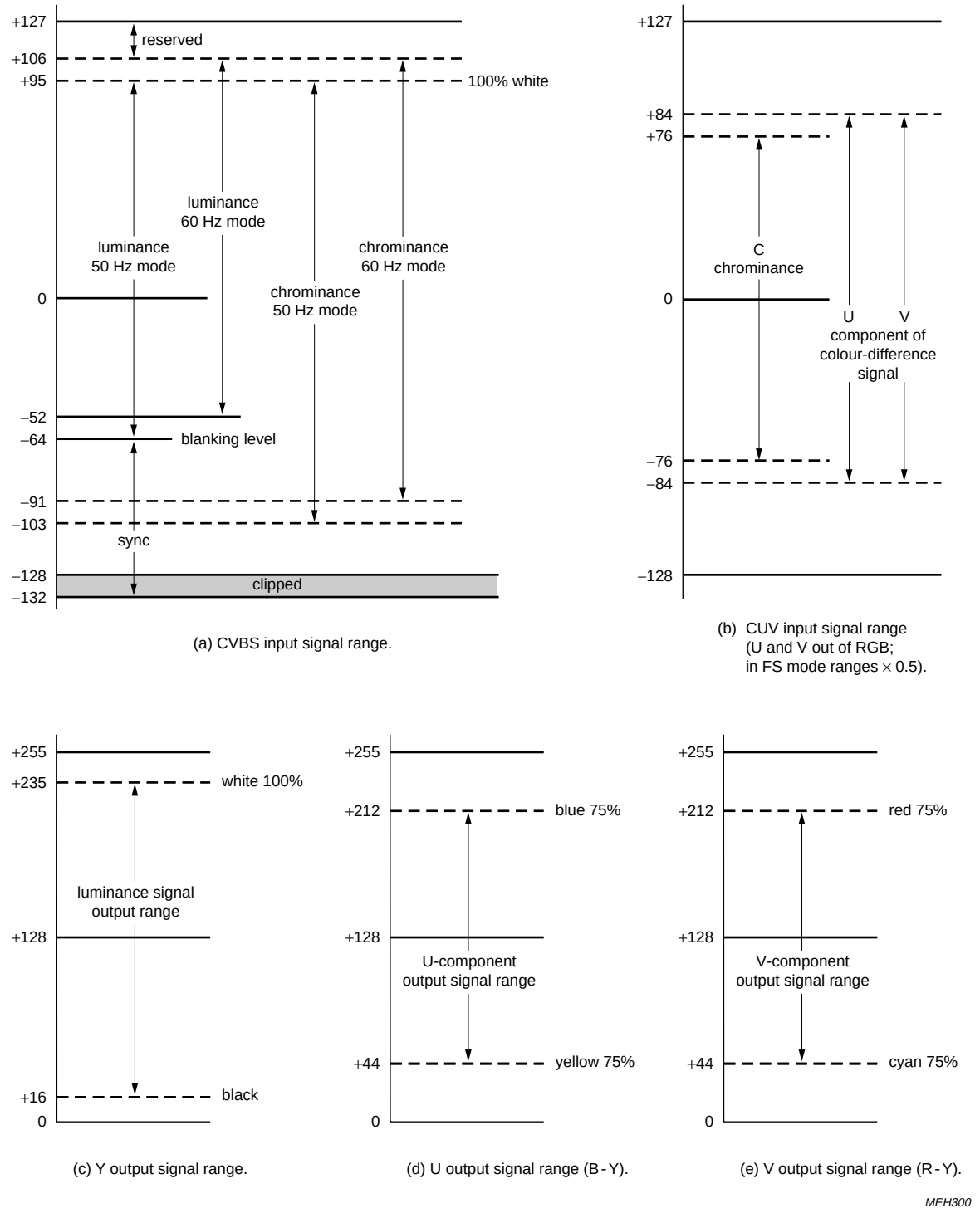


(e) V output signal range (R - Y).

MEH299

Notes: 1. All levels related to EBU colour bar.
2. Values in decimal at 100% luminance and 75% chrominance amplitude

Fig.14 Input and output signal ranges in DTV mode (digital TV).



(a) CVBS input signal range.

(b) CUV input signal range (U and V out of RGB; in FS mode ranges × 0.5).

(c) Y output signal range.

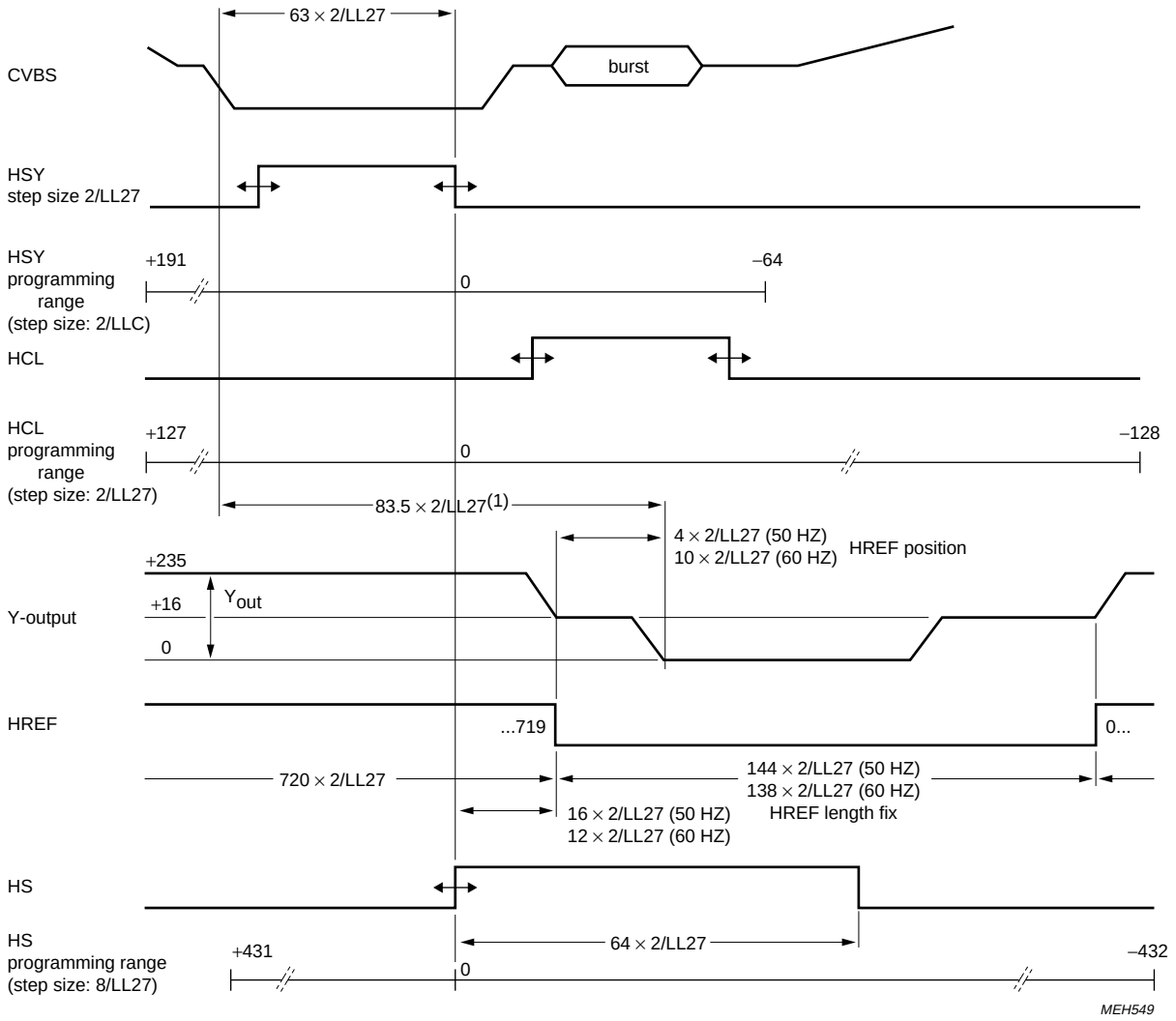
(d) U output signal range (B-Y).

(e) V output signal range (R-Y).

MEH300

Notes: 1. All levels are related to EBU colour bar.
2. Values in decimal at 100 % luminance and 75 % chrominance amplitude.
3. For SECAM input signals the CCIR levels will be exceeded.

Fig.15 Input and output signal ranges in CCIR mode.



(1) the processing delay will be influenced in future enhancements.

Fig.16 Horizontal sync and clamping timing for 50/60 Hz (signals HSY, HCL, HREF and HS).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins 19, 35, 38, 51 and 67 as well as supply pins 5, 18, 28, 37 and 52 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 18, 28, 37, 52)	−0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{SS\ A} - V_{SS(1\ to\ 4)}$	−	±100	mV
V_I	voltage on all inputs	−0.5	V_{DD}+0.5	V
V_O	voltage on all outputs ($I_{O\ max}$ = 20 mA)	−0.5	V_{DD}+0.5	V
P_{tot}	total power dissipation	−	2.5	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling[1] for all pins	−	±2000	V

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor; inputs and outputs are protected against electrostatic discharge in normal handling. Normal precautions appropriate to handle MOS devices is recommended (*"Handling MOS Devices"*).

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 5, 18, 28, 37, 52)		4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37, 52)	V_{DD} = 5 V; inputs LOW; outputs not connected	–	100	250	mA
I²C-bus, SDA and SCL (pins 40 and 41)						
$V_{I\,L}$	input voltage LOW		–0.5	–	1.5	V
$V_{I\,H}$	input voltage HIGH		3	–	V_{DD}+0.5	V
$I_{40,\,41}$	input current		–	–	±10	μA
I_{ACK}	output current on pin 40	acknowledge	3	–	–	mA
$V_{O\,L}$	output voltage at acknowledge	I_{40} = 3 mA	–	–	0.4	V
Data, clock and control inputs (pins 3, 4, 6 to 17, 20 to 23, 27, 34, 64 and 68); Figures 14 and 15						
$V_{I\,L}$	LL27 input voltage (pin 27)	LOW	–0.5	–	0.6	V
$V_{I\,H}$		HIGH	2.4	–	V_{DD}+0.5	V
$V_{I\,L}$	other input voltages	LOW	–0.5	–	0.8	V
$V_{I\,H}$		HIGH	2.0	–	V_{DD}+0.5	V
I_{leak}	input leakage current		–	–	10	μA
C_I	input capacitance	data inputs; note 1	–	–	8	pF
		I/O high-impedance	–	–	8	pF
		clock inputs	–	–	10	pF
$t_{SU.DAT}$	input data set-up time	Fig.17	11	–	–	ns
$t_{HD.DAT}$	input data hold time		3	–	–	ns
YUV-bus, HREF and VS outputs (pins 30, 42, 45 to 50 and pins 53 to 62), Figures 10, 14 and 15						
$V_{O\,L}$	output voltage LOW	notes 1 and 2	0	–	0.6	V
$V_{O\,H}$	output voltage HIGH		2.4	–	V_{DD}	V
C_L	load capacitor		15	–	50	pF
LFCO output (pin 36)						
V_o	output signal (peak-to-peak value)	note 2	1.4	–	2.6	V
V_{36}	output voltage range		1	–	V_{DD}	V
Control outputs (pins 24 to 26, 29, 31, 32, 33, 39, 63, 65 and 66); Figures 12, 16 and 17						
$V_{O\,L}$	output voltage LOW	notes 1 and 2	0	–	0.6	V
$V_{O\,H}$	output voltage HIGH		2.4	–	V_{DD}	V
C_L	load capacitor		7.5	–	25	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing of YUV-bus and control outputs		Figures 10, 12 and 13				
t_{OH}	output signal hold time	YUV, HREF, VS at C_L = 15 pF;	13	–	–	ns
		controls at C_L = 7.5 pF	13	–	–	ns
t_{OS}	output set-up time	YUV, HREF, VS at C_L = 50 pF;	20	–	–	ns
		controls at C_L = 25 pF	20	–	–	ns
t_{SZ}	data output disable transition time	to 3-state condition	22	–	–	ns
t_{ZS}	data output enable transition time	from 3-state condition	20	–	–	ns
Chrominance PLL						
f_C	catching range		±400	–	–	Hz
Crystal oscillator		Figures 19 and 20; note 3				
f_n	nominal frequency	3rd harmonic	–	24.576	–	MHz
$\Delta f / f_n$	permissible deviation f_n		–	–	±50	10^{-6}
	temperature deviation from f_n		–	–	±20	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	–	70	°C
	load capacitance C_L		8	–	–	pF
	series resonance resistance R_S		–	40	80	Ω
	motional capacitance C_1		–	1.5±20%	–	fF
	parallel capacitance C_0		–	3.5±20%	–	pF
Line locked clock input LL27 (pin 27)		Fig.9 and 17				
t_{LL27}	cycle time	note 4	35	–	39	ns
t_p	duty factor	t_{LL27H} / t_{LL27}	40	50	60	%
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	6	ns

Notes

1. Data output signals are Y7 to Y0 and UV7 to UV0. All other are control signals.
2. Levels are measured with load circuit. YUV-bus, HREF and VS outputs with 1.2 kΩ in parallel to 50 pF at 3 V (TTL load);

   LFCO output with 10 kΩ in parallel to 15 pF and other outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load).
3. Recommended crystal: Philips 4322 143 05291.
4. t_{SU}, t_{HD}, t_{OH} and t_{OD} include t_r and t_f.

Table 4 High-impedance control for YUV-bus (Fig.17)

OEDY	OEDC	FEIN	Y(7:0)	UV(7:0)
0	0	0	Z	Z
0	1	0	Z	active
1	0	0	active	Z
1	1	0	Z	Z
X	X	1	Z	Z

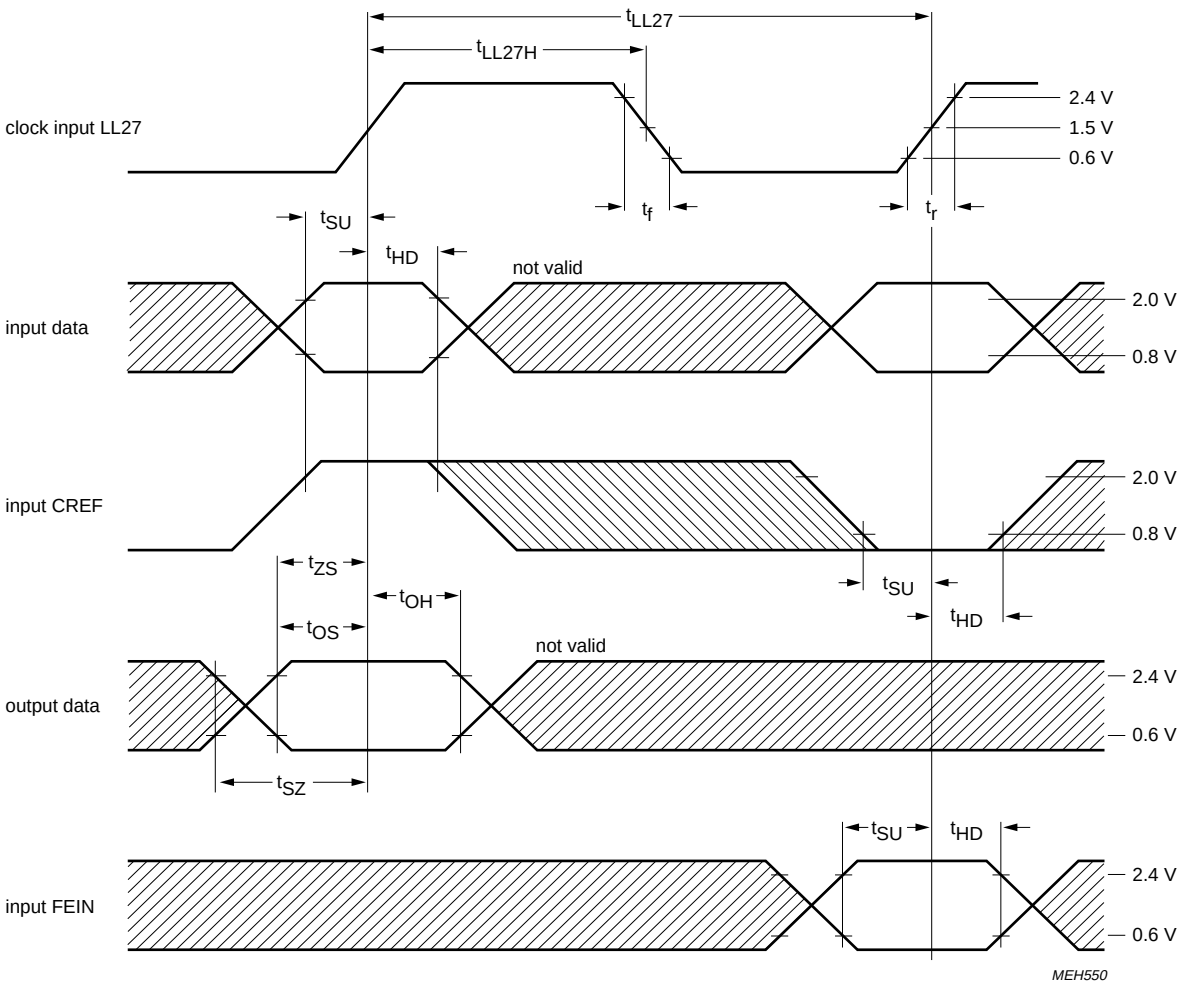
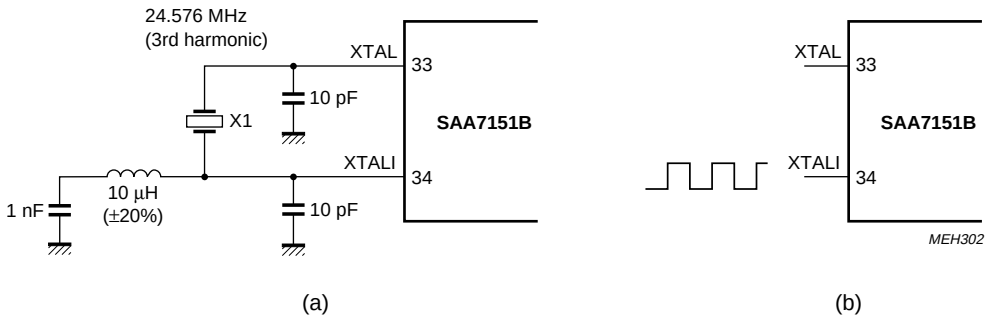


Fig.17 Data input and output timing diagram.



(a) (b)

Fig.18 Oscillator application (a) and optional clock from external (b).

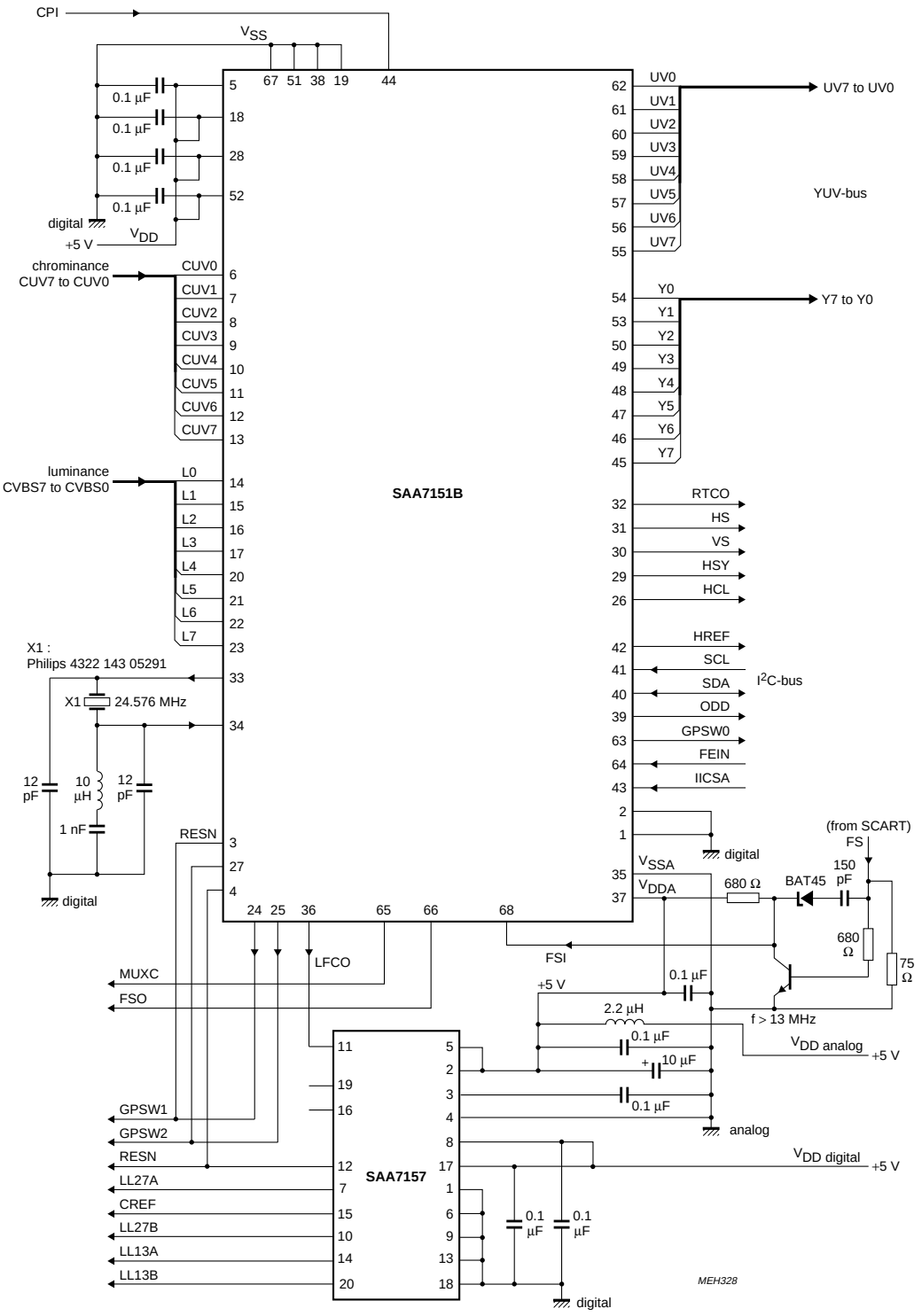


Fig.19 Application of SAA7151B.

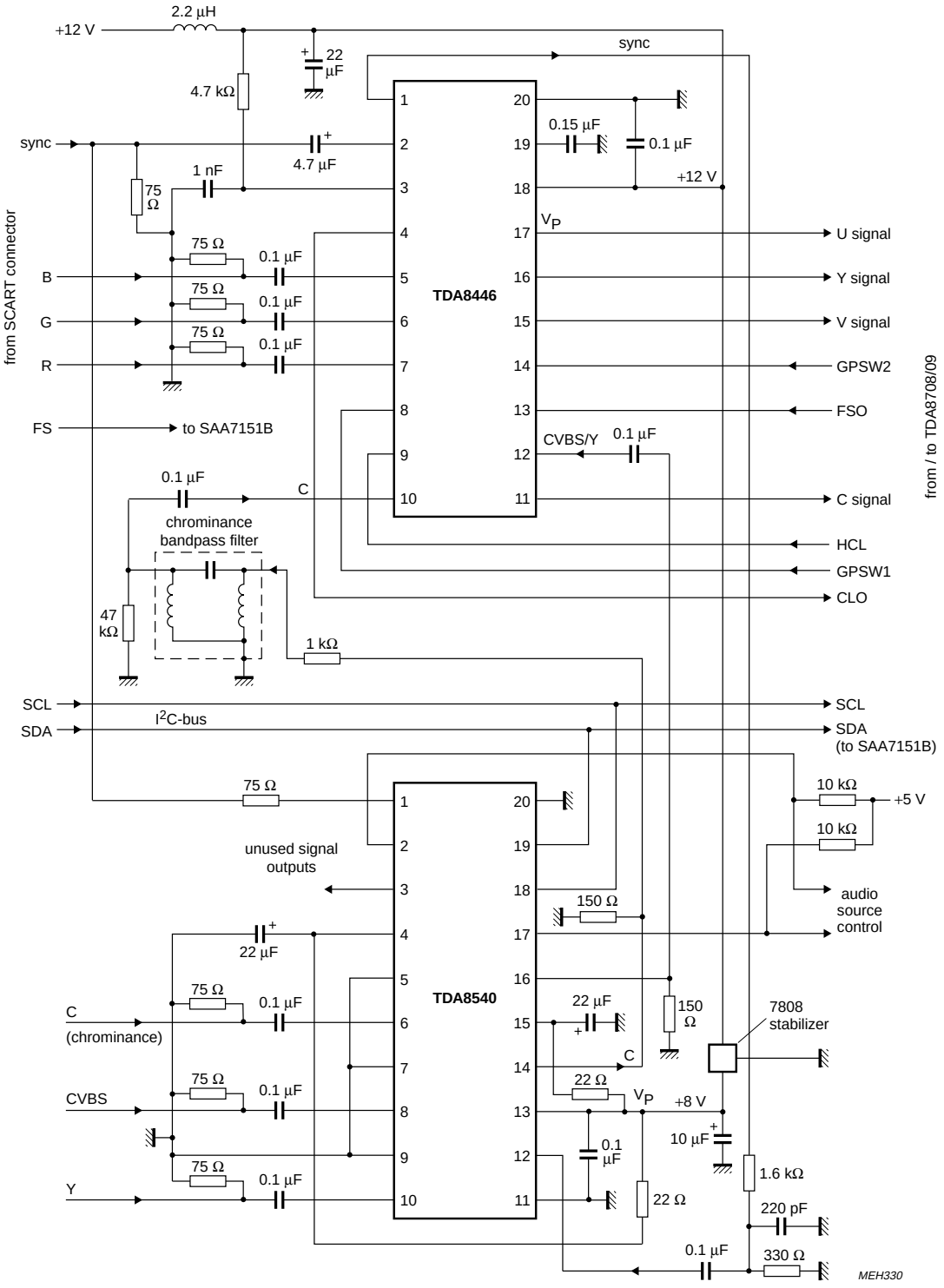


Fig.20 Application of input signal selecting (SCART interface).

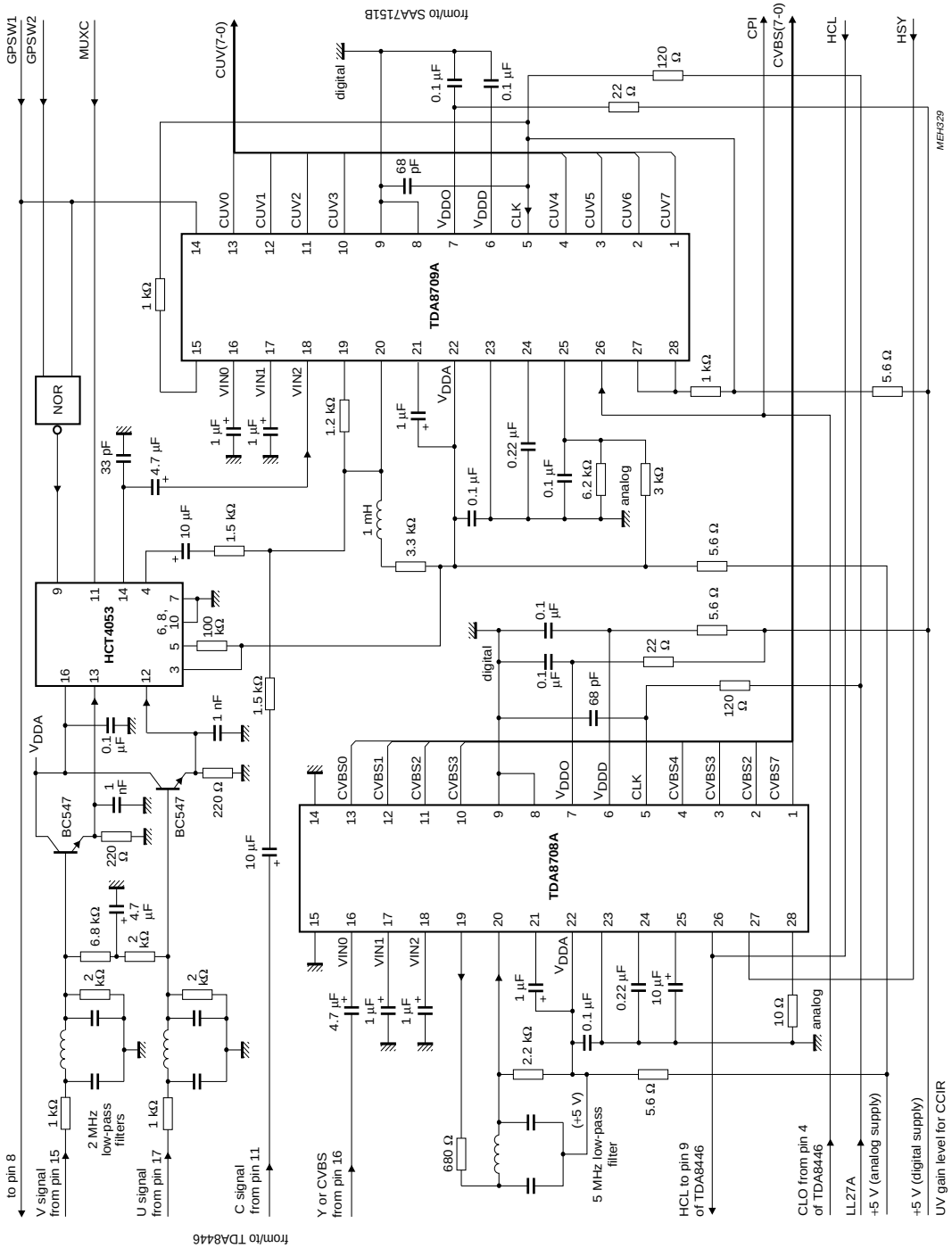


Fig.21 Application circuit analog-to-digital conversions.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S	=	start condition
SLAVE ADDRESS	=	**1000 101X** (IICSA = LOW) **or 1000 111X** (IICSA = HIGH)
A	=	acknowledge, generated by the slave
SUBADDRESS(1)	=	subaddress byte (Table 5)
DATA	=	data byte (Table 5)
P	=	stop condition
X	=	read/write control bit X = 0, order to write (the circuit is slave receiver) X = 1, order to read (the circuit is slave transmitter)

Note

1. If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Remarks: - Prior to reset of the IC all outputs are undefined.
- After power-on reset, the control register 12 (hex) is set to 00 (hex).

Table 5 I²C-bus; DATA for status byte (X in address byte = 1; slave address 8B (hex) at IICSA = LOW or 8F (hex) at IICSA = HIGH)

FUNCTION		DATA							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
status byte		STTC	HLCK	FIDT	FSST1	FSST0	CDET2	CDET1	CDET0

Function of the bits:

STTC — Status time constant (to be used for gogical combfilter SAA7152)
0 = TV mode; 1 = VCR mode

HLCK — Horizontal PLL information: 0 = HPLL locked; 1 = HPLL unlocked

FIDT — Field information: 0 = 50 Hz system detected; 1 = 60 Hz system detected

FSST1 to FSST0 — Fast switching output mode:

FSST1	FSST0	mode
0	0	RGB; FSI = HIGH (pin 68)
0	1	Y/C; FSI = LOW (pin 68)
1	0	fast switching (toggle)
1	1	not used

CDET2 to CDET0 — Identified colour standard

CDET2	CDET2	CDET2	standard
0	0	0	PAL-B/G, -H, -I; 50 Hz
0	0	1	PAL-N; 50 Hz
0	1	0	SECAM; 50 Hz
0	1	1	PAL-M; 60 Hz
1	0	0	PAL 4.43; 60 Hz
1	0	1	NTSC-M; 60 Hz
1	1	0	NTSC 4.43; 60 Hz
1	1	1	black/white

Table 6 I²C-bus; subaddress and data bytes for writing (X in address byte = 0; slave address 8A (hex) at IICSA = LOW or 8E at IICSA = HIGH)

function	subaddress byte	data byte							
		D7	D6	D5	D4	D3	D2	D1	D0
increment delay	00	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0
H-sync HSY begin	01	HSYB7	HSYB6	HSYB5	HSYB4	HSYB3	HSYB2	HSYB1	HSYB0
H-sync HSY stop	02	HSYS7	HSYS6	HSYS5	HSYS4	HSYS3	HSYS2	HSYS1	HSYS0
H-clamp HCL begin	03	HCLB7	HCLB6	HCLB5	HCLB4	HCLB3	HCLB2	HCLB1	HCLB0
H-clamp HCL stop	04	HCLS7	HCLS6	HCLS5	HCLS4	HCLS3	HCLS2	HCLS1	HCLS0
H-sync after PHI1	05	HPHI7	HPHI6	HPHI5	HPHI4	HPHI3	HPHI2	HPHI1	HPHI0
luminance control	06	BYPS	PREF	BPSS1	BPSS0	BFBY	CORI	APER1	APER0
hue control	07	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
miscellaneous controls #1	08	CSTD2	CSTD1	CSTD0	CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0
miscellaneous controls #2	09	OSCE	LFIS1	LFIS0	CKTS4	CKTS3	CKTS2	CKTS1	CKTS0
PAL switch sensitivity	0A	PLSE7	PLSE6	PLSE5	PLSE4	PLSE3	PLSE2	PLSE1	PLSE0
SECAM switch sensitivity	0B	SESE7	SESE6	SESE5	SESE4	SESE3	SESE2	SESE1	SESE0
miscellaneous controls #3	0C	FSAU	GPSI2	GPSI1	CGFX	AMPF3	AMPF2	AMPF1	AMPF0
miscellaneous controls #4	0D	COLO	CHSB	GPSW0	SUVI	SXCR	FSDL2	FSDL1	FSDL0
miscellaneous controls #5	0E	CCIR	COFF	OEHS	OEVS	UVSS	CHRS	CDMO	CDPO
miscellaneous controls #6	0F	AUFD	FSEL	HPLL	SCEN	VTRC	MUIV	FSIV	WIND
miscellaneous controls #7	10	ASTD	OFTS	IPBP	CDVI	YDEL3	YDEL2	YDEL1	YDEL0
chroma gain reference	11	CHCV7	CHCV6	CHCV5	CHCV4	CHCV3	CHCV2	CHCV1	CHCV0
miscellaneous controls #8	12	OEDY	OEDC	VNOI1	VNOI0	BFON	BOFL2	BOFL1	BOFL0

Function of the bits of Table 6

IDEL7 to IDEL0	Increment delay time, step size = 4/LL27 = 148 ns[1]									
"00"	D7	D6	D5	D4	D3	D2	D1	D0	decimal number	note
	1	1	1	1	1	1	1	1	–1 to –110	minimum –148 ns
	1	0	0	1	0	0	1	0		–16.3 µs (outside available range)
	1	0	0	1	0	0	0	1	–111 to –214	–16.44 µs
	0	0	1	0	1	0	1	0		–31.7 µs (maximum value at FSEL = 1)
	0	0	1	0	1	0	0	1	–215	–31.85 µs (outside central counter range at FSEL = 1 [2])
	0	0	1	0	1	0	0	0	–216	–32.0 µs (maximum value at FSEL = 0 [2])
	0	0	1	0	0	1	1	1	–217 to –256	–32.148 µs (outside central counter range at FSEL = 0 [2])
	0	0	0	0	0	0	0	0		–37.9 µs (outside central counter [2])
HSYB7 to HSYB0	Horizontal sync begin, step size = 2/LL27 = 74 ns									
HSYS7 to HSYS0	Horizontal sync stop, step size = 2/LL27 = 74 ns									
"01" and "02"	D7	D6	D5	D4	D3	D2	D1	D0	decimal multiplier	note
	1	0	1	1	1	1	1	1	191 to 1	–14.2 µs (maximum negative value)
	0	0	0	0	0	0	0	1		–74 ns
	0	0	0	0	0	0	0	0	0	0 equals reference value
	1	1	1	1	1	1	1	1	–1 to –64	+74 ns
	1	1	0	0	0	0	0	0		+4.7 µs
HCLB7 to HCLB0	Horizontal clamp begin, step size = 2/LL27 = 74 ns									
HCLS7 to HCLS0	Horizontal clamp stop, step size = 2/LL27 = 74 ns									
"03" and "04"	D7	D6	D5	D4	D3	D2	D1	D0	decimal multiplier	note
	0	1	1	1	1	1	1	1	127 to 1	–9.4 µs (maximum negative value)
	0	0	0	0	0	0	0	1		–74 ns
	0	0	0	0	0	0	0	0	0	0 equals reference value
	1	1	1	1	1	1	1	1	–1 to –128	+74 ns
	1	0	0	0	0	0	0	0		+9.5 µs (maximum positive value)
HPHI7 to HPHI0	Horizontal sync start, step size = 8/LL27 = 296 ns									
"05"	D7	D6	D5	D4	D3	D2	D1	D0	decimal multiplier	note
	0	1	1	1	1	1	1	1	+127 to +109	) forbidden (outside available central
	0	1	1	0	1	1	0	1		) counter range)
	0	1	1	0	1	1	0	0	+108 to +1	–32 µs (maximum negative value)
	0	0	0	0	0	0	0	1		–0.296 ns
	0	0	0	0	0	0	0	0	0	0 equals reference value
	1	1	1	1	1	1	1	1	–1 to –107	+0.296 µs
	1	0	0	1	0	1	0	1		+31.7 µs (maximum positive value)
	1	0	0	1	0	1	0	0	–108 to –128	) forbidden (outside available central
	1	0	0	0	0	0	0	0		) counter range)

BYPS "06": Input mode select bit: 0 = CVBS mode (chroma trap active); 1 = S-Video mode (chroma trap by-passed)

PREF: Use of pre-emphasis (to be used if chrominance trap is active): 0 = pre-filter bypassed; 1 = pre-filter on

BPSS1 to BPSS0: Aperture bandpass to select different centre frequencies (Figures 25 to 40):

BPSS1	BPSS0	centre frequency
0	0	4.1 MHz
0	1	3.8 MHz
1	0	2.6 MHz
1	1	2.9 MHz

BFBY: Bandfilter bypass switching: 0 = bandfilter active; 1 = bandfilter bypassed

CORI: Coring function: 0 = coring off; 1 = ±1 LSB coring

APER1 to APER0: Aperture factor (Figures 25 to 40):

APER1	APER0	factor
0	0	0
0	1	0.25
1	0	0.5
1	1	1

HUE7 to HUE0 "07": Hue control from +178.6° to −180.0°, equals data bytes 7F to 80 (hex); 0° equals 00.

CSTD2 to CSTD0 "08": Forced colour standard of input signal;

CSTD2	CSTD1	CSTD0	standard
0	0	0	PAL-B/G, -H, -I; 50 Hz
0	0	1	PAL-N; 50 Hz
0	1	0	SECAM; 50 Hz
0	1	1	PAL-M; 60 Hz
1	0	0	PAL 4.43; 60 Hz
1	0	1	NTSC-M; 60 Hz
1	1	0	NTSC 4.43; 60 Hz
1	1	1	black/white

CKTQ4 to CKTQ0: Colour killer threshold QAM (PAL/NTSC):

CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0	
1	1	1	1	1	approximately −30 to −24 dB
1	0	0	0	0	−24 dB to −18 dB
0	0	0	0	0	

OSCE
"09"

External UV offset compensation: 0 = disabled; 1 = enabled

LFIS1 to LFIS0

Chrominance gain control (AGC filter):

LFIS1	LFIS0	control of loop filter time constant
0	0	slow
0	1	medium
1	0	fast
1	1	actual gain, stored (for test purposes only)

CKTS4 to CKTS0

Colour killer threshold SECAM as previously described under CKTQ subaddress "08"

PLSE7 to PLSE0
"0A"

PAL switch sensitivity from LOW to HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.

SESE7 to SESE0
"0B"

SECAM switch sensitivity from LOW to HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.

FSAU; GPSI2, and GPSI1
"0C"

Set port outputs (general purpose switching, internal)

FSAU	GPSI2	GPSI1	output GPSW2 (pin 25)	output GPSW1 (pin 24)
0	0	0	LOW	LOW
0	0	1	LOW	HIGH
0	1	0	HIGH	LOW
0	1	1	HIGH	HIGH
1	X	X	status bit FSST1 set	status bit FSST0 set

CGFX

Chrominance gain pre-determination: 0 = gain controlled via loop; 1 = gain set by AMPF-bits

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AMPF3 to AMPF0

Chrominance amplification factor

AMPF3	AMPF2	AMPF1	AMPF0	gain
0	0	0	0	–6 dB
0	1	0	0	0 dB
0	1	0	1	+1.5 dB
.	.	.	.	+3 to +16.5 dB (approximately 1.5 dB steps)
1	1	1	1	+17 dB

COLO “0D”	Colour-on bit:	0 = colour-killer automatically enabled; 1 = forced colour-on.
CHSB	Chrominance (UV) output code:	0 = two’s complement; 1 = straightly binary
GPSW0	General purpose port output (pin 63):	0 = LOW; 1 = HIGH
SUVI	SECAM UV output signal polarity:	0 = U and V positive; 1 = U and V negative
SXCR	SECAM cross-colour reduction:	0 = off; 1 = on
FDSL2 to FDSL0	Fast switching delay adjustment in 37 ns steps:	

FDSL2	FDSL1	FDSL0	delay
0	0	0	0
0	0	1	37 ns
0	1	0	74 ns
0	1	1	111 ns
1	0	0	−148 ns (negative delay)
1	0	1	−111 ns
1	1	0	−74 ns
1	1	1	−37 ns

CCIR “0E”	Set CCIR mode: 0 = digital TV mode (DTV); 1 = CCIR mode	
COFF	Set colour off: 0 = colour on; 1 = colour off	
OEHS	Enable horizontal sync outputs HS and HREF:	0 = output high-impedance; 1 = HS and HREF enabled
OEVS	Enable vertical sync output VS:	0 = output high-impedance; 1 = VS enabled
UVSS	Select UV pixel sample:	1 = first pixel after U/V signal has changed; 0 = second pixel (free of crosstalk signals)
CHRS	S-Video input mode:	0 = chrominance signal from CVBS or CUV input and controlled by BYPS (subaddress 06); 1 = S-Video mode; chrominance signal from CUV input
CDMO, CDPO	Chrominance delay:	

CDMO	CDPO	
0	0	no delay
1	X	−37 ns (negative delay)
0	1	+37 ns

AUFD “0F”	Automatic field detection:	0 = field selection by FSEL-bit; 1 = automatic field detection
FSEL	Field select (AUFD-bit = 0):	0 = 50 Hz (625 lines); 1 = 60 Hz (525 lines)
HPLL	Horizontal PLL:	0 = PLL closed; 1 = PLL open, horizontal frequency fixed
SCEN	Sync and clamping pulse enable:	0 = HCL and HSY outputs HIGH (pins 26 and 29); 1 = HCL and HSY outputs active.
VTRC	VTR/TV mode select:	0 = TV mode (slow time constant); 1 = VTR mode (fast time constant).
MUIV	MUXC signal invertion:	0 = inverted; 1 = not inverted
FSIV	Fast switch input signal inversion:	0 = not inverted; 1 = inverted
WIND	Narrow fast switch window:	0 = off; 1 = on

ASTD “10”	Automatic standard switching:	0 = off; 1 = on
OFTS	Select output format:	0 = 4 : 1 : 1 format; 1 = 4 : 2 : 2 format.
IPBP	External UV signal interpolation filter:	0 = active; 1 = bypassed
CDVI	Chrominance PLL filter selection for:	0 = VTR or TV source; 1 = fast time constant for FSC-PLL (only for special applications)
YDEL3 to YDEL0	Luminance delay compensation in 37 ns steps:	

YDEL3	YDEL2	YDEL1	YDEL0	delay
0	0	0	0	0 to 259 ns (step 0 to 7)
0	1	1	1	
1	0	0	0	−296 to −37 ns (negative delay; step -8 to -1)
1	1	1	1	

CHCV7 to CHCV0 “11” — Chroma gain reference value

D7	D6	D5	D4	D3	D2	D1	D0	gain	
1	1	1	1	1	1	1	1	maximum gain	default programmed values dependent on application
	:				:			to	
1	0	1	1	0	0	1	1	DTV level	
	:				:			to	
0	0	1	1	1	1	0	1	CCIR level	
	:				:			to	
0	0	0	0	0	0	0	0	minimum gain	

OEDY "12": Enable Y signals on YUV-bus: 0 = output high-impedance; 1 = output active (dependent on FEIN)

OEDC: Enable UV signals on YUV-bus: 0 = output high-impedance; 1 = output active (dependent on FEIN)

VNOI1, VNOI0: Vertical noise reduction mode:

VNOI1	VNOI0	mode
0	0	normal
0	1	searching
1	0	free-running
1	1	bypassed

BFON: Bottom flutter compensation switching: 0 = off; 1 = on (controlled by BOFL-bit)

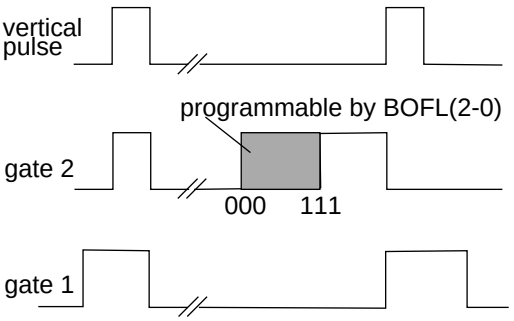
BOFL2 to BOFL0: Bottom flutter compensation

BOFL2	BOFL1	BOFL0	start at line number
0	0	0	297 for PAL (247 for NTSC; active to end of field)
0	0	1	298 for PAL (248 for NTSC; active to end of field)
.	.	.	. .
1	1	0	303 for PAL (253 for NTSC; active to end of field)
1	1	1	304 for PAL (254 for NTSC; active to end of field)

The bottom flutter circuit is able to compensate for horizontal phase jump of up to ±16 µs.

Note: The bottom flutter gate is active at
- HPLL is locked
- HPLL in VTR mode
- the vertical noise limiter (VNL) is in the VTR mode
- gating is switched by BFON-bit = 1 (subaddress 12)

Gate 2	Gate 1	HPLL function
0	0	normal
1	0	disabled
0	1	double speed
1	1	unused



Notes

1. an internal sign-bit D8 set to HIGH indicates that all values are always negative
2. H-PLL does not operate in this condition; the system clock frequency is set to a value fixed by the last update and is within ±7.1 % of the nominal frequency.

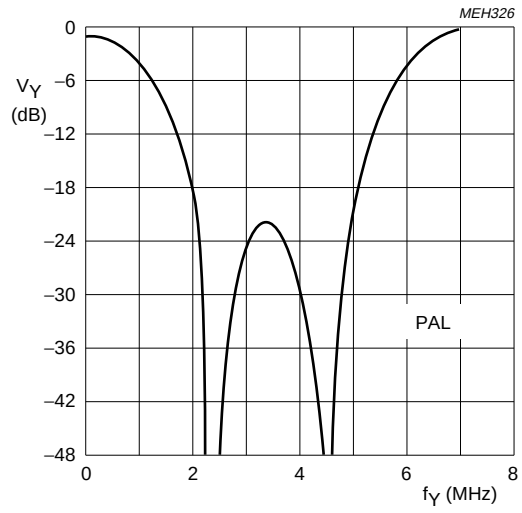


Fig.22 Frequency response of chroma stop filter in colour-difference mode for 50 Hz PAL. Filter is only active in fast switching mode, but bypassed in RGB mode. The selected filter is dependent on actual detected colour standard.

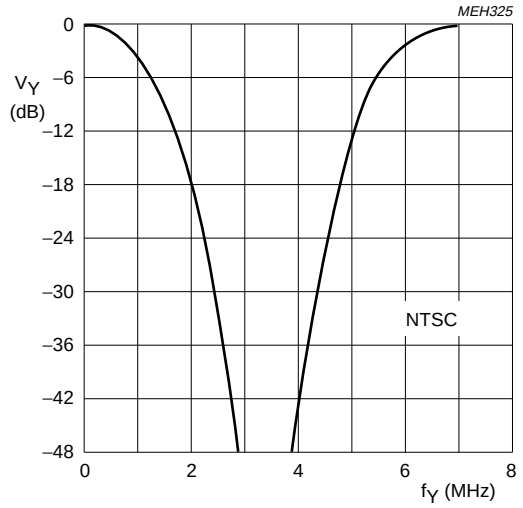


Fig.23 Frequency response of chroma stop filter in colour-difference mode for 60 Hz NTSC. Filter is only active in fast switching mode, but bypassed in RGB mode. The selected filter is dependent on actual detected colour standard.

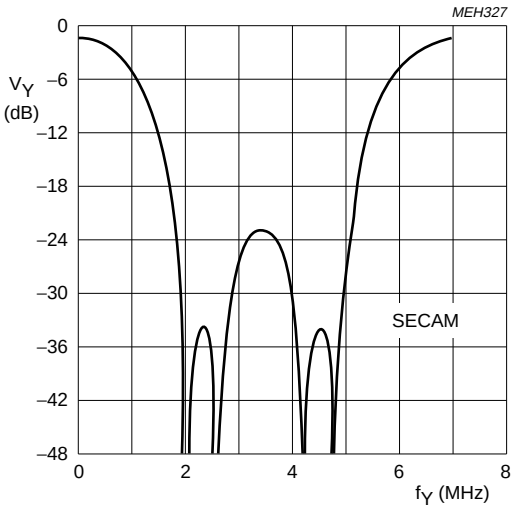


Fig.24 Frequency response of chroma stop filter colour-difference mode for 50 Hz SECAM. Filter is only active in fast switching mode, but bypassed in RGB mode. The selected filter is dependent on actual detected colour standard.

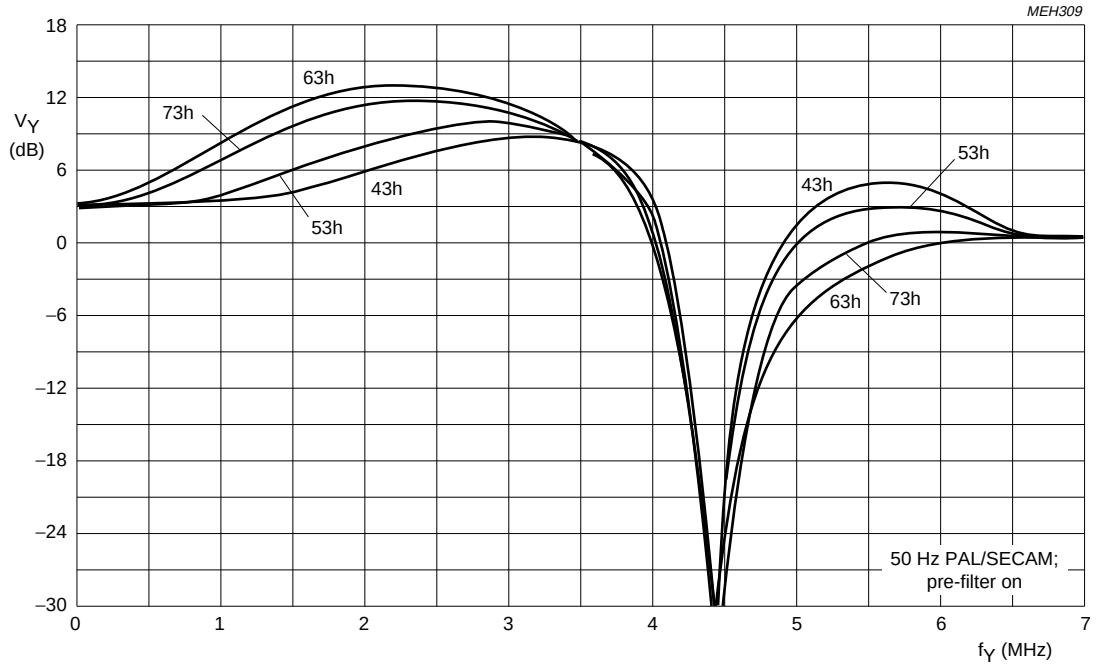


Fig.25 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter on; and bandfilter on.

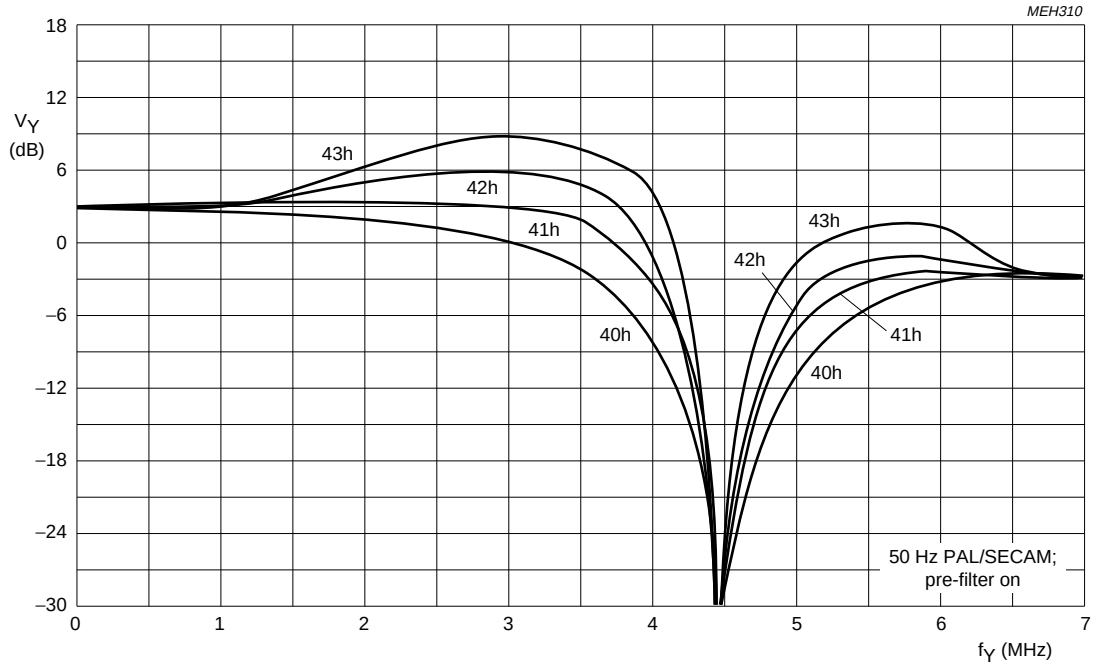


Fig.26 3.8 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter on and bandfilter on.

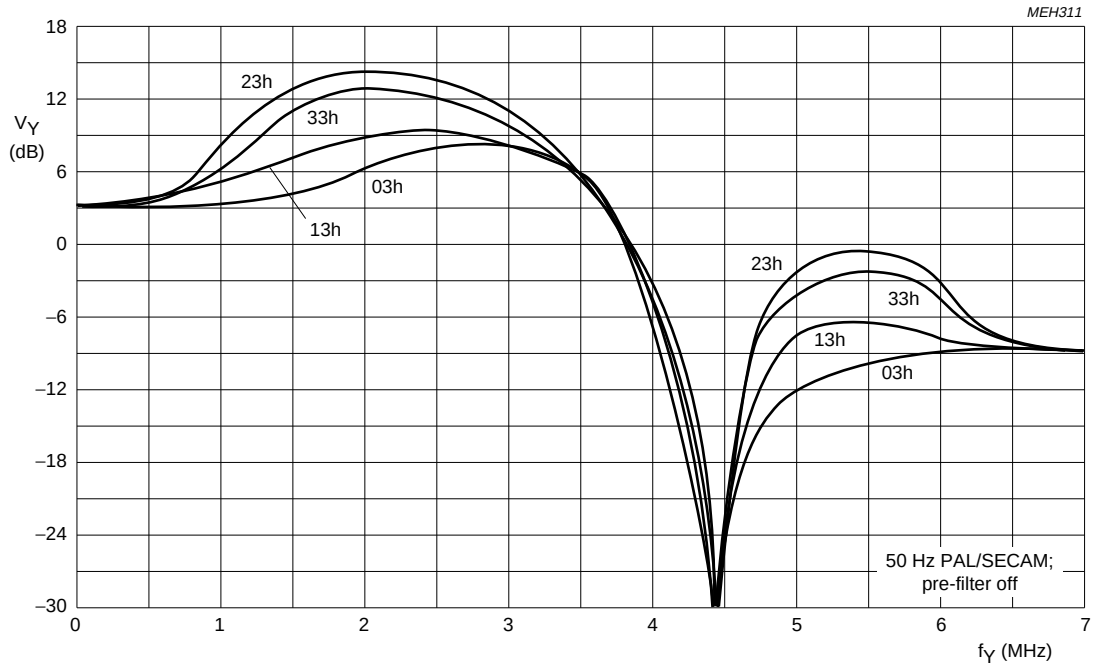


Fig.27 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter off; and bandfilter on.

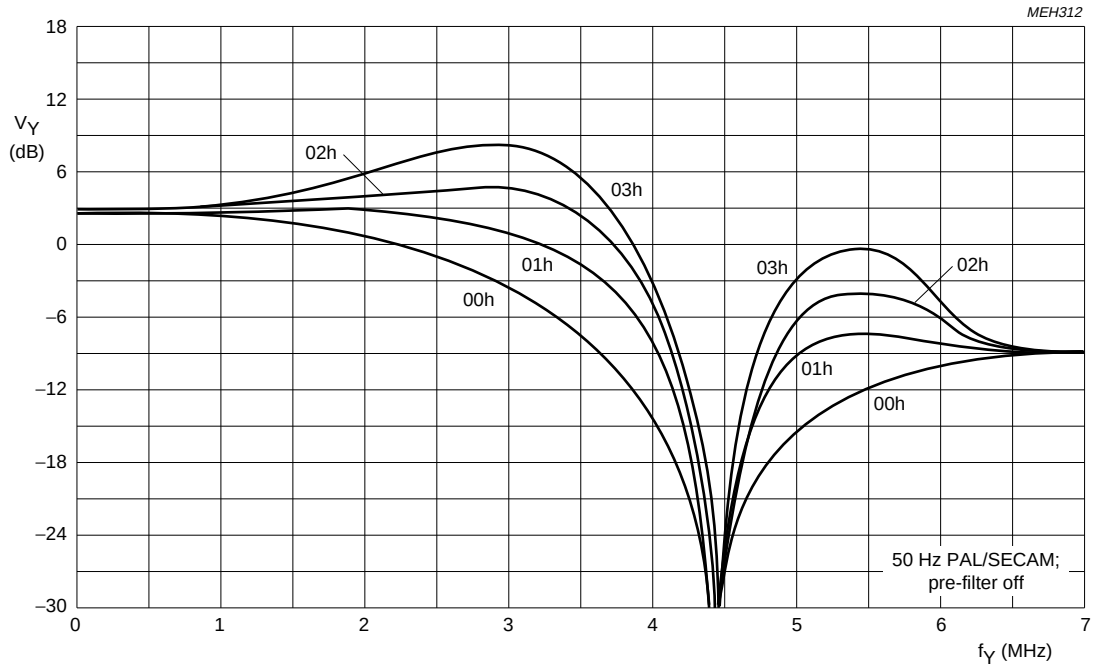


Fig.28 4.1 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter off and bandfilter on.

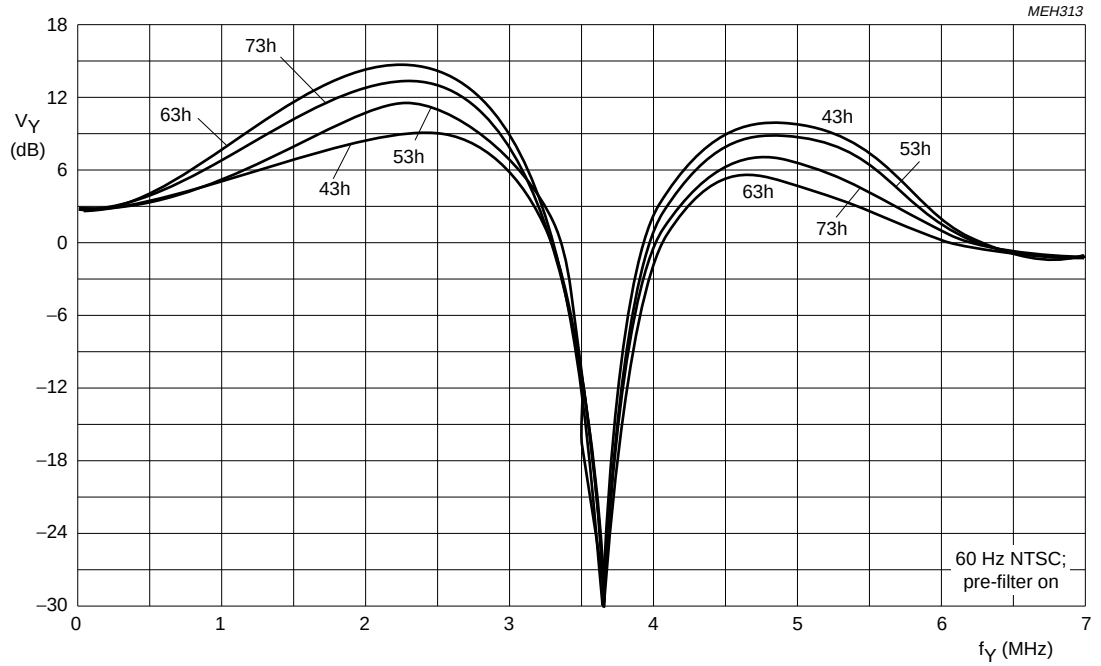


Fig.29 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter on; and bandfilter on.

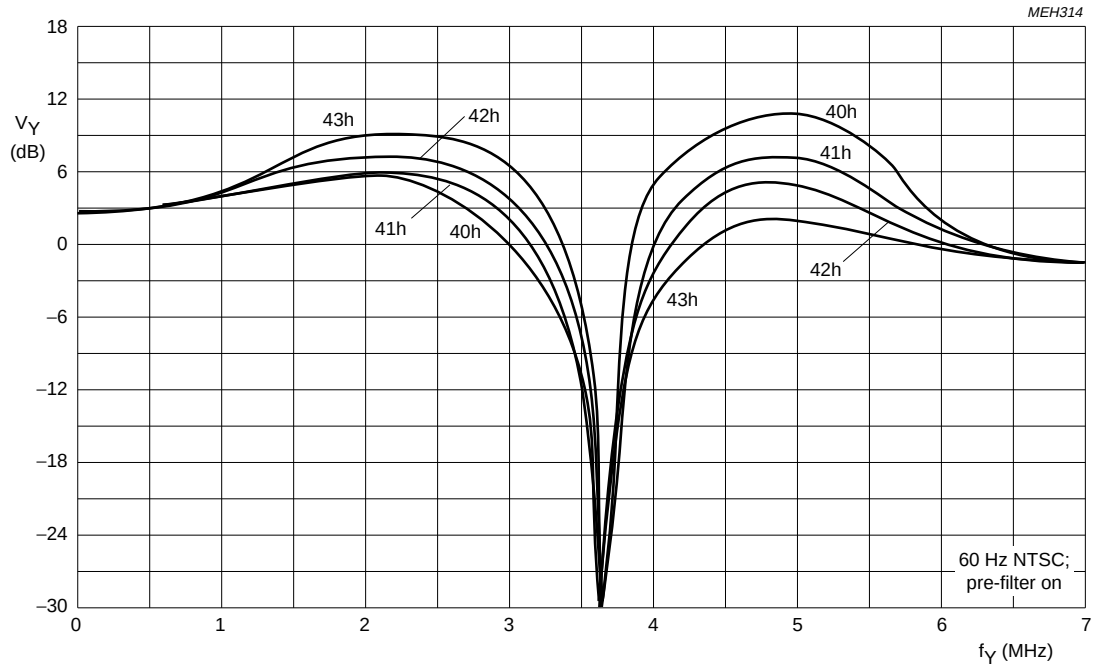


Fig.30 3.8 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter on and bandfilter on.

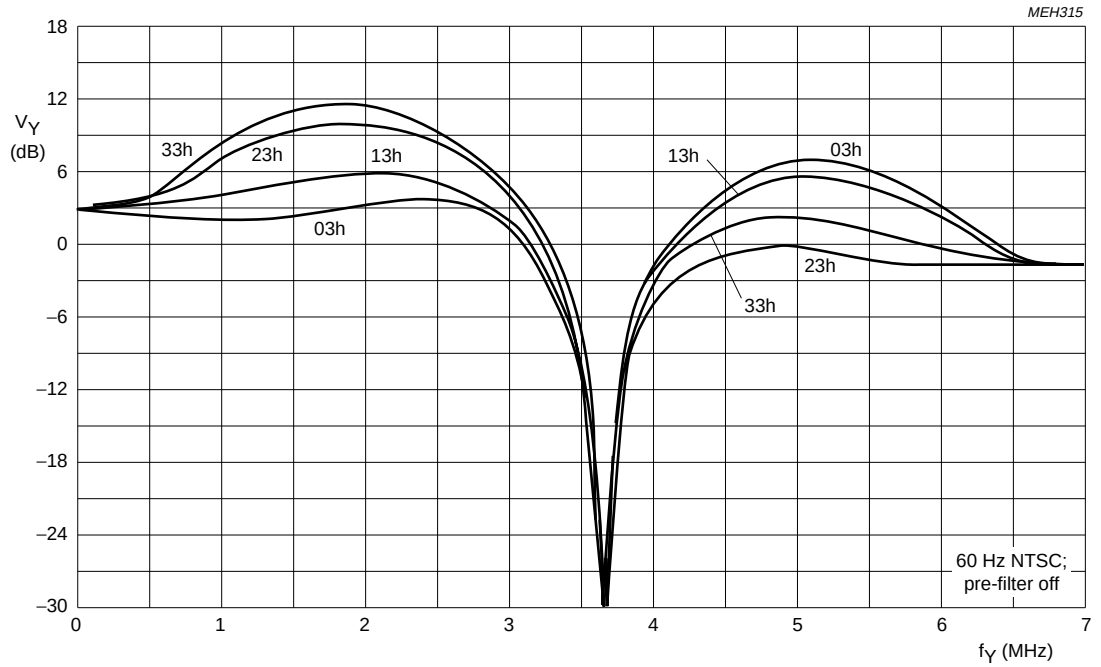


Fig.31 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter off; and bandfilter on.

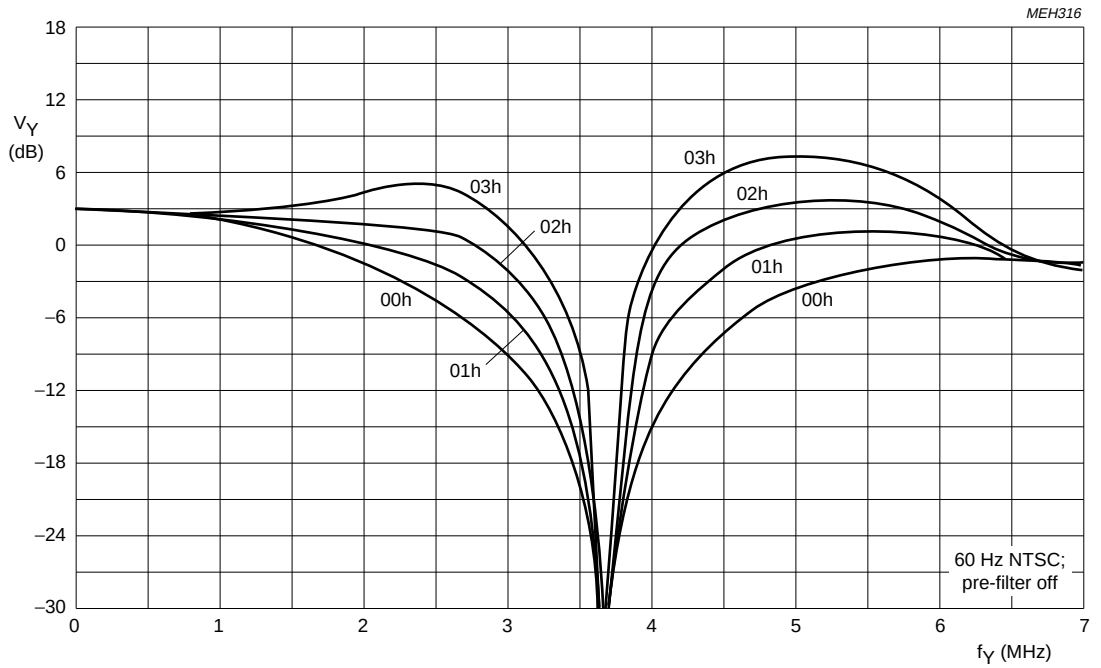


Fig.32 4.1 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter off and bandfilter on.

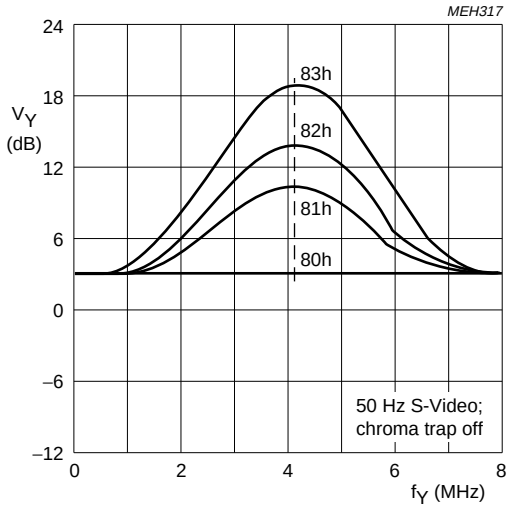


Fig.33 4.1 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

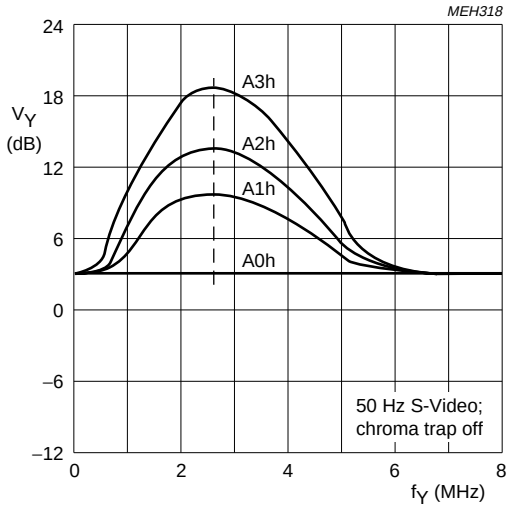


Fig.34 2.6 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

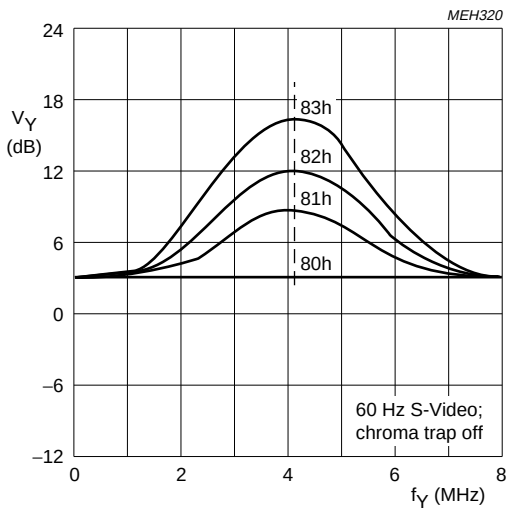


Fig.35 4.1 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

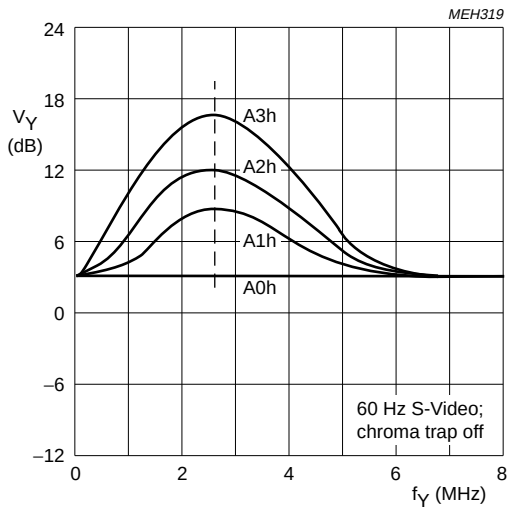


Fig.36 2.6 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

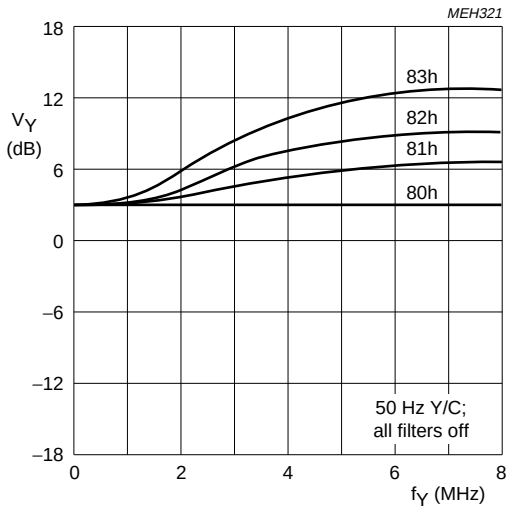


Fig.37 4.1 MHz luminance peaking control in 50 Hz / S-VHS mode as a function of four different aperture factors controllable by subaddress byte 06.

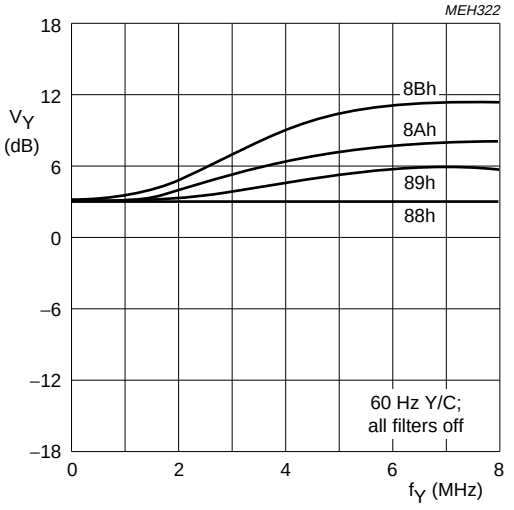


Fig.38 4.1 MHz luminance peaking control in 60 Hz / S-VHS mode as a function of four different aperture factors controllable by subaddress byte 06.

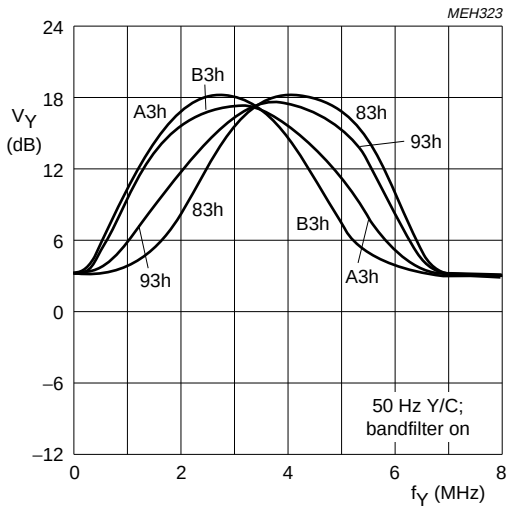


Fig.39 Maximum luminance peaking control in 50 Hz / S-VHS mode as a function of four aperture centre frequencies controllable by subaddress byte 06.

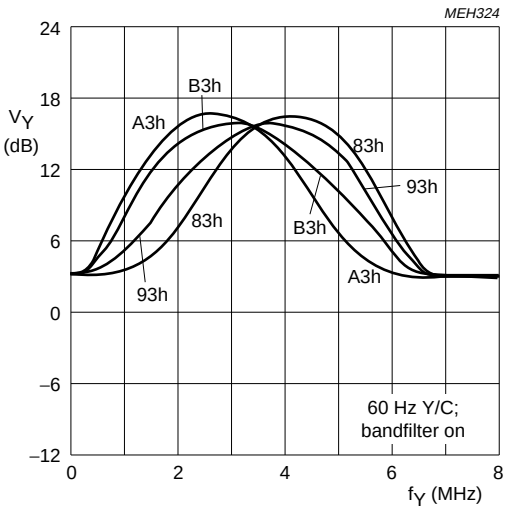


Fig.40 Maximum luminance peaking control in 60 Hz / S-VHS mode as a function of four aperture centre frequencies controllable by subaddress byte 06.

PROGRAMMING EXAMPLE

Coefficients to set operation for application circuits Figures 19, 20 and 21. Values recommended for PAL CVBS input signal and 4:2:2 CCIR output signal (all numbers of the Table 6 are hex values).

Table 7 Recommended default values (note 1)

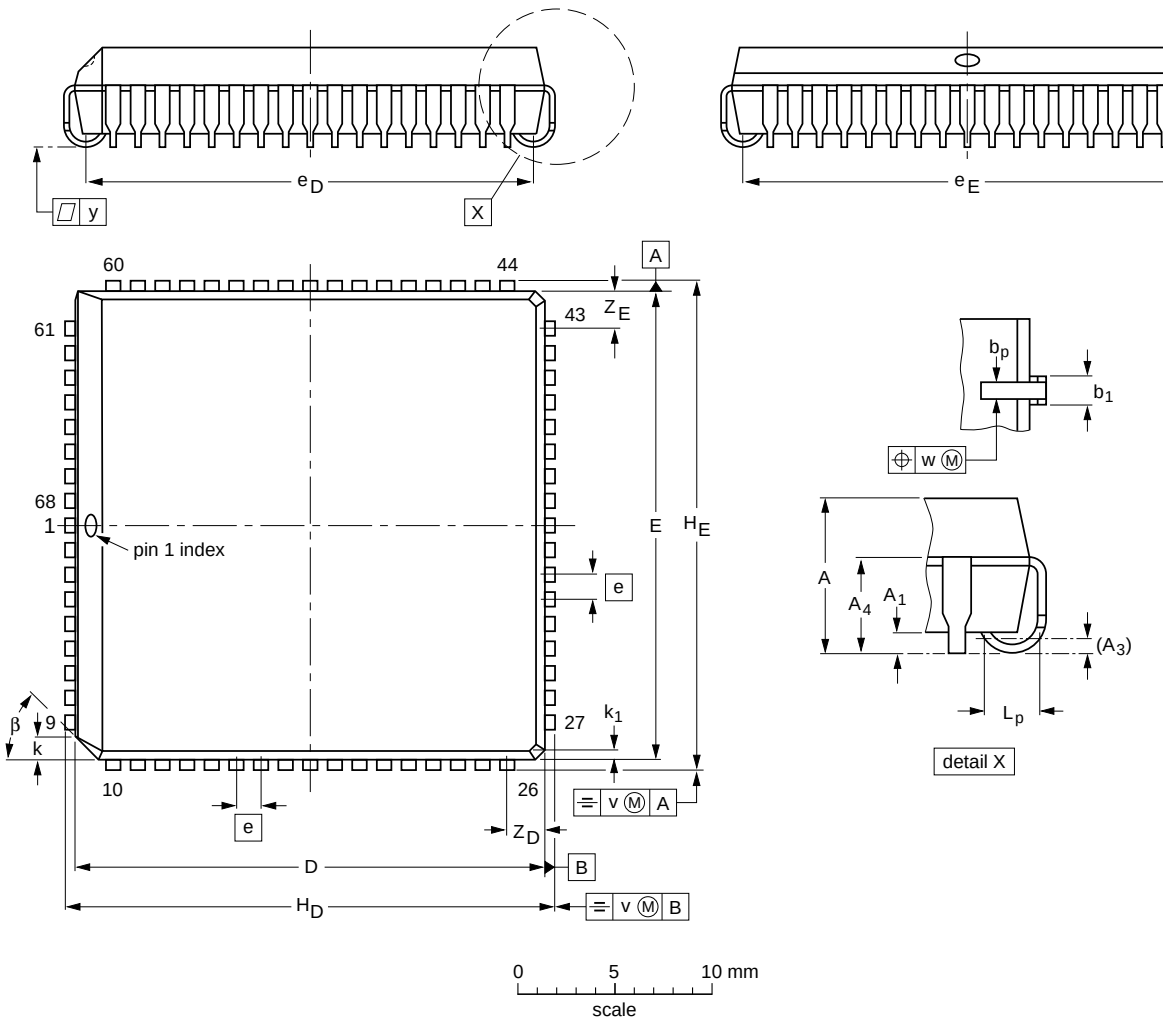
SUBADDRESS	BIT NAME	FUNCTION	VALUE (HEX)
00	IDEL(7-0)	increment delay	4D
01	HSYB(7-0)	horizontal sync HSY begin	3D
02	HSYS(7-0)	horizontal sync HSY stop	0D
03	HCLB(7-0)	horizontal clamping HCL begin	F3
04	HCLS(7-0)	horizontal clamping HCL stop	C6
05	HPHI(7-0)	horizontal sync after PHI1	FB
06	BYPS, PREF, BPSS(1-0) BFBY, CORI, APER(1-0)	luminance bandwidth control:	02 (note 2)
07	HUEC(7-0)	hue control (0 degree)	00
08	CSTD(2-0), CKTQ(4-0)	miscellaneous controls #1	09
09	OSCE, LFIS(1-0), CKTS(4-0)	miscellaneous controls #2	C0
0A	PLSE(7-0)	PAL switch sensitivity	4D
0B	SESE(7-0)	SECAM switch sensitivity	40
0C	FSAU, GPSI(2-1), CGFX, AMPF(3-0)	miscellaneous controls #3	80
0D	COLO, CHSB, GPSW0, SUVI, SXCR, FSDL(2-0)	miscellaneous controls #4	60
0E	CCIR, COEF, OEHS, OEVS UVSS, CHRS, CDMO, CDPO	miscellaneous controls #5	B4
0F	AUFD, FSEL, HPLL, SCEN, VTRC, MUIV, FSIV, WIND	miscellaneous controls #6	9F
10	ASTD, OFTS, IPBP, CDVI, YDEL(3-0)	miscellaneous controls #7	C0
11	CHCV(7-0)	nominal chrominance gain	4F
12	OEDY, OEDC, VNOI(1-0), BFON, BOFL(2-0)	miscellaneous controls #8	C2

Notes

1. Slave address is 8A (hex) at IICSA = LOW or 8E (hex) at IICSA = HIGH.
2. Dependent on applications (Figures 25 to 40).

PACKAGE OUTLINE

PLCC68: plastic leaded chip carrier; 68 leads **SOT188-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-2	112E10	MO-047AC				~~92-11-17~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.