SECTION II — TECHNICAL DATA

GENERAL CHARACTERISTICS AND SPECIFICATIONS

(See pages NO TAG through NO TAG for definitions of symbols and abbreviations.)

In subsequent sections of this Data Book, the important MECL parameters are identified and characterized, and complete data provided for each of the functions. To make this data as useful as possible, and to avoid a great deal of repetition, the data that is common to all functional blocks in a line is not repeated on each individual sheet. Rather, these common characteristics, as well as the application information that applies to each family, are discussed in this section.

In general, the common characteristics of major importance are:

Maximum Ratings, including both dc and ac characteristics and temperature limits;

Transfer Characteristics, which define logic levels and switching thresholds;

DC Parameters, such as output levels, threshold levels, and forcing functions.

AC Parameters, such as propagation delays, rise and fall times and other time dependent characteristics.

In addition, this section will discuss general layout and design guides that will help the designer in building and testing systems with MECL circuits.

LETTER SYMBOLS AND ABBREVIATIONS

Throughout this section, and in the subsequent data sheets, letter symbols and abbreviations will be used in discussing electrical characteristics and specifications. The symbols used in this book, and their definitions, are listed on the preceding pages.

MAXIMUM RATINGS

The limit parameters beyond which the life of the devices may be impaired are given in Table 1. In addition, Table 2 provides certain limits which, if exceeded, will not damage the devices, but could degrade the performance below that of the guaranteed specifications.

Table 1 — LIMITS BEYOND WHICH DEVICE LIFE MAY BE IMPAIRED

Characteristic	Symbol	Unit	MECL 10H	MECL 10K	MECL III
Power Supply	V_{EE}	Vdc	–8.0 to 0	–8.0 to 0	–8.0 to 0
Input Voltage (V_{CC} = 0)	V_{in}	Vdc	0 to V_{EE}	0 to V_{EE}	0 to V_{EE}
Output Source Current Continuous	I_{out}	mAdc	50	50	40
Output Source Current Surge	I_{out}	mAdc	100	100	—
Storage Temperature	T_{stg}	°C	–65 to +150	–65 to +150	–65 to +150
Junction Temperature Ceramic Package①	T_J	°C	165	165	165②
Junction Temperature Plastic Package③	T_J	°C	140	140	140

NOTES: 1. Maximum T_J may be exceeded ($\leq$ 250°C) for short periods of time ($\leq$ 240 hours) without significant reduction in device life.
2. Except MC1670 which has a maximum junction temperature = 145°C.
3. For long term ($\geq$ 10 yrs.) max T_J of 110°C required. Max T_J may be exceeded ($\leq$ 175°C) for short periods of time ($\leq$ 240 hours) without significant reduction in device life.

Table 2 — LIMITS BEYOND WHICH PERFORMANCE MAY BE DEGRADED

Characteristics	Symbol	Unit	MECL 10H	MECL 10K	MECL III
Operating Temperature Range Commercial①	T_A	°C	0 to +75	–30 to +85	–30 to +85
Supply Voltage (V_{CC} = 0)	V_{EE}	Vdc	–4.94 to –5.46	–4.68 to –5.72②⑤	–4.68 to –5.72②
Output Drive Commercial	—	Ω	50 Ω to –2.0 Vdc	50 Ω to –2.0 Vdc	50 Ω to –2.0 Vdc④

NOTES: 1. With airflow $\geq$ 500 lfpm.
2. Functionality only. Data sheet limits are specified for –5.2 V ± 0.010 V.
3. Except MC1648 which has an internal output pulldown resistor.
4. Functional and Data sheet limits.
5. MC10137 has a guaranteed supply voltage of –5.2 V to –5.72 V @ –30°C.

MECL TRANSFER CURVES and SPECIFICATION TEST POINTS

Figure 1 – MECL 10K

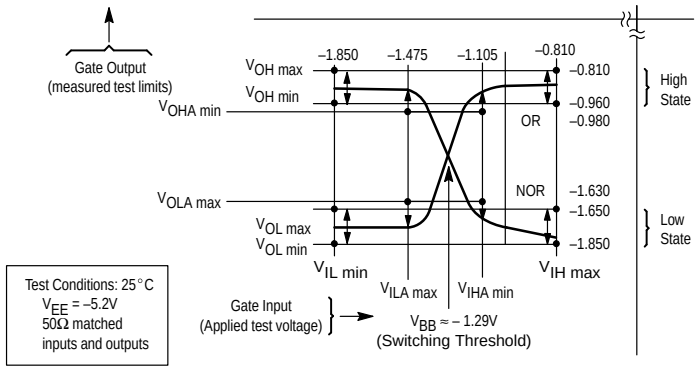
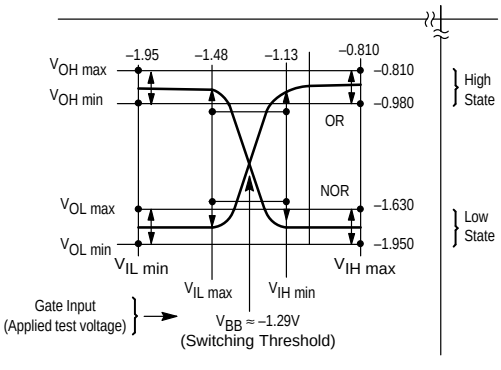


Figure 2 – MECL 10H



MECL TRANSFER CURVES

For MECL logic gates, the dual (complementary) outputs must be represented by two transfer curves: one to describe the OR switching action and one to describe the NOR switching action. Typical transfer curves and associated data for the MECL 10K/10H family are shown in Figure 1 and Figure 2, respectively.

It is not necessary to measure transfer curves at all points of the curves. To guarantee correct operation it is sufficient merely to measure two sets of min/max logic level parameters.

The first set is obtained for 10K by applying test voltages, $V_{IL\ min}$ and $V_{IH\ max}$ (sequentially) to the gate inputs, and measuring the OR and NOR output levels to make sure they are between $V_{OL max}$ and $V_{OL min}$, and $V_{OH max}$ and $V_{OH min}$ specifications.

The second set of logic level parameters relates to the switching thresholds. This set of data is distinguished by an "A" in symbol subscripts. A test voltage, $V_{ILA\ max}$, is applied to the gate and the NOR and OR outputs are measured to see that they are above the $V_{OHA\ min}$ and below the $V_{OLA\ max}$ levels, respectively. Similar checks are made using the test input voltage $V_{IHA\ min}$.

The result of these specifications insures that:

(a) The switching threshold ($\approx V_{BB}$) falls within the darkest rectangle; i.e. switching does not begin outside this rectangle;

(b) Quiescent logic levels fall in the lightest shaded ranges;

(c) Guaranteed noise immunity is met.

As shown in Figure 3, MECL 10K outputs rise with increasing ambient temperature. All circuits in each family have the same worst–case output level specifications regardless of power dissipation or junction temperature differences to reduce loss of noise margin due to thermal differences.

All of these specifications assume –5.2 V power supply operation. Operation at other power–supply voltages is possible, but will result in further transfer curve changes. Table 3 gives rate of change of output voltages as a function of power supply.

Figure 3 — TYPICAL TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE (MECL 10K)

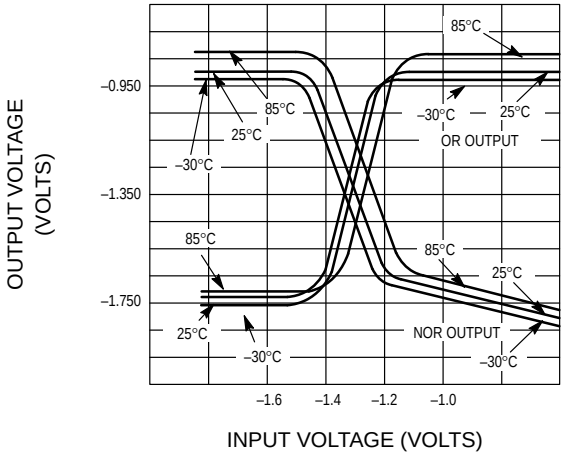


Table 3 — TYPICAL LEVEL CHANGE RATES / 1V

Voltage	MECL 10H	MECL 10K	MECL III
$\Delta V_{OH}/\Delta V_{EE}$	0.008	0.016	0.033
$\Delta V_{OL}/\Delta V_{EE}$	0.020	0.250	0.270
$\Delta V_{BB}/\Delta V_{EE}$	0.010	0.148	0.140

NOISE MARGIN

"Noise margin" is a measure of logic circuit's resistance to undesired switching. MECL noise margin is defined in terms of the specification points surrounding the switching threshold. The critical parameters of interest here are those designated with the "A" subscript ($V_{OHA\ min}$, $V_{OLA\ max}$, $V_{IHA\ min}$, $V_{ILA\ max}$) in the transfer characteristic curves. MECL 10H is specified and tested with:

$$V_{OHA\ min} = V_{OH\ min}$$
$$V_{OLA\ max} = V_{OL\ max}$$
$$V_{IHA\ min} = V_{IH\ min}$$

and

$$V_{ILA\ max} = V_{IL\ max}$$

Guaranteed noise margin (NM) is defined as follows:

$$NM_{HIGH\ LEVEL} = V_{OHA\ min} - V_{IHA\ min}$$
$$NM_{LOW\ LEVEL} = V_{ILA\ max} - V_{OLA\ max}$$

To see how noise margin is computed, assume a MECL gate drives a similar MECL gate, Figure 4.

At a gate input (point B) equal to $V_{ILA\ max}$, MECL gate #2 can begin to enter the shaded transition region.

This is a "worst case" condition, since the $V_{OLA\ max}$ specification point guarantees that no device can enter the transition region before an input equal to $V_{ILA\ max}$ is reached. Clearly then, $V_{ILA\ max}$ is one critical point for noise margin computation, since it is the edge of the transition region.

To find the other critical voltage, consider the output from MECL gate #1 (point A). What is the most positive value possible for this voltage (considering worst case specifications)? From Figure 4 it can be observed that the $V_{OLA\ max}$ specification insures that the LOW state OR output from gate #1 can be no greater than $V_{OLA\ max}$.

Note that $V_{OLA\ max}$ is more negative than $V_{ILA\ max}$. Thus, with $V_{OLA\ max}$ at the input to gate #2, the transition region is not yet reached. (The input voltage to gate #2 is still to the left of $V_{ILA\ max}$ on the transfer curve.)

In order to ever run the chance of switching gate #2, we would need an additional voltage, to move the input from $V_{OLA\ max}$ to $V_{ILA\ max}$. This constitutes the "safety factor" known as noise margin. It can be calculated as the magnitude of the difference between the two specification voltages, or for the MECL 10K levels shown:

NM_{LOW} — $V_{ILA\ max} - V_{OLA\ max}$
— –1.475 V – (–1.630 V)
— 155 mV.

Similarly, for the HIGH state:

NM_{HIGH} — $V_{OHA\ min} - V_{IHA\ min}$
— –0.980 V – (–1.105 V)
— 125 mV

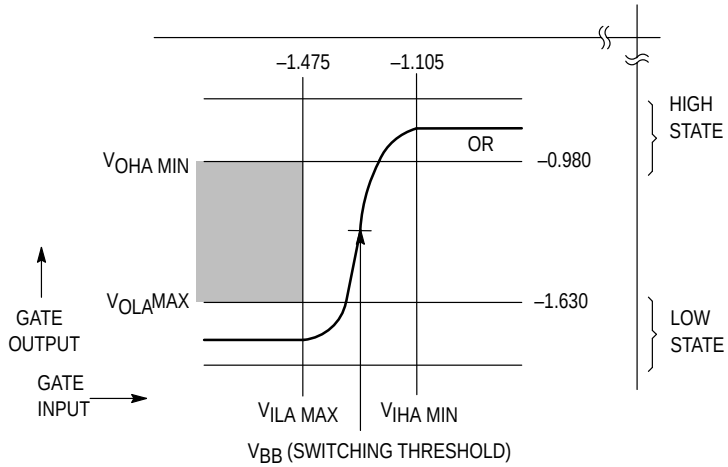
Analogous results are obtained when considering the "NOR" transfer data.

Note that these noise margins are absolute worst case conditions. The lessor of the two noise margins is that for the HIGH state, 125 mV. This then, constitutes the guaranteed margin against signal undershoot, and power or thermal disturbances.

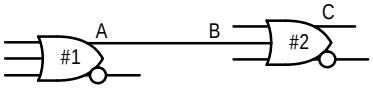
As shown in the table, typical noise margins are usually better than guaranteed — by about 75 mV. For MECL 10H the "noise margin" is 150 mV for NM low and NM high. (See Section 3 for details.)

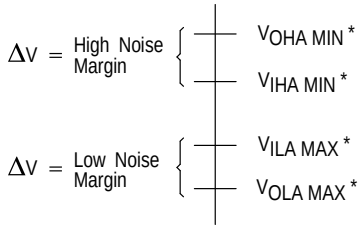
Noise margin is a dc specification that can be calculated, since it is defined by specification points tabulated on MECL data sheets. However, by itself, this specification does not give a complete picture regarding the noise immunity of a system built with a particular set of circuits. Overall system noise immunity involves not only noise–margin specifications, but also other circuit–related factors that determine how difficult it is to apply a noise signal of sufficient magnitude and duration to cause the circuit to propagate a false logic state. In general, then, noise immunity involves line impedances, circuit output impedances, and propagation delay in addition to noise–margin specifications. This subject to discussed in greater detail in the MECL System Design Handbook, HB205.

Figure 4 — MECL Noise Margin Data



Specification Points for Determining Noise Margin





*$V_{OHA\ min} = V_{OH\ min}$, $V_{OLA\ max} = V_{OL\ max}$, $V_{IHA\ min} = V_{IH\ min}$ and $V_{ILA\ max} = V_{IL\ max}$ for MECL 10H.

Noise Margin Computations

Family	Guaranteed Worst–Case dc Noise Margin (V)	Typical dc Noise Margin (V)
MECL 10H	0.150	0.270
MECL 10K	0.125	0.210
MECL III	0.115	0.200

AC OR SWITCHING PARAMETERS

Time–dependent specifications are those that define the effects of the circuit on a specified input signal, as it travels through the circuit. They include the time delay involved in changing the output level from one logic state to another. In addition, they include the time required for the output of a circuit to respond to the input signal, designated as propagation delay, MECL waveform and propagation delay terminologies are depicted in Figure 5. Specific rise, fall, and propagation delay times are given on the data sheet for each specific functional block, but like the transfer characteristics, ac parameters are temperature and voltage dependent. Typical variations for MECL 10K are given in the curves of Figure 6 through Figure 9.

Figure 5 — TYPICAL LOGIC WAVEFORMS

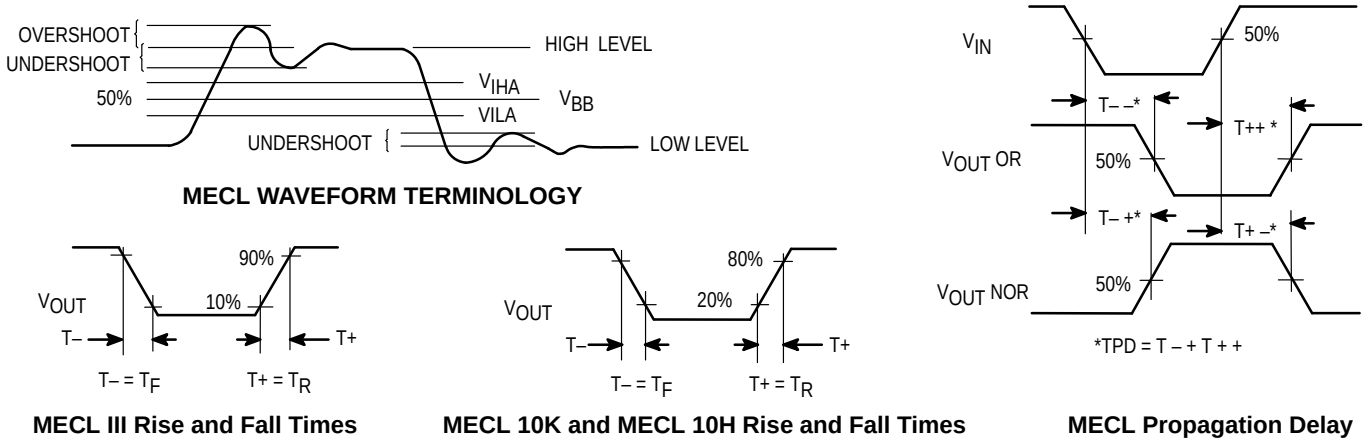


Figure 6 — TYPICAL PROPAGATION DELAY t– – versus V_{EE} AND TEMPERATURE (MECL 10K)

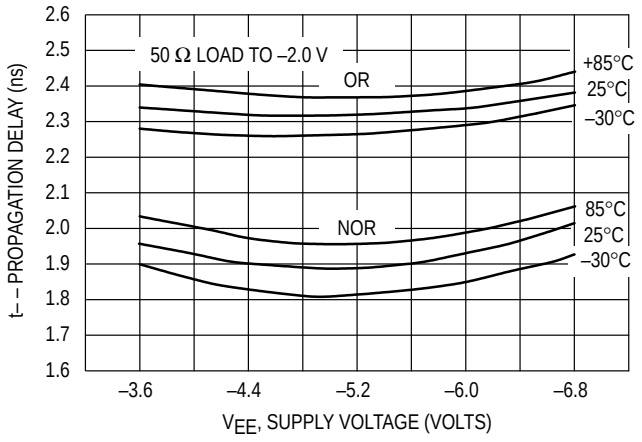


Figure 7 — TYPICAL PROPAGATION DELAY t+ + versus V_{EE} AND TEMPERATURE (MECL 10K)

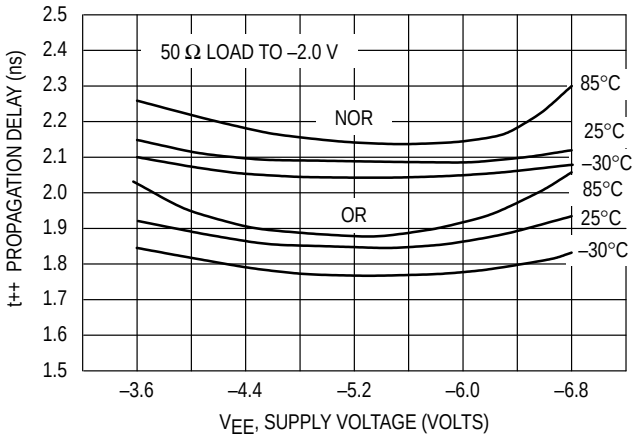


Figure 8 — TYPICAL FALL TIME (90% to 10%) versus TEMPERATURE AND SUPPLY VOLTAGE (MECL 10K)

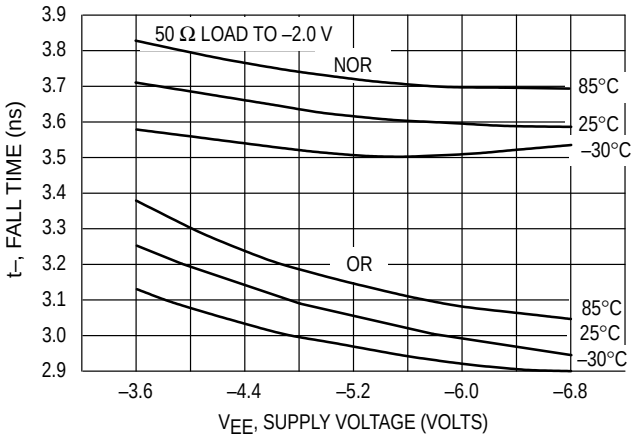
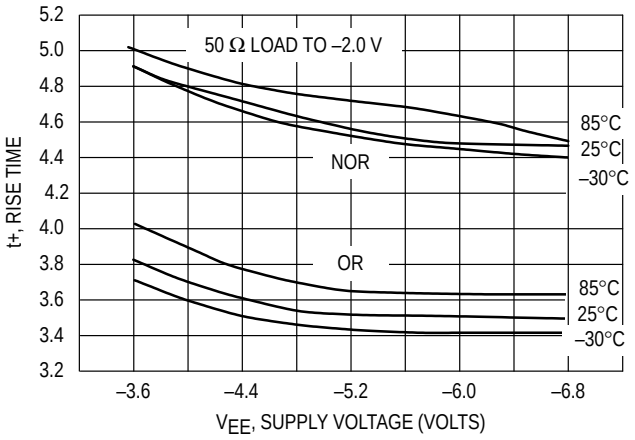


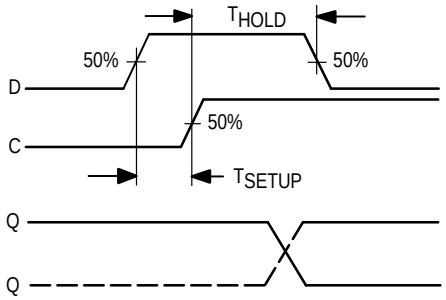
Figure 9 — TYPICAL FALL TIME (10% to 90%) versus TEMPERATURE AND SUPPLY VOLTAGE (MECL 10K)



SETUP AND HOLD TIMES

Setup and hold times are two ac parameters which can easily be confused unless clearly defined. For MECL logic devices, t_{setup} is the minimum time (50% – 50%) before the positive transition of the clock pulse (C) that information must be present at the Data input (D) to insure proper operation of the device. The t_{hold} is defined similarly as the minimum time after the positive transition of the clock pulse (C) that the information must remain unchanged at the Data input (D) to insure proper operation. Setup and hold waveforms for logic devices are shown in Figure 10.

Figure 10 — SETUP AND HOLD WAVEFORMS FOR MECL LOGIC DEVICES



TESTING MECL 10H, MECL 10K AND MECL III

To obtain results correlating with Motorola circuit specifications certain test techniques must be used. A schematic of a typical gate test circuit is shown in Figure 11. This test circuit is the standard ac test configuration for most MECL devices. (Exceptions are shown with device specification.)

A solid ground plane is used in the test setup, and capacitors bypass V_{CC1}, V_{CC2}, and V_{EE} pins to ground. All power leads and signal leads are kept as short as possible.

The sampling scope interface runs directly to the 50–ohm inputs of Channel A and B via 50–ohm coaxial cable. Equal–length coaxial cables must be used between the test set and the A and B scope inputs. A 50–ohm coax cable such as RG58/U or RG188A/U, is recommended.

Interconnect fittings should be 50–ohm GR, BNC, Sealectro Conhex, or equivalent. Wire length should be < ¼ inch from TP_{in} to input pin and TP_{out} to output pin.

The pulse generator must be capable of 2.0 ns rise and fall times for MECL 10K and 1.5 ns for MECL 10H and MECL III. In addition, the generator voltage must have an offset to give MECL signal swings of ≈ ±400 mV about a threshold of ≈ +0.7 V when V_{CC} = +2.0 and V_{EE} = –3.2 V for ac testing of logic devices.

The power supplies are shifted +2.0 V, so that the device under test has only one resistor value to load into the precision 50–ohm input impedance of the sampling oscilloscope. Use of this technique yields a close correlation between Motorola and customer testing. Unused outputs are loaded with a 50–ohm resistor (100–ohm for MC105XX devices) to ground. The positive supply (V_{CC}) should be decoupled from the test board by RF type 25 μF capacitors to ground. The V_{CC} pins are bypassed to ground with 0.1 μF, as is the V_{EE} pin.

Additional information on testing MECL 10K and understanding data sheets is found in Application Note AN701 and the MECL System Design Handbook, HB205.

Figure 11 — MECL LOGIC SWITCHING TIME TEST SETUP