TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA8201AK

BTL AUDIO POWER AMPLIFIER

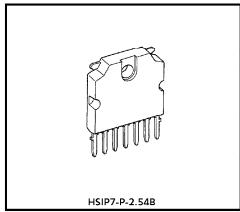
The TA8201AK is audio power amplifier for consumer application.

This IC is applying BTL system in which output coupling condenser and bootstrap condenser are not necessary and output 17W (V_{CC} = 14.4V, B_L = 4Ω , THD = 10%) can be obtained.

Since the package is a 7 pin SIP, (Single Inline Package), it greatly simplifies construction of a power amplifier both in design and assembly.

It also contains various kind of protector.

It is suitable for car-audio power amplifier with high performance.



Weight: 2.19g (Typ.)

FEATURES

High Power: POUT (1) = 17W (Typ.)

 $(V_{CC} = 14.4V, f = 1kHz, THD = 10\%, R_L = 4\Omega)$

: POUT(2) = 14W (Typ.)

 $(V_{CC} = 13.2V, f = 1kHz, THD = 10\%, R_L = 4\Omega)$

- Very Few External Parts
- Built in Protector Circuit
 Thermal Shut Down, Over Voltage Protector (Typ. V_{CC} = 24V)
 ASO Protector (R_L Short, Out to GND, Out to V_{CC})
- 7 pin Small Package
- Operating Supply Voltage Range : V_{CC} = 9~18V

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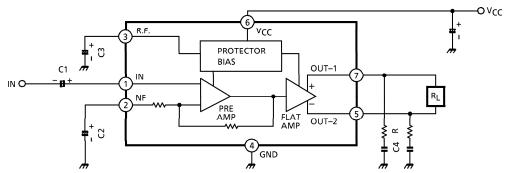
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 The product is often the final stage (the external output stage) of a circuit. Substandard performance or malfunction
- of the destination device to which the circuit supplies output may cause damage to the circuit or to the product.

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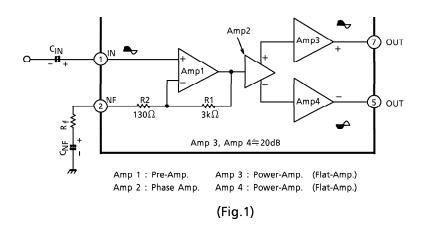
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BLOCK DIAGRAM



DIRECTIONS FOR USE AND APPLICATION METHOD

1. VOLTAGE GAIN ADJUSTMENT



This IC has the amplifier construction as shown in Fig.1. The Pre-Amp. Amp 1 is provided to the primary stage, and the input voltage is amplified by the Flat Amps, Amp 3 and Amp 4 of each channel through the phase Amp. Amp 2.

Since the input offset is prevented by Pre-Amp when V_{CC} is set to ON, this circuit can remarkably reduce the pop noise.

The total closed loop gain G_V of this IC can be obtained by expression below when the closed loop voltage gain of Amp 1 is G_{V1} .

$$G_{V1} = 20 log \frac{R1 + (R_f + R2)}{R_f + R2}$$
 (dB) (1)

The closed loop voltage gain of POWER Amp, Amp 3 and Amp 4 is fixed at $G_{V3} = G_{V4} = 20$ dB. Therefore, the total closed circuit voltage gain G_V is obtained through BTL connection by the expression below.

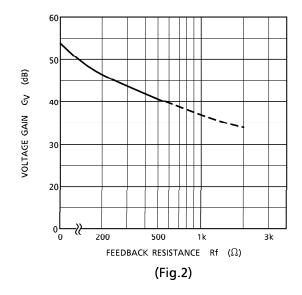
$$G_V = G_{V1} + G_{V3} + 6$$
 (dB)(2)

For example, when $R_f = 0\Omega$, G_V is obtained by the expression below.

$$G_V = 28 + 20 + 6 = 54$$
 (dB)

The voltage gain is reduced when Rf is increased. (Fig.2)

With the voltage gain reduced, since ① the oscillation stability is reduced, and ② the pop noise changes when VCC is set to ON, refer to the items 2 and 4.



2. CAPACITIVE VALUE OF INPUT AND NF CAPACITOR

This IC has the built-in circuit which makes the input voltage of AMP. 1 and the voltage of NF terminal equal at V_{CC}→ON by means of providing the pre-AMP (AMP 1) at the first stage. Therefore, the off-set voltage produced at the first stage is suppressed, and the pop noise is prevented.

Set the capacitive value of input and NF capacitor according to the gain to be used.

[Reference] (A) At $G_V = 54dB$ ($R_f = 0$) $C_{IN} = 4.7 \mu F$, $C_{NF} = 47 \mu F$

(B) At $G_V = 40 dB$ ($R_f = 560 \Omega$) $C_{IN} = 3.3 \mu F$, $C_{NF} = 33 \mu F$

3. CAPACITANCE OF RIPPLE FILTER CAPACITOR

The capacitance of the ripple filter capacitor of ③ pin determines the time constant at V_{CC}→ON and $V_{CC} \rightarrow OFF$.

Since the pop noise varies according to the capacitance of the ripple filter capacitor, C3 = $220 \mu F$ recommended.

Having the built-in rapid discharging circuit of Ripple and NF voltage at the time when V_{CC}→OFF, this IC is effective for preventing the pop noise of V_{CC} continuous ON/OFF.

4. PREVENTIVE MEASURE AGAINST OSCILLATION

For preventing the oscillation, it is advisable to use C4, the condenser of polyester film having small characteristic fluctuation of the temperature and the frequency.

The resistance R to be series applied to C4 is effective for phase correction of high frequency, and improves the oscillation allowance.

Since the oscillation allowance is varied according to the causes described below, perform the temperature test to check the oscillation allowance.

- ① Voltage gain to be used (G_V setting)
- 2 Capacity value condenser
- 3 Kind of condenser
- 4 Layout of printed board

By increasing R_f, decrease of G_V is possible.

However, care must be taken since the feedback increase is liable to produce oscillation.

5. EXTERNAL PART LIST AND DESCRIPTION

	S. EXTENDED TART LIST AND DESCRIPTION								
NAME OF PART	RECOMMENDED VALUE	ОВЈЕСТ	SMALLER THAN RECOMMENDED VALUE	UENCE LARGER THAN RECOMMENDED VALUE	REMARKS				
C1	4 .7μF	DC blocking	Related to popping	noise at V _{CC} →ON	Related to gain.				
		Feedback condenser	Related to popping	Refer to item 2.					
C2	47 μF		Determination of low $C2 = \frac{1}{2\pi f_L \cdot R_f}$						
C3	220 μF	Ripple reduction	Time constant is small at $V_{CC}\rightarrow ON$ or OFF.	Time constant is large at V _{CC} →ON or OFF.	Refer to item 3.				
C4	0.15 <i>μ</i> F	Oscillation prevention	Made liable to oscillate.	Oscillation allowance improved.	Refer to item 4.				
C 5	1000 <i>μ</i> F	Ripple filter	For filtering power s Large at using AC re Small at using DC po						

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Peak Supply Voltage (0.2 sec)	V _{CC} (surge)	50	V
DC Supply Voltage	V _{CC} (DC)	25	V
Operating Supply Voltage	V _{CC} (opr)	18	V
Output Current (Peak)	IO (peak)	4.5	Α
Power Dissipation	PD	15	w
Operating Temperature	T _{opr}	- 30∼85	°C
Storage Temperature	T _{stg}	- 55∼150	°C

ELECTRICAL CHARACTERISTICS

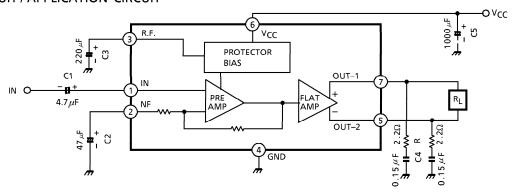
(Unless otherwise specified, V_{CC} = 13.2V, R_L = 4Ω , f = 1kHz, Ta = 25°C)

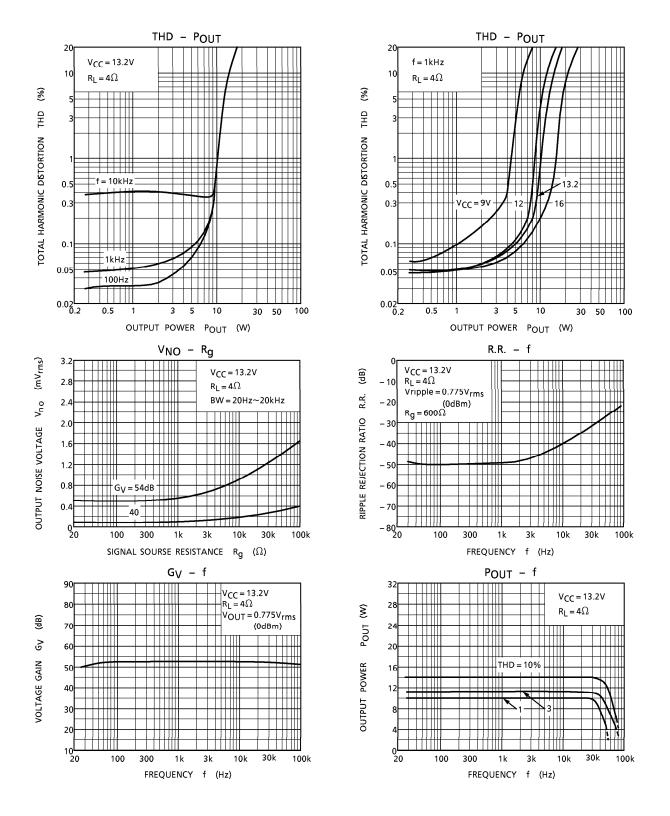
CHARACTERISTIC	SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Quiescent Current	lccQ	_	V _{IN} = 0	_	60	95	mA	
Output Power	POUT (1)	_	V _{CC} = 14.4V, THD = 10%	_	17	_	w	
Output Fower	POUT (2)	—	THD = 10%	10	14	_] **	
Total Harmonic Distortion	THD	_	P _{OUT} = 1W	_	0.05	0.4	%	
Voltage Gain	GV	_	$R_f = 0\Omega$	52	54	56	dB	
Output Noise Voltage	VNO	_	$R_g = 10k\Omega$, BW = 20Hz~20kHz	_	0.9	2.0	mV _{rms}	
Ripple Rejection Ratio	R.R.	—	fripple = 100Hz, $R_g = 600\Omega$	40	50	_	dB	
Input Resistance	R _{IN}	_	f = 1kHz	_	30	_	kΩ	
Output Offset Voltage	Voffset	_	V _{IN} = 0	-0.3	0	0.3	V	

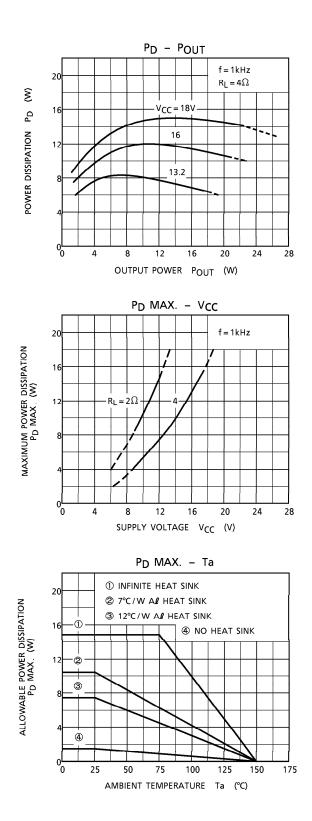
TYPICAL DC VOLTAGE OF EACH TERMINAL ($V_{CC} = 13.2V \setminus V_{IN} = 0V \setminus Ta = 25^{\circ}C$)

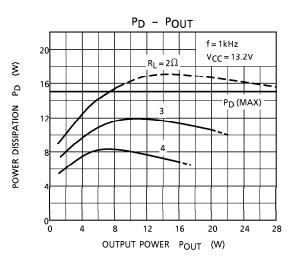
TERMINAL NO	1	2	3			6	7
TERMINAL No.	ı	2	3	4	3	0	,
Terminal	IN	NF	R.F	GND	OUT	VCC	OUT
DC Voltage (V)	4.55	4.55	4.55	0	5.6	13.2	5.6

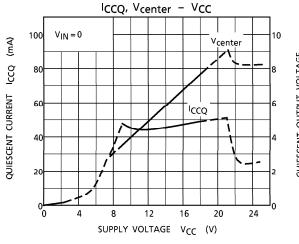
TEST CIRCUIT/APPLICATION CIRCUIT

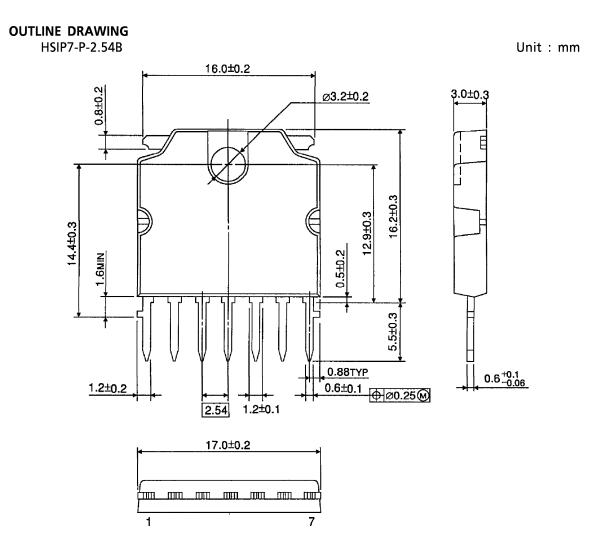












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