SECTION IV — SYSTEM DESIGN CONSIDERATIONS

THERMAL MANAGEMENT

Circuit performance and long–term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit — from the junction region to the ambient environment. The basic formula (a) for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\overline{\theta}_{JC} + \overline{\theta}_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D(\overline{\theta}_{JA}) \quad (2)$$

where

T_J = maximum junction temperature
T_A = maximum ambient temperature
P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation in section III).
$\overline{\theta}_{JC}$ = average thermal resistance, junction to case
$\overline{\theta}_{CA}$ = average thermal resistance, case to ambient
$\overline{\theta}_{JA}$ = average thermal resistance, junction to ambient

This Motorola recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL–M–38510 (JAN) MECL 10K devices.

Only two terms on the right side of equation (1) can be varied by the user — the ambient temperature, and the device case–to–ambient thermal resistance, $\overline{\theta}_{CA}$. (To some extent the device power dissipation can be also controlled, but under recommended use the V_{EE} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\overline{\theta}_{CA}$ thermal resistance term. $\overline{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

Table 1 — THERMAL RESISTANCE VALUES FOR STANDARD MECL I/C PACKAGES

Thermal Resistance in Still Air										
Package Description							θ_{JA} (°C/Watt)		θ_{JC} (°C/Watt)	
No. Leads	Body Style	Body Material	Body WxL	Die Bond	Die Area (Sq. Mils)	Flag Area (Sq. Mils)	Avg.	Max.	Avg.	Max.
8	DIL	EPOXY	1/4″×3/8″	EPOXY	2496	8100	102	133	50	80
8	DIL	ALUMINA	1/4″×3/8″	SILVER/GLASS	2496	N/A	140	182	35	56
14	DIL	EPOXY	1/4″×3/4″	EPOXY	4096	6400	84	109	38	61
14	DIL	ALUMINA	1/4″×3/4″	SILVER/GLASS	4096	N/A	100	130	25	40
16	DIL	EPOXY	1/4″×3/4″	EPOXY	4096	12100	70	91	34	54
16	DIL	ALUMINA	1/4″×3/4″	SILVER/GLASS	4096	N/A	100	130	25	40
20	PLCC	EPOXY	0.35″×0.35″	EPOXY	4096	14,400	74	82	N/A (6)	N/A (6)
24	DIL (4)	EPOXY	1/2″×1–1/4″	EPOXY	8192	22500	67	87	31	50
24	DIL (5)	ALUMINA	1/2″×1–1/4″	SILVER/GLASS	8192	N/A	50	65	10	16
28	PLCC	EPOXY	0.45″×0.45″	EPOXY	7134	28,900	65	68	N/A (6)	N/A (6)

NOTES:
1. All plastic packages use copper lead frames — ceramic packages use alloy 42 frames.
2. Body style DIL is "Dual–In–Line."
3. Standard Mounting Methods:
   a. Dual–In–Line In Socket or P/C board with no contact between bottom of package and socket or P/C board.
   b. PLCC packages solder attached to traces on 2.24″ × 2.24″ × 0.062″ FR4 type glass epoxy board with 1 oz./S.F. copper (solder coated) mounted to tester with 3 leads of 24 gauge copper wire.
4. Case Outline 649
5. Case Outline 623
6. $\theta_{JC} = \theta_{JA} - \left(\frac{T_C - T_A}{P_D}\right)$

T_C = Case Temperature (determined by thermocouple)

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature–controlled heatsink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D (\bar{\theta}_{JC}) \quad (3)$$

where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average thermal resistance values for standard MECL IC packages are given in Table 1. In , this basic data is converted into graphs showing the maximum power dissipation allowable at various ambient temperatures (still air) for circuits mounted in the different packages, taking into account the maximum permissible operating junction temperature for long term life ($\geq$ 100,000 hours for ceramic packages).

AIR FLOW

The effect of air flow over the packages on $\bar{\theta}_{JA}$ (due to a decrease in $\bar{\theta}_{CA}$) is illustrated in the graphs of Figure 1 through Figure 3. This air flow reduces the thermal resistance of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

As an example of the use of the information above, the maximum junction temperature for a 16 lead ceramic dual–in–line packaged MECL 10K quad OR/NOR gate (MC10101L) loaded with four 50 ohm loads can be calculated. Maximum total power dissipation (including 4 output loads) for this quad gate is 195 mW. Assume for this thermal study that air flow is 500 linear feet per minute. From Figure 4, $\bar{\theta}_{JA}$ is 50°C/W. With T_A (air flow temperature at the device) equal to 25°C, the following maximum junction temperature results:

$$T_J = P_D (\bar{\theta}_{JA}) + T_A$$
$$T_J = (0.195\ W)\ (50°C/W) + 25°C = 34.8°C$$

Under the above operating conditions, the MECL 10K quad gate has its junction elevated above ambient temperature by only 9.8°C.

Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperatures as the air passes over the devices, or differences in ambient temperature between two devices.

Figure 1 —AMBIENT TEMPERATURE DERATING CURVES (CERAMIC DUAL–IN–LINE PACKAGE)

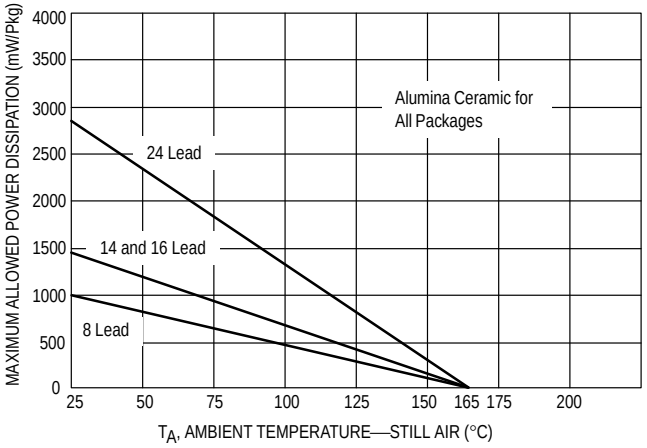


Figure 2 —AMBIENT TEMPERATURE DERATING CURVES (PLASTIC DUAL–IN–LINE PACKAGE)

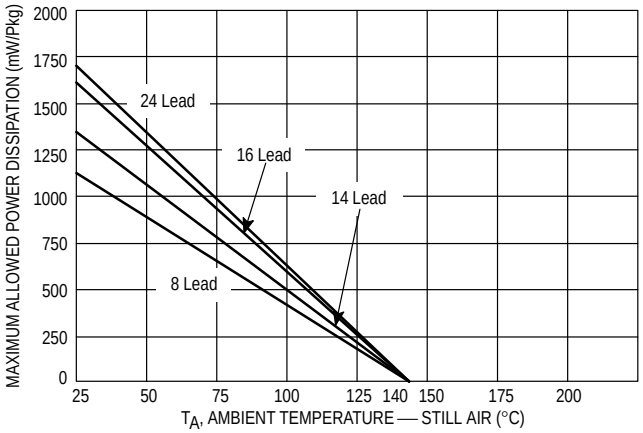


Figure 3 — AMBIENT TEMPERATURE DERATING CURVES (PLCC PACKAGE)

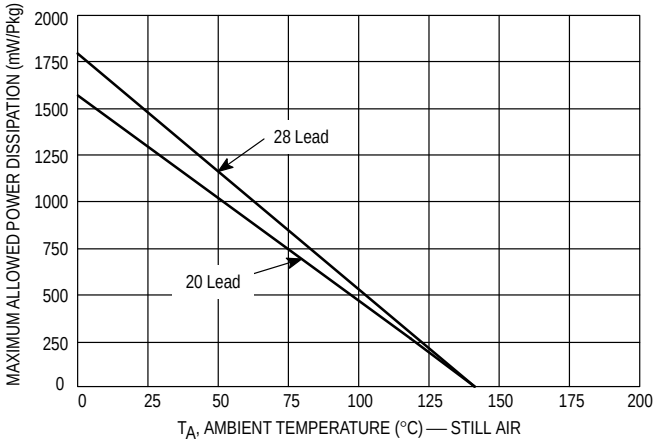


Figure 4 — AIRFLOW versus THERMAL RESISTANCE (CERAMIC DUAL–IN–LINE PACKAGE)

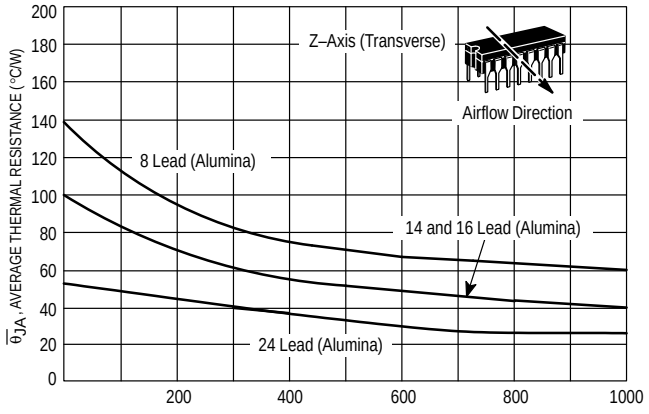


Figure 5 — AIRFLOW versus THERMAL RESISTANCE (PLASTIC DUAL–IN–LINE PACKAGE)

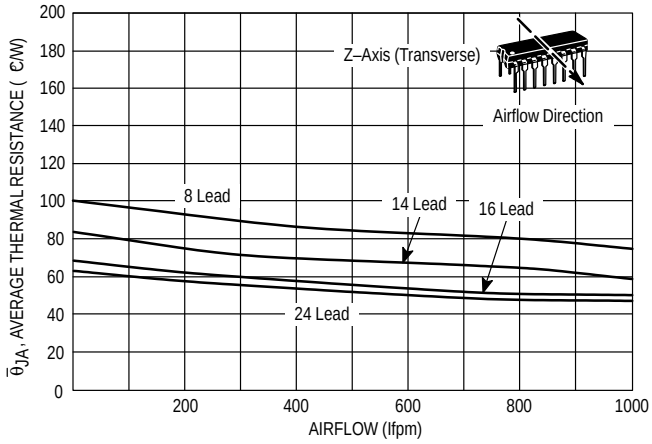


Figure 6 — AIRFLOW versus THERMAL RESISTANCE (PLCC PACKAGE)

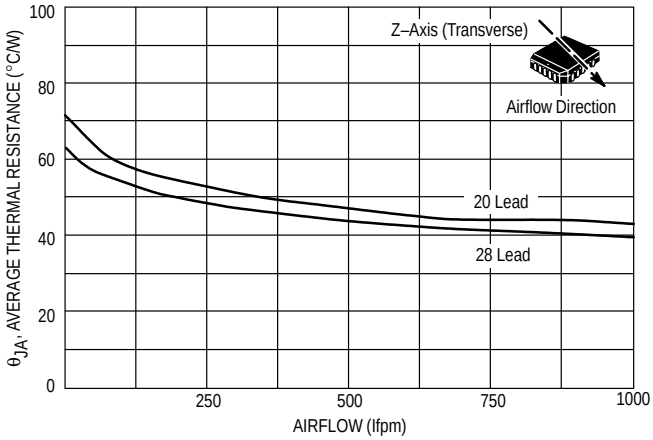


Table 2 — THERMAL GRADIENT OF JUNCTION TEMPERATURE (16–Pin MECL Dual–In–Line Package)

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062″ PC board with Z axis spacing 0.5″. Air flow is 500 lfpm along the Z axis.

The majority of MECL 10H, MECL 10K, and MECL III users employ some form of air–flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipations. Table 2 provides gradient data at power levels of 200 mW, 250 mW, 300 mW, and 400 mW with an air flow rate of 500 lfpm. These figures show the proportionate increase in the junction temperature of each dual–in–line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

OPTIMIZING THE LONG TERM RELIABILITY OF PLASTIC PACKAGES

Todays plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However when the ultimate in system reliability is required, thermal management must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperatures are consistent with system reliability goals.

Predicting Bond Failure Time:

Based on the results of almost ten (10) years of +125°C operating life testing, a special arrhenius equation has been developed to show the relationship between junction temperature and reliability.

$$(1)\ T = (6.376 \times 10^{-9})e\left[\frac{11554.267}{273.15 + T_J}\right]$$

Where: T = Time in hours to 0.1% bond failure (1 failure per 1,000 bonds).
T_J = Device junction temperature, °C.

And:

$$(2)\ T_J = T_A + P_D\theta J_A = T_A + \Delta T_J$$

Where: T_J = Device junction temperature, °C.
T_A = Ambient temperature, °C.
P_D = Device power dissipation in watts.
θJ_A = Device thermal resistance, junction to air, °C/Watt.
ΔT_J = Increase in junction temperature due to on–chip power dissipation.

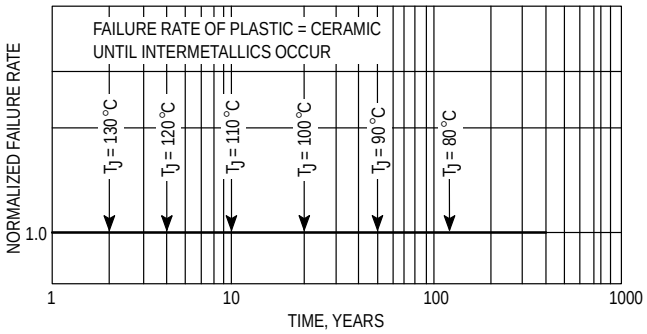
Table 3 shows the relationship between junction temperature, and continuous operating time to 0.1% bond failure, (1 failure per 1,000 bonds).

Table 3 — DEVICE JUNCTION TEMPERATURE versus TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Table 3 is graphically illustrated in Figure 7 which shows that the reliability for plastic and ceramic devices are the same until elevated junction temperatures induces intermetallic failures in plastic devices. Early and mid–life failure rates of plastic devices are not effected by this intermetallic mechanism.

Figure 7. FAILURE RATE versus TIME JUNCTION TEMPERATURE



MECL Junction Temperatures:

Power levels have been calculated for a number of MECL 10K and MECL 10H devices in 20 pin plastic leaded chip carriers and translated to the resulting increase of junction temperature (ΔT_J) for still air and moving air at 500 LFPM using equation 2 and are shown in Table 4.

Table 4 — INCREASE IN JUNCTION TEMPERATURE DUE TO I/C POWER DISSIPATION. 20 PIN PLASTIC LEADED CHIP CARRIER

MECL 10K Device Type	ΔT_J, °C Still Air	ΔT_J, °C 500 LFPM Air	MECL 10H Device Type	ΔT_J, °C Still Air	ΔT_J, °C 500 LFPM Air
MC10101	21.8	14.1	MC10H016	48.0	30.0
MC10102	17.6	11.4	MC10H100	16.6	10.8
MC10103	17.6	11.4	MC10H101	22.1	14.5
MC10104	20.8	13.4	MC10H102	18.0	11.8
MC10105	17.2	11.2	MC10H103	18.0	11.8
MC10106	13.0	8.4	MC10H104	21.0	13.5
MC10107	19.8	12.8	MC10H105	17.8	11.7
MC10109	11.7	7.7	MC10H106	13.2	8.7
MC10110	24.7	16.1	MC10H107	20.0	12.9
MC10111	24.7	16.1	MC10H109	11.9	7.8
MC10113	22.2	14.3	MC10H113	22.8	14.8
MC10114	22.6	14.6	MC10H115	16.7	10.9
MC10115	16.7	10.9	MC10H116	17.8	11.7
MC10116	17.2	11.1	MC10H117	16.7	11.0
MC10117	16.2	10.5	MC10H121	13.9	9.1
MC10121	13.5	8.5	MC10H123	23.1	15.0
MC10123	37.6	24.0	MC10H124	44.2	28.4
MC10124	42.9	27.3	MC10H125	—	—
MC10125	—	—	MC10H130	28.2	18.2
MC10131	26.9	17.1	MC10H135	33.2	21.4
MC10133	34.4	21.9	MC10H136	61.7	38.5
MC10134	27.0	17.2	MC10H141	44.3	28.0
MC10135	31.9	20.3	MC10H145	59.4	36.9
MC10136	52.3	32.6	MC10H158	25.3	16.4
MC10138	37.0	23.2	MC10H159	27.3	17.7
MC10141	42.7	26.7	MC10H160	32.1	20.5
MC10153	34.4	21.9	MC10H161	41.5	26.7
MC10158	23.9	15.2	MC10H162	41.5	26.7
MC10159	25.8	16.4	MC10H164	31.9	20.6
MC10160	32.0	20.4	MC10H165	56.3	35.8
MC10161	40.7	26.0	MC10H166	44.4	28.3
MC10162	40.7	26.0	MC10H171	41.9	26.9
MC10164	31.3	20.1	MC10H172	41.9	26.9
MC10165	53.7	33.6	MC10H173	32.6	21.1
MC10166	43.5	27.6	MC10H174	32.5	21.0
MC10168	34.4	21.9	MC10H175	45.9	29.6
MC10170	29.9	18.9	MC10H176	50.9	32.3
MC10171	41.1	26.2	MC10H179	35.0	22.6
MC10172	41.1	26.2	MC10H180	42.4	27.2
MC10173	30.5	19.3	MC10H181[4]	64.4	38.6
MC10174	31.9	20.5	MC10H186	50.2	31.8
MC10175	43.7	27.6	MC10H188	25.8	16.7
MC10176	49.6	31.3	MC10H189	25.8	16.7
MC10178	38.1	23.9	MC10H209	18.9	12.5
MC10186	49.6	31.1	MC10H210	25.0	16.4
MC10188	25.4	16.4	MC10H211	25.0	16.4
MC10189	24.6	15.9	MC10H330[4]	65.8	36.1
MC10192	67.0	43.0	MC10H332	52.2	33.5
MC10195	46.7	29.9	MC10H334	77.8	49.3
MC10197	27.7	17.7	MC10H350	—	—
MC10198	21.2	13.4	MC10H351	27.2	18.1
MC10210	24.5	16.0	MC10H352	27.2	18.1
MC10211	24.6	16.0	MC10H424	37.7	24.3
MC10212	24.3	15.8			
MC10216	24.1	15.6			
MC10231	30.6	19.5			

NOTES:
(1) All ECL outputs are loaded with a 50 Ω resistor and assumed operating at 50% duty cycle.
(2) ΔT_J for ECL to TTL translators are excluded since the supply current to the TTL section is dependent on frequency, duty cycle and loading.
(3) Thermal Resistance (θ_{JA}) measured with PLCC packages solder attached to traces on 2.24″ x 2.24″ x 0.062″ FR4 type glass epoxy board with 1 oz./sq. ft. copper (solder–coated) mounted to tester with 3 leads of 24 gauge copper wire.
(4) 28 lead PLCC.

Case Example:

After the desired system failure rate has been established for failure mechanisms other than intermetallics, each plastic device in the system should be evaluated for maximum junction temperature using Table 4. Knowing the maximum junction temperature refer to Table 3 or Equation 1 to determine the continuous operating time required to 0.1% bond failures due to intermetallic formation. At this time, system reliability departs from the desired value as indicated in Figure 7.

To illustrate, assume that system ambient air temperature is 55°C (an accepted industry standard for evaluating system failure rates). Reference is made to Table 4 to determine the maximum junction temperature for each device for still air and transverse air flow of 500 LFPM.

Adding the 55°C ambient to the highest, ΔT_J listed, 77.8°C (for the MC10H334 with no air flow), gives a maximum junction temperature of 132.8°C. Reference to Table 3 indicates a departure from the desired failure rate after about 2 years of constant exposure to this junction temperature. If 500 LFPM of air flow is utilized, maximum junction temperature for this device is reduced to 104.3°C for which Table 3 indicates an increased failure rate in about 15 years.

Air flow is one method of thermal management which should be considered for system longevity. Other commonly used methods include heat sinks for higher powered devices, refrigerated air flow and lower density board stuffing.

The material presented here emphasizes the need to consider thermal management as an integral part of system design and also the tools to determine if the management methods being considered are adequate to produce the desired system reliability.

THERMAL EFFECTS ON NOISE MARGIN

The data sheet dc specifications for standard MECL 10K and MECL III devices are given for an operating temperature range from –30°C to +85°C (0° to +75°C for MECL 10H and memories). These values are based on having an airflow of 500 lfpm over socket or P/C board mounted packages with no special heatsinking (i.e., dual–in–line package mounted on lead seating plane with no contact between bottom of package and socket or P/C board and flat package mounted with bottom in direct contact with non–metalized area of P/C board).

The designer may want to use MECL devices under conditions other than those given above. The majority of the low–power device types may be used without air and with higher $\overline{\theta}_{JA}$. However, the designer must bear in mind that junction temperatures will be higher for higher $\overline{\theta}_{JA}$, even though the ambient temperature is the same. Higher junction temperatures will cause logic levels to shift.

As an example, a 300 mW 16 lead dual–in–line ceramic device operated at $\overline{\theta}_{JA}$ = 100°C/W (in still air) shows a HIGH logic level shift of about 21 mV above the HIGH logic level when operated with 500 lfpm air flow and a $\overline{\theta}_{JA}$ = 50°C/W. (Level shift = $\Delta T_J \times 1.4$ mV/°C).

If logic levels of individual devices shift by different amounts (depending on P_D and θ_{JA}), noise margins are somewhat reduced. Therefore, the system designer must lay out his system bearing in mind that the mounting procedures to be used should minimize thermal effects on noise margin.

The following sections on package mounting and heatsinking are intended to provide the designer with sufficient information to insure good noise margins and high reliability in MECL system use.

MOUNTING AND HEATSINK SUGGESTIONS

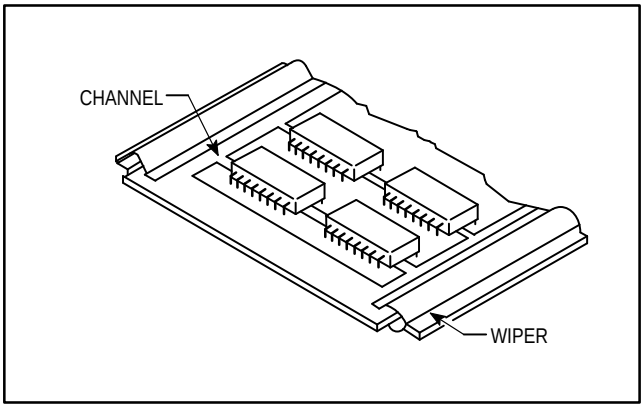
With large high–speed logic systems, the use of multilayer printed circuit boards is recommended to provide both a better ground plane and a good thermal path for heat dissipation. Also, a multilayer board allows the use of microstrip line techniques to provide transmission line interconnections.

Two–sided printed circuit boards may be used where board dimensions and package count are small. If possible, the V_{CC} ground plane should face the bottom of the package to form the thermal conduction plane. If signal lines must be placed on both sides of the board, the V_{EE} plane may be used as the thermal plane, and at the same time may be used as a pseudo ground plane. The pseudo ground plane becomes the ac ground reference under the signal lines placed on the same side as the V_{CC} ground plane (now on the opposite side of the board from the packages), thus maintaining a microstrip signal line environment.

Two–ounce copper P/C board is recommended for thermal conduction and mechanical strength. Also, mounting holes for low power devices may be countersunk to allow the package bottom to contact the heat plane. This technique used along with thermal paste will provide good thermal conduction.

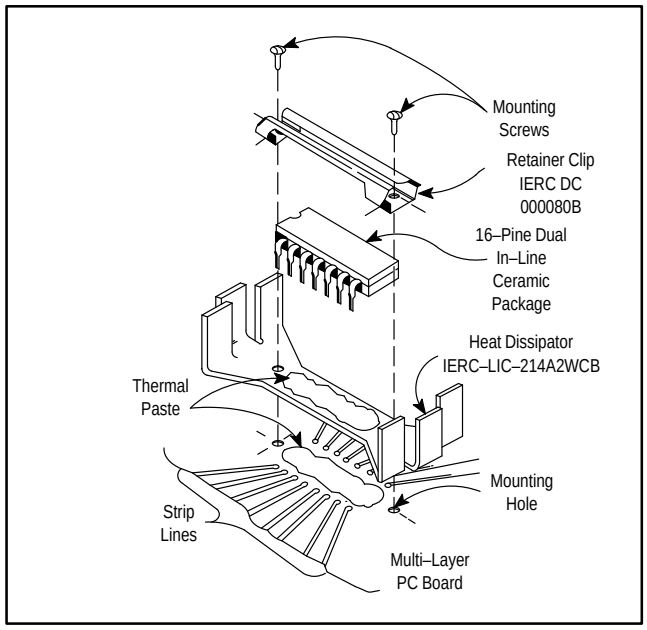
Printed channeling is a useful technique for conduction of heat away from the packages when the devices are soldered into a printed circuit board. As illustrated in Figure 8, this heat dissipation method could also serve as V_{EE} voltage distribution or as a ground bus. The channels should terminate into channel strips at each side or the rear of a plug–in type printed circuit board. The heat can then be removed from the circuit board, or board slide rack, by means of wipers that come into thermal contact with the edge channels.

Figure 8 — CHANNEL/WIPER HEATSINKING ON DOUBLE LAYER BOARD



For operating some of the higher power device types* in 16 lead dual–in–line packages in still air, requiring $\overline{\theta}_{JA}$ <100°C/W, a suitable heatsink is the IERC LIC–214A2WCB shown in Figure 9. This sink reduces the still air $\overline{\theta}_{JA}$ to around 55°C/W. By mounting this heatsink directly on a copper ground plane (using silicone paste) and passing 500 lfpm air over the packages, $\overline{\theta}_{JA}$ is reduced to approximately 35°C/W, permitting use at higher ambient temperatures than +85°C (+75°C for MECL 10H memories) or in lowering T_J for improved reliability.

Figure 9 — MECL HIGH–POWER DUAL–IN–LINE PACKAGE MOUNTING METHOD



It should be noted that the use of a heatsink on the top surface of the dual–in–line package is not very effective in lowering the $\overline{\theta}_{JA}$. This is due to the location of the die near the bottom surface of the package. Also, very little (< 10%) of the internal heat is withdrawn through the package leads due to the isolation from the ceramic by the solder glass seals and the limited heat conduction from the die through 1.0 to 1.5 mil aluminum bonding wires.

INTERFACING MECL TO SLOWER LOGIC TYPES

MECL circuits are interfaceable with most other logic forms. For MECL/TTL/DTL interfaces, when MECL is operated at the recommended –5.2 volts and TTL/DTL at +5.0 V supply, currently available translator circuits, such as the MC10124 and MC10125, may be used.

For systems where a dual supply (–5.2 V and +5 V) is not practical, the MC10H350 includes four single supply MECL to TTL translators, or a discrete component translator can be designed. For details, see MECL System Design Handbook (HB205). Such circuits can easily be made fast enough for any available TTL.

MECL also interfaces readily with MOS. With CMOS operating at +5 V, any of the MECL to TTL translators works very well.

Specific circuitry for use in interfacing MECL families to other logic types is given in detail in the MECL System Design Handbook.

Complex MECL 10K devices are presently available for interfacing MECL with MOS logic, MOS memories, TTL three–state circuits, and IBM bus logic levels. See Application Note AN–720 for additional interfacing information.

CIRCUIT INTERCONNECTIONS

Though not necessarily essential, the use of multilayer printed circuit boards offers a number of advantages in the development of high–speed logic cards. Not only do multilayer boards achieve a much higher package density, interconnecting leads are kept shorter, thus minimizing propagation delay between packages. This is particularly beneficial with MECL III which has relatively fast (1 ns) rise and fall times. Moreover, the unbroken ground planes made possible with multilayer boards permit much more precise control of transmission line impedances when these are used for interconnecting purposes. Thus multilayer boards are recommended for MECL III layouts and are justified when operating MECL 10H and MECL 10K at top circuit speed, when high–density package is a requirement, or when transmission line interconnects are used.

Point–to–point back–plane wiring without matched line terminations may be employed for MECL interconnections if line runs are kept short. At MECL 10K speeds, this applies to line runs up to 6 inches, for MECL 10H and MECL III up to 1 inch (Maximum open wire lengths for less than 100 mV undershoot). But, because of the open–emitter outputs of MECL 10H, MECL 10K and MECL III circuits, pull–down resistors are always required. Several ways of connecting such pull–down resistors are shown in Figure 10 through Figure 12.

Resistor values for the connection in Figure 10 may range from 270 ohms to kΩ depending on power and load requirements. (See MECL System Design Handbook.) Power may be saved by connecting pull–down resistors in the range of 50 ohms to 150 ohms, to –2.0 Vdc, as shown in Figure 11. Use of a series damping resistor, Figure 12, will extend permissible lengths of unmatched–impedance interconnec–tions, with some loss of edge speed.

With proper choice of the series damping resistor, line lengths can be extended to any length,** while limiting overshoot and undershoot to a predetermined amount. Damping resistors usually range in value from 10 ohms to 100 ohms, depending on the line length, fanout, and line impedance, the open emitter–follower outputs of MECL 10H, MECL III and MECL 10K give the system designer all possible line driving options.

One major advantage of MECL over saturated logic is its capability for driving matched–impedance transmission lines. Use of transmission lines retains signal integrity over long distances. The MECL 10H and MECL 10K emitter–follower output transistors will drive a 50–ohm transmission line terminated to –2.0 Vdc. This is the equivalent current load of 22 mA in the HIGH logic state and 6 mA in the LOW state.

* 10129, 10136, 10H136, and 10137, Max P_D > 800 mW.

** Limited only by line attenuation and band–width characteristics.

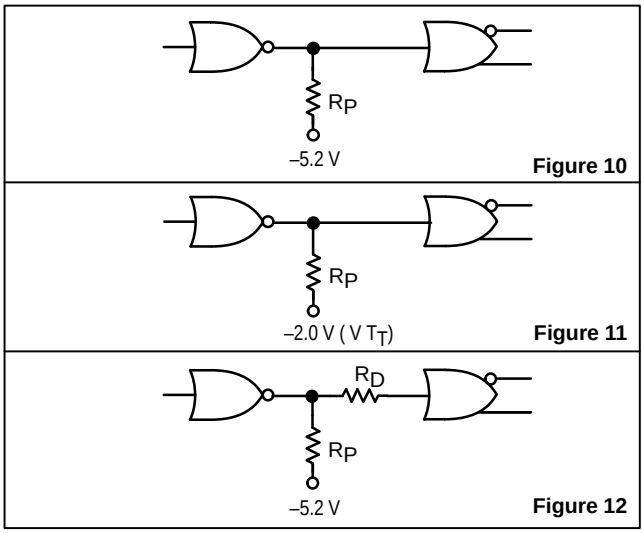
Parallel termination of transmission lines can be done in two ways. One, as shown in Figure 13, uses a single resistor whose value is equal to the impedance (Z_0) of the line. A terminating voltage (V_{TT}) of –2.0 Vdc must be supplied to the terminating resistor.

Another method of parallel termination uses a pair of resistors, R1 and R2. Figure 14 illustrates this method. The following two equations are used to calculate the values of R1 and R2:

$$R1 = 1.6\ Z_0$$
$$R2 = 2.6\ Z_0$$

Another popular approach is the series–terminated transmission line (see Figure 13 and Figure 14). This differs from parallel termination in that only one–half the logic swing is propagated through the lines. The logic swing doubles at the end of the transmission line due to reflection on an open line, again establishing a full logic swing.

PULL–DOWN RESISTOR TECHNIQUES



To maintain clean wave fronts, the input impedance of the driven gate must be much greater than the characteristic impedance of the transmission line. This condition is satisfied by MECL circuits which have high impedance inputs. Using the appropriate terminating resistor (R_S) at point A (Figure 15), the reflections in the transmission line will be terminated.

Figure 13 — PARALLEL TERMINATED LINE

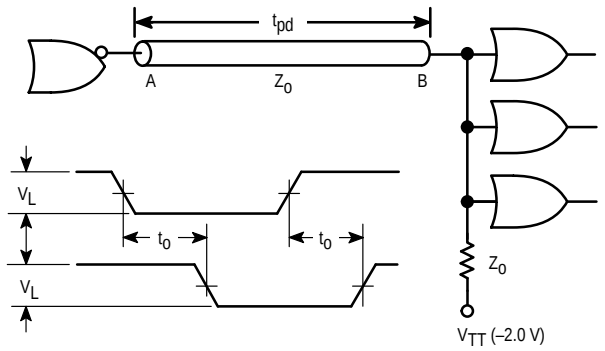


Figure 14 — PARALLEL TERMINATION — THEVENIN EQUIVALENT

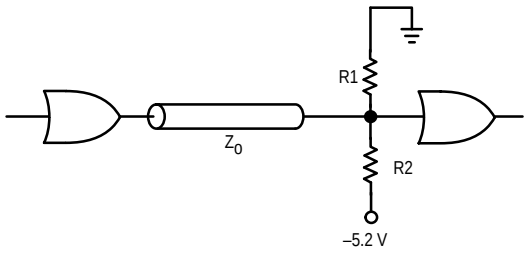
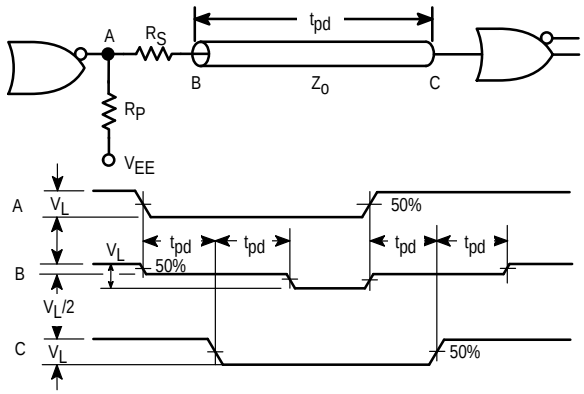


Figure 15 — SERIES TERMINATED LINE



The advantages of series termination include ease of driving multiple series–terminated lines, low power consumption, and low cross talk between adjacent lines. The disadvantage of this system is that loads may not be distributed along the transmission line due to the one–half logic swing present at intermediate points.

For board–to–board interconnections, coaxial cable may be used for signal conductors. The termination techniques just discussed also apply when using coax. Coaxial cable has the advantages of good noise immunity and low attenuation at high frequencies.

Twisted pair lines are one of the most popular methods of interconnecting cards or panels. The complementary outputs of any MECL function may be connected to one end of the twisted pair line, and any MECL differential line receiver to the other as shown in the example, Figure 16. R_T is used to terminate the twisted pair line. The 1 to 1.5 V common–mode noise rejection of the line receiver ignores common–mode cross talk, permitting multiple twisted pair lines to be tied into cables. MECL signals may be sent very long distances (> 1000 feet) on twisted pair, although line attenuation will limit bandwidth, degrading edge speeds when long line runs are made.

If timing is critical, parallel signals paths (shown in Figure 17) should be used when fanout to several cards is required. This will eliminate distortion caused by long stub lengths off a signal path.

Wire–wrapped connections can be used with MECL 10K. For MECL III and MECL 10H, the fast edge speeds (1 ns) create a mismatch at the wire–wrap connections which can cause reflections, thus reducing noise immunity. The mismatch occurs also with MECL 10K, but the distance

between the wire–wrap connections and the end of the line is generally short enough so the reflections cause no problem.

Series damping resistors may be used with wire–wrapped lines to extend permissible backplane wiring lengths. Twisted pair lines may be used for even longer distances across large wire–wrapped cards. The twisted pair gives a more defined characteristic impedance (than a single wire), and can be connected either single–ended, or differentially using a line receiver.

The recommended wire–wrapped circuit cards have a ground plane on one side and a voltage plane on the other side to insure a good ground and a stable voltage source for the circuits. In addition, the ground plane near the wire–wrapped lines lowers the impedance of those lines and facilitates terminating the line. Finally, the ground plane serves to minimize cross talk between parallel paths in the signal lines. Point–to–point wire routing is recommended because cross talk will be minimized and line lengths will be shortest. Commercial wire–wrap boards designed for MECL 10K are available from several vendors.

Figure 16 — TWISTED PAIR LINE DRIVER/RECEIVER

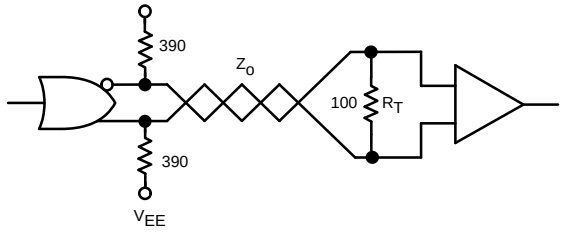
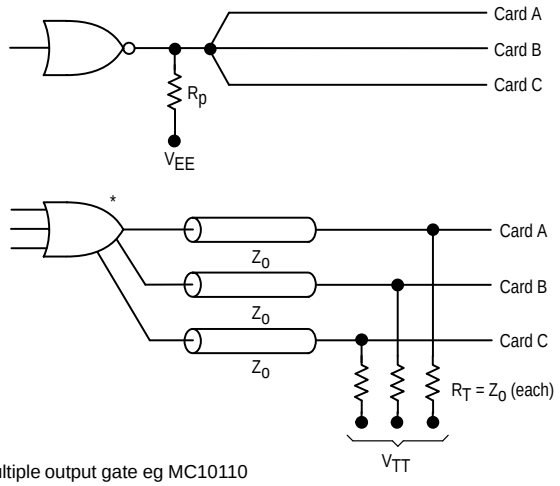


Figure 17 — PARALLEL FANOUT TECHNIQUES

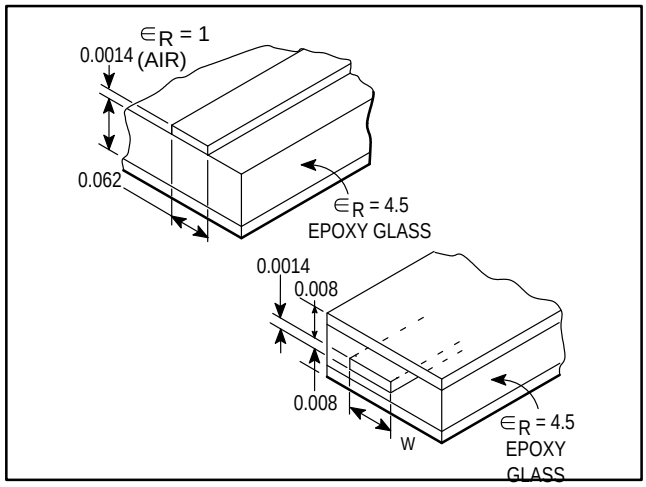


*Multiple output gate eg MC10110

Microstrip and Stripline

Microstrip and stripline techniques are used with printed circuit boards to form transmission lines. Microstrip consists of a constant–width conductor on one side of a circuit board, with a ground plane on the other side (shown in Figure 18). The characteristic impedance is determined by the width and thickness of the conductor, the thickness of the circuit board, and the dielectric constant of the circuit board material.

Figure 18 — PC INTERCONNECTION LINES FOR USE WITH MECL



Stripline is used with multilayer circuit boards as shown in Figure 18. Stripline consists of a constant–width conductor between two ground planes.

Refer to MECL System Design Handbook for a full discussion of the properties and use of these.

CLOCK DISTRIBUTION

Clock distribution can be a system problem. At MECL 10K speeds, either coaxial cable or twisted pair line (using the MC10101 and MC10115) can be used to distribute clock signals throughout a system. Clock line lengths should be controlled and matched when timing could be critical. Once the clocking signals arrive on card, a tree distribution should be used for large–fanouts at high frequency. An example of the application of the technique is shown in Figure 19.

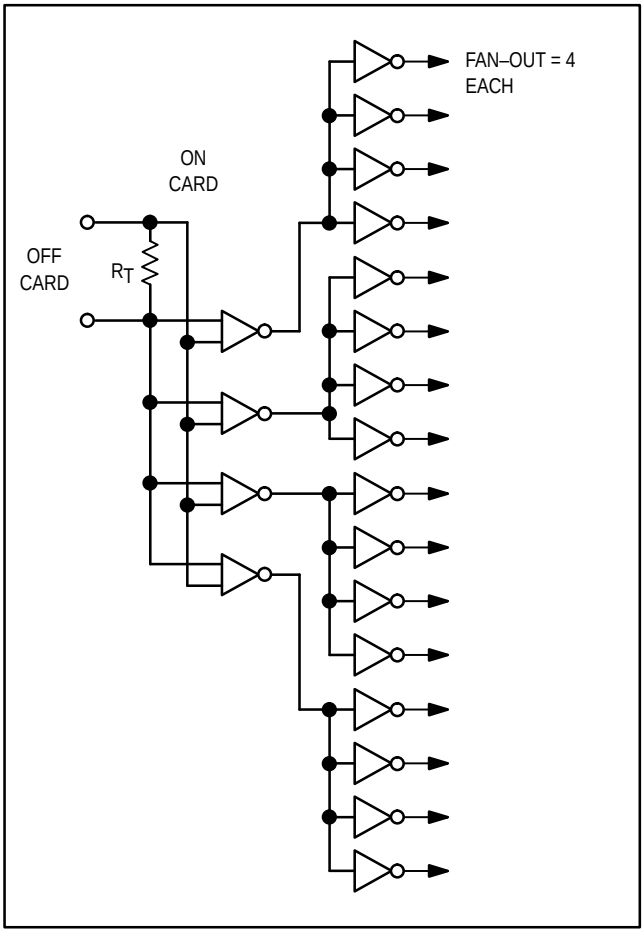
Because of the very high clock rates encountered in MECL III systems, rules for clocking are more rigorous than in slower systems.

The following guidelines should be followed for best results:

A. On–card Synchronous Clock Distribution via Transmission Line

1. Use the NOR output in developing clock chains or trees. Do not mix OR and NOR outputs in the chain.
2. Use balanced fanouts on the clock drivers.
3. Overshoot can be reduced by using two parallel drive lines in place of one drive line with twice the lumped load.

Figure 19 — 64 FANOUT CLOCK DISTRIBUTION (PROPER TERMINATION REQUIRED)



4. To minimize clock skewing problems on synchronous sections of the system, line delays should be matched to within 1 ns.

5. Parallel drive gates should be used when clocking repetition rates are high, or when high capacitance loads occur. The bandwidth of a MECL III gate may be extended by paralleling both halves of a dual gate. Approximately 40 or 50 MHz bandwidth can be gained by paralleling two or three clock driver gates.

6. Fanout limits should be applied to clock distribution drivers. Four to six loads should be the maximum load per driver for best high speed performance. Avoid large lumped loads at the end of lines greater than 3 inches. A lumped load, if used, should be four or fewer loads.

7. For wire–OR (emitter dotting), two–way lines (busses) are recommended. To produce such lines, both ends of a transmission line are terminated with 100–ohm impedance. This method should be used when wire–OR connections exceed 1 inch apart on a drive line.

B. Off–Card Clock Distribution

1. The OR/NOR outputs of an MC1660 may be used to drive into twisted pair lines or into flat, fixed–impedance ribbon cable. At the far end of the twisted pair on MC1692 differential line receiver is used. The line should be terminated as shown in Figure 16. This method not only provides high speed, board–to–board clock distribution, but also provides system noise margin advantages. Since the line receiver operates independently of the V_{BB} reference voltage (differential inputs) the noise margin from board to board is also independent of temperature differentials.

LOGIC SHORTCUTS

MECL circuitry offers several logic design conveniences. Among these are:

1. **Wire–OR** (can be produced by wiring MECL output emitters together outside packages).
2. **Complementary Logic Outputs** (both OR and NOR are brought out to package pins in most cases).

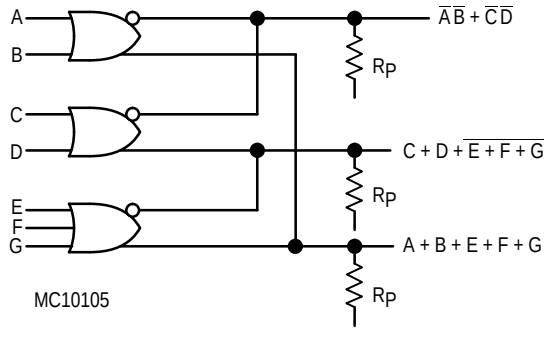
An example of the use of these two features to reduce gate and package count is shown in Figure 20.

The connection shown saves several gate circuits over performing the same functions with non–ECL type logic. Also, the logic functions in Figure 20 are all accomplished with one gate propagation delay time for best system speed. Wire–ORing permits direct connections of MECL circuits to busses. (MECL System Design Handbook and Application Note AN–726).

Propagation delay is increased approximately 50 ps per wire–OR connection. In general, wire–OR should be limited to 6 MECL outputs to maintain a proper LOW logic level. The MC10123 is an exception to this rule because it has a special V_{OL} level that allows very high fanout on a bus or wire–OR line. The use of a single output pull–down resistor is recommended per wire–OR, to economize on power dissipation. However, two pull–down resistors per wired–OR can improve fall times and be used for double termination of busses.

Wire–OR should be done between gates in a package or nearby packages to avoid spikes due to line propagation delay. This does not apply to bus lines which activate only one driver at a time.

Figure 20 — USE OF WIRE–OR AND COMPLEMENTARY OUTPUTS



SYSTEM CONSIDERATIONS — A SUMMARY OF RECOMMENDATIONS

	MECL 10H	MECL 10K	MECL III
Power Supply Regulation	±5% (1)	10% (2)	10% (2)
On–Card Temperature Gradient	20°C	Less Than 25°C	Less Than 25°C
Maximum Non–Transmission Line Length (No Damping Resistor)	1″	8″	1″
Unused Inputs	Leave Open (3)	Leave Open (3)	Leave Open (3)
PC Board	Multilayer	Standard 2–Sided or Multilayer	Multilayer
Cooling Requirements	500 lfpm Air	500 lfpm Air	500 lfpm Air
Bus Connection Capability	Yes (Wire–OR)	Yes (Wire–OR)	Yes (Wire–OR)
Maximum Twisted Pair Length (Differential Drive)	Limited By Cable Response Only, Usually >1000′	Limited by Cable Response Only, Usually >1000′	Limited by Cable Response Only, Usually >1000′
The Ground Plane to Occupy Percent Area of Card	>75%	>50%	>75%
Wire Wrap may be used	Not Recommended	Yes	Not Recommended
Compatible with MECL 10,000	Yes	—	Yes

(1) All dc and ac parameters guaranteed for V_{EE} = –5.2 V ± 5%.
(2) At the devices (functional only).
(3) Except special functions without input pull–down resistors.