MOTOROLA

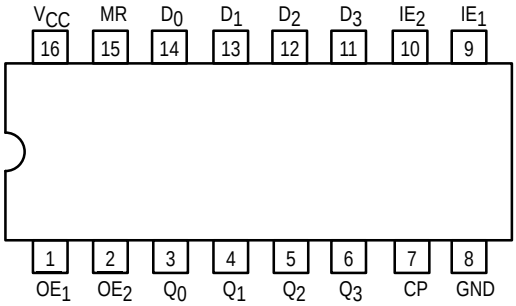
SN54/74LS173A

4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

The SN54/74LS173A is a high-speed 4-Bit Register featuring 3-state outputs for use in bus-organized systems. The clock is fully edge-triggered allowing either a load from the D inputs or a hold (retain register contents) depending on the state of the Input Enable Lines ($\overline{IE}_1$, $\overline{IE}_2$). A HIGH on either Output Enable line (OE_1, OE_2) brings the output to a high impedance state without affecting the actual register contents. A HIGH on the Master Reset (MR) input resets the Register regardless of the state of the Clock (CP), the Output Enable (OE_1, OE_2) or the Input Enable ($\overline{IE}_1$, $\overline{IE}_2$) lines.

- Fully Edge-Triggered
- 3-State Outputs
- Gated Input and Output Enables
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

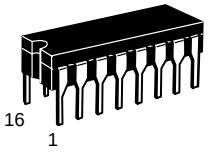
PIN NAMES

		LOADING (Note a) HIGH	LOW
D_0-D_3	Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{IE}_1-\overline{IE}_2$	Input Enable (Active LOW)	0.5 U.L.	0.25 U.L.
OE_1-OE_2	Output Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
CP	Clock Pulse (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset Input (Active HIGH)	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Outputs (Note b)	65 (25) U.L.	15 (7.5) U.L.

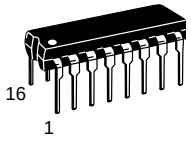
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

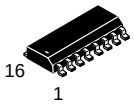
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

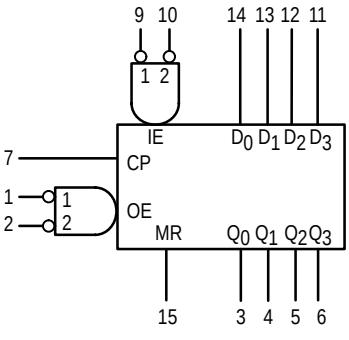


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

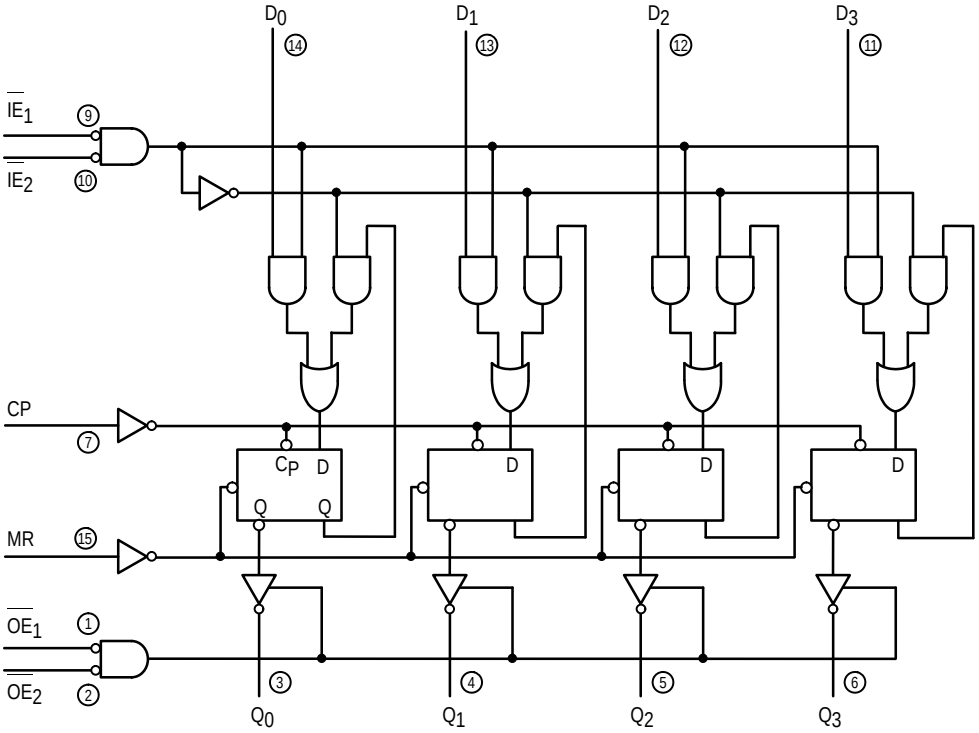
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8
◯ = PIN NUMBERS

TRUTH TABLE

MR	CP	$\overline{IE}_1$	$\overline{IE}_2$	D_n	Q_n
H	x	x	x	x	L
L	L	x	x	x	Q_n
L	⌐	H	x	x	Q_n
L	⌐	x	H	x	Q_n
L	⌐	L	L	L	L
L	⌐	L	L	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

When either OE_1, or OE_2 are HIGH, the output is in the off state (High Impedance); however this does not affect the contents or sequential operation of the register.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	–55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			–1.0 –2.6	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.4	3.1		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_O = 2.7 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_O = 0.4 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				30	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
f_{MAX}	Maximum Input Clock Frequency	30	50		MHz	V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		17 22	25 30	ns	
t_{PHL}	Propagation Delay, MR to Output		26	35	ns	
t_{PZH} t_{PZL}	Output Enable Time		15 18	23 27	ns	
t_{PLZ} t_{PHZ}	Output Disable Time		11 11	17 17	ns	C_L = 5.0 pF, R_L = 667 Ω

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_W	Clock or MR Pulse Width	20			ns	V_{CC} = 5.0 V
t_s	Data Enable Setup Time	35			ns	
t_s	Data Setup Time	17			ns	
t_h	Hold Time, Any Input	0			ns	
t_{rec}	Recovery Time	10			ns	

AC WAVEFORMS

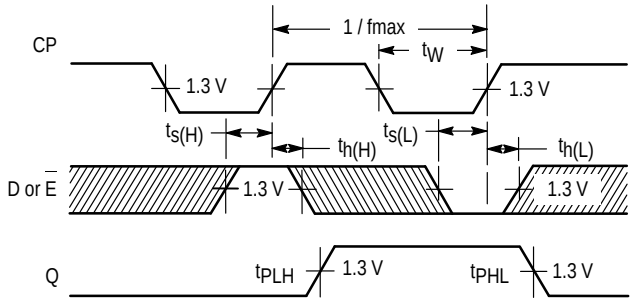


Figure 1

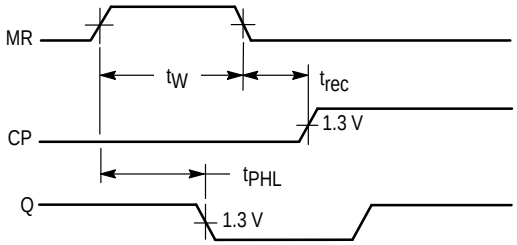


Figure 2

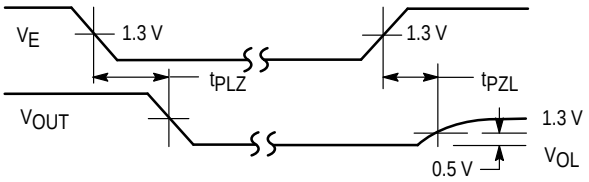


Figure 3

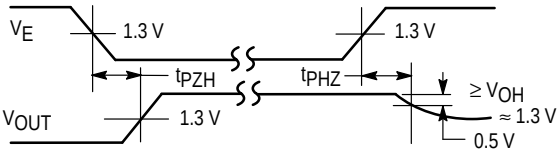
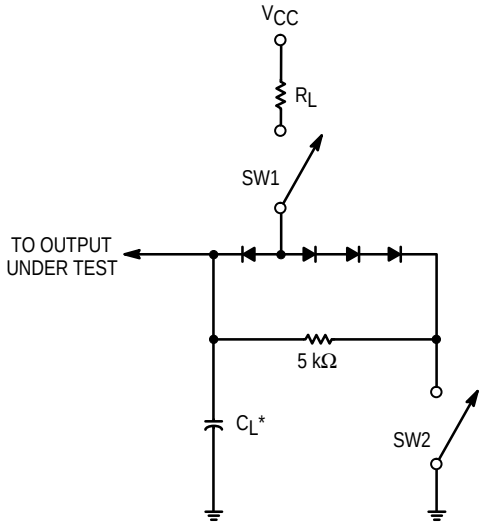


Figure 4

AC LOAD CIRCUIT



*Includes Jig and Probe Capacitance.

Figure 5

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed