MOTOROLA

# SN54/74LS170

# 4 x 4 REGISTER FILE OPEN-COLLECTOR

The TTL/MSI SN54/74LS170 is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

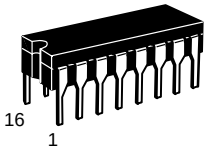
Open-collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The SN54/74LS670 provides a similar function to this device but it features 3-state outputs.

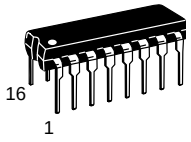
- Simultaneous Read/Write Operation
- Expandable to 512 Words of n-Bits
- Typical Access Time of 20 ns
- Low Leakage Open-Collector Outputs for Expansion
- Typical Power Dissipation of 125 mW

**4 x 4 REGISTER FILE OPEN-COLLECTOR**

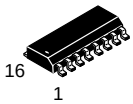
**LOW POWER SCHOTTKY**




**J SUFFIX**
CERAMIC
CASE 620-09




**N SUFFIX**
PLASTIC
CASE 648-08

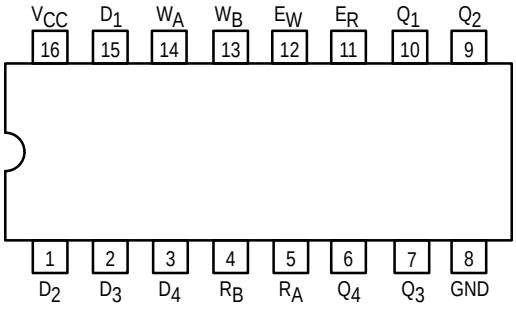



**D SUFFIX**
SOIC
CASE 751B-03

**ORDERING INFORMATION**

| | |
|---|---|
| SN54LSXXXJ | Ceramic |
| SN74LSXXXN | Plastic |
| SN74LSXXXD | SOIC |

**CONNECTION DIAGRAM DIP** (TOP VIEW)



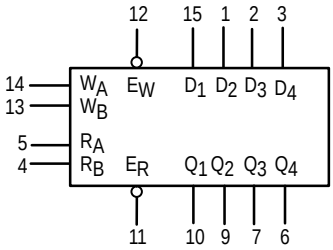

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

**PIN NAMES**

| | | LOADING (Note a) HIGH | LOW |
|---|---|---|---|
| $D_1-D_4$ | Data Inputs | 0.5 U.L. | 0.25 U.L. |
| $\overline{W}_A$, $W_B$ | Write Address Inputs | 0.5 U.L. | 0.25 U.L. |
| $E_W$ | Write Enable (Active LOW) Input | 1.0 U.L. | 0.5 U.L. |
| $\overline{R}_A$, $R_B$ | Read Address Inputs | 0.5 U.L. | 0.25 U.L. |
| $E_R$ | Read Enable (Active LOW) Input | 1.0 U.L. | 0.5 U.L. |
| $Q_1-Q_4$ | Outputs (Note b) | Open-Collector | 5 (2.5) U.L. |

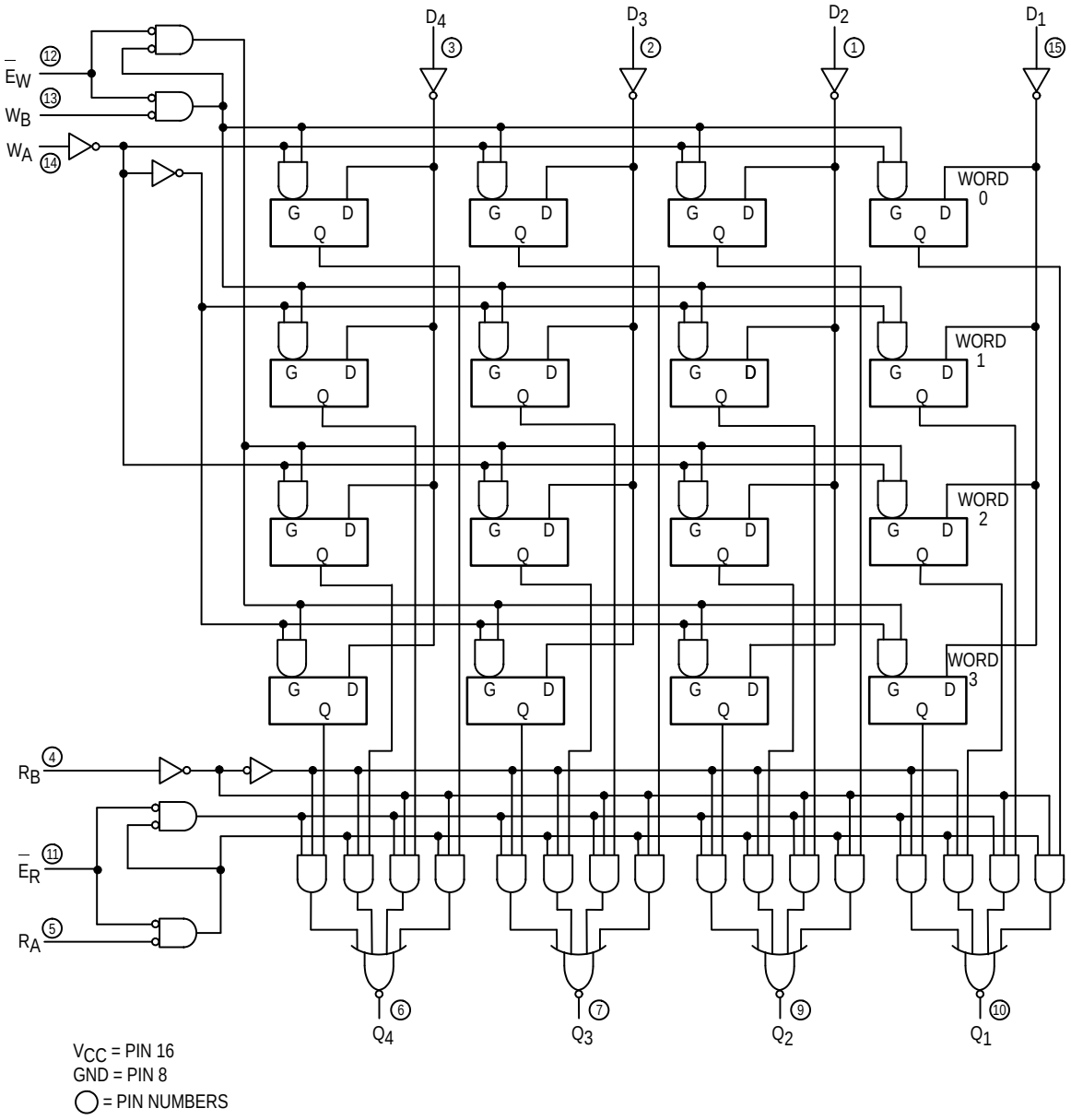
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive must be supplied by an external resistor to $V_{CC}$.

**LOGIC SYMBOL**




$V_{CC}$ = PIN 16
GND = PIN 8

**LOGIC DIAGRAM**



**WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)**

| WRITE INPUTS | | | WORD | | | |
|---|---|---|---|---|---|---|
| $W_B$ | $W_A$ | $\overline{E}_W$ | 0 | 1 | 2 | 3 |
| L | L | L | Q = D | $Q_0$ | $Q_0$ | $Q_0$ |
| L | H | L | $Q_0$ | Q = D | $Q_0$ | $Q_0$ |
| H | L | L | $Q_0$ | $Q_0$ | Q = D | $Q_0$ |
| H | H | L | $Q_0$ | $Q_0$ | $Q_0$ | Q = D |
| X | X | H | $Q_0$ | $Q_0$ | $Q_0$ | $Q_0$ |

**READ FUNCTION TABLE (SEE NOTES A AND D)**

| READ INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| $R_B$ | $R_A$ | $\overline{E}_R$ | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ |
| L | L | L | W0B1 | W0B2 | W0B3 | W0B4 |
| L | H | L | W1B1 | W1B2 | W1B3 | W1B4 |
| H | L | L | W2B1 | W2B2 | W2B3 | W2B4 |
| H | H | L | W3B1 | W3B2 | W3B3 | W3B4 |
| X | X | H | H | H | H | H |

NOTES: A. H = HIGH Level. L = LOW Level, X = Irrelevant.
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. $Q_0$ = the level of Q before the indicated input conditions were established.
D. $W_{0B1}$ = The first bit of word 0, etc.

**GUARANTEED OPERATING RANGES**

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 54<br>74 | 4.5<br>4.75 | 5.0<br>5.0 | 5.5<br>5.25 | V |
| $T_A$ | Operating Ambient Temperature Range | 54<br>74 | −55<br>0 | 25<br>25 | 125<br>70 | °C |
| $V_{OH}$ | Output Voltage — High | 54, 74 | | | 5.5 | V |
| $I_{OL}$ | Output Current — Low | 54<br>74 | | | 4.0<br>8.0 | mA |

**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| Symbol | Parameter | | Limits Min | Limits Typ | Limits Max | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | 54 | | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs | |
| | | 74 | | | 0.8 | | | |
| $V_{IK}$ | Input Clamp Diode Voltage | | | −0.65 | −1.5 | V | $V_{CC}$ = MIN, $I_{IN}$ = −18 mA | |
| $I_{OH}$ | Output HIGH Current | 54, 74 | | | 100 | µA | $V_{CC}$ = MIN, $V_{OH}$ = MAX | |
| $V_{OL}$ | Output LOW Voltage | 54, 74 | | 0.25 | 0.4 | V | $I_{OL}$ = 4.0 mA | $V_{CC}$ = $V_{CC}$ MIN, $V_{IN}$ = $V_{IL}$ or $V_{IH}$ per Truth Table |
| | | 74 | | 0.35 | 0.5 | V | $I_{OL}$ = 8.0 mA | |
| $I_{IH}$ | Input HIGH Current<br>Any D, R, W<br>$E_R$, $E_W$ | | | | 20<br>40 | µA | $V_{CC}$ = MAX, $V_{IN}$ = 2.4 V | |
| | Any D, R, W<br>$E_R$, $E_W$ | | | | 0.1<br>0.2 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 7.0 V | |
| $I_{IL}$ | Input LOW Current<br>Any D, R, W<br>$E_R$, $E_W$ | | | | −0.4<br>−0.8 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 0.4 V | |
| $I_{CC}$ | Power Supply Current | | | | 40 | mA | $V_{CC}$ = MAX | |

**AC CHARACTERISTICS** ($T_A$ = 25°C)

| Symbol | Parameter | Limits | | | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay, Negative-Going $\overline{E}_R$ to Q Outputs | | 20<br>20 | 30<br>30 | ns | Figure 1 | $V_{CC}$ = 5.0 V<br>$C_L$ = 15 pF<br>$R_L$ = 2.0 kΩ |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay, $R_A$ or $R_B$ to Q Outputs | | 25<br>24 | 40<br>40 | ns | Figure 2 | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay, Negative-Going $\overline{E}_W$ to Q Outputs | | 30<br>26 | 45<br>40 | ns | Figure 1 | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay, Data Inputs to Q Outputs | | 30<br>22 | 45<br>35 | ns | Figure 1 | |

**AC SETUP REQUIREMENTS** ($T_A$ = 25°C)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| $t_W$ | Pulse Width, $\overline{E}_R$, $\overline{E}_W$ | 25 | | | ns | $V_{CC}$ = 5.0 V<br>$R_L$ = 2.0 kΩ |
| $t_s$ | Setup Time, Data to $\overline{E}_W$ | 10 | | | ns | |
| $t_s$ | Setup Time, $W_A$, $W_B$ to $\overline{E}_W$ | 15 | | | ns | |
| $t_h$ | Hold Time, Data to $\overline{E}_W$ | 15 | | | ns | |
| $t_h$ | Hold Time, $W_A$, $W_B$ to $\overline{E}_W$ | 5.0 | | | ns | |
| $t_{LATCH}$ | Latch Time | 25 | | | ns | |

**VOLTAGE WAVEFORMS**

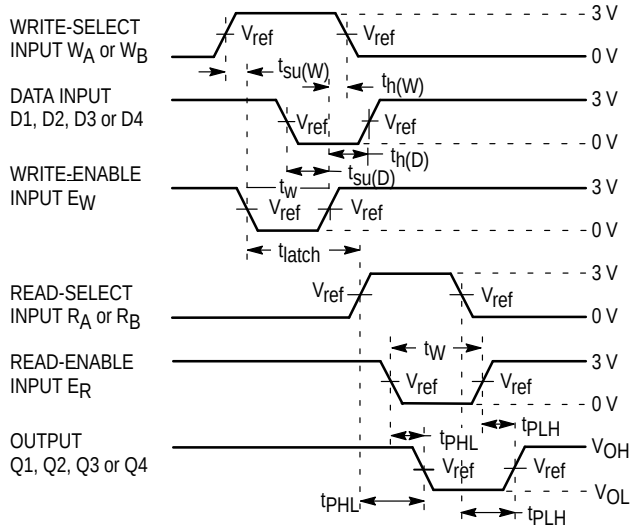



**Figure 1**

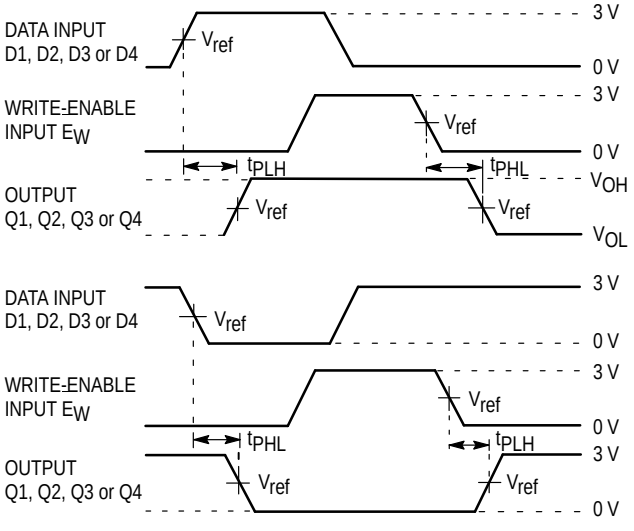



**Figure 2**