

Contents

Features..... 1

Pin Assignment..... 1

Block Diagram..... 2

Operation Mode 2

Absolute Maximum Ratings 2

Recommended Operating Conditions..... 2

DC Electrical Characteristics 3

Rewriting Times 3

Pin Capacitance..... 3

AC Electrical Characteristics..... 4

Operation 8

Dimensions 9

Ordering Information 10

Characteristics 11

The S-2812A and the S-2817A are low power 2K×8-bit parallel E²PROMs. The S-2812A features wide operating voltage range, and the S-2817A features 5-V single power supply. Since provided with 32-byte page write function, they can perform fast programming operation.

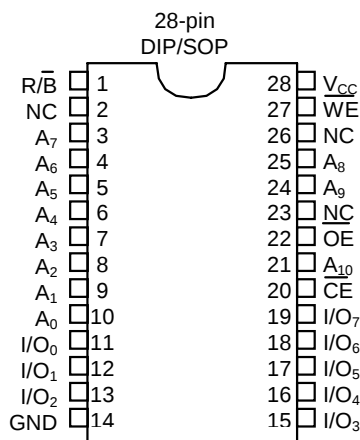
■ Features

- Access time: 150 ns
($V_{CC}=5\text{ V}\pm 10\%$, $T_a=0^\circ\text{C}$ to 70°C)
- Low power consumption
Operating: 30 mA max. ($V_{CC}=5\text{ V}\pm 10\%$)
Standby: 1 μA max. ($V_{CC}=5\text{ V}\pm 10\%$)
- Operating voltage range

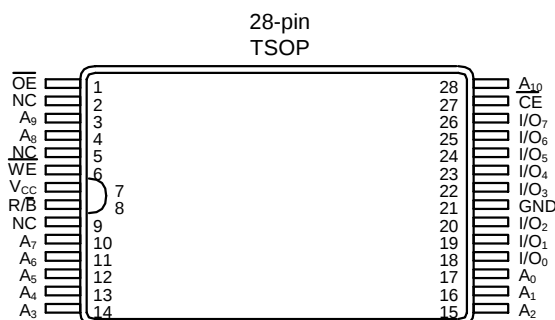
	S-2812A	S-2817A
Read:	1.8 to 5.5 V	5 V $\pm 10\%$
Write:	2.7 to 5.5 V	5 V $\pm 10\%$
- Write inhibition

S-2812A:	2.1 V typ.
S-2817A:	3.5 V typ.
- Data polling
- With Ready/Busy pin
- Page write for 32 bytes
- Rewritings: 10⁵ times
- Data retention: 10 years
- Program noise immunity
- Package: 28-pin DIP/SOP/TSOP
- Supply in bare chip is also available

■ Pin Assignment



Pin name	Function
A_0 to A_{10}	Address input
I/O_0 to I/O_7	Data input / output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$R/\overline{B}$	Ready/Busy (opendrain output)
V_{CC}	Power supply voltage
GND	Ground (0 V)



Figure

CMOS 16K-bit PARALLEL E²PROM
S-2812A/2817A

■ Block Diagram

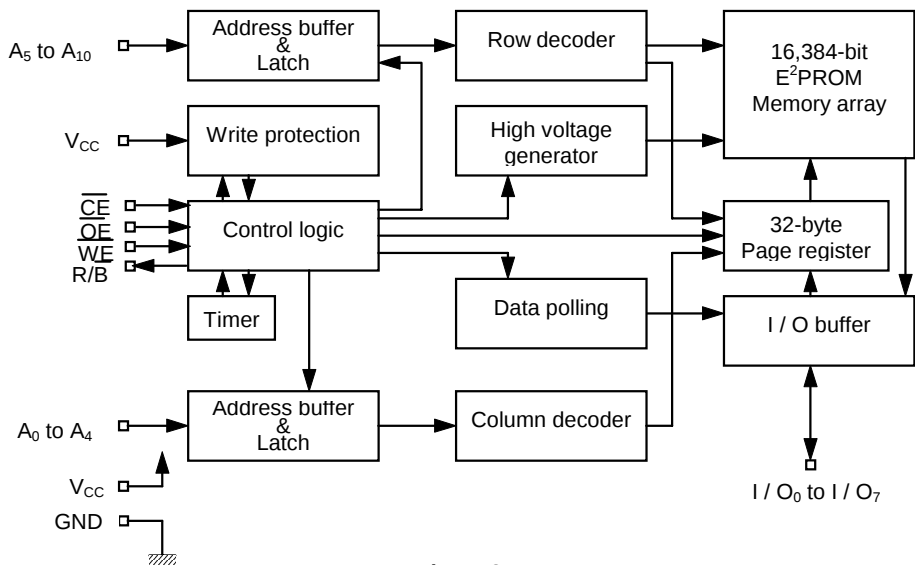


Figure 2

■ Operation Mode

Table 1

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O
Read	L	L	H	Data output
Write	L	H	L	Data input
Write inhibition	x	x	H	—
	x	L	x	—
Standby	H	x	x	High-Z

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to $V_{\text{CC}}+0.3$	V
Output voltage	V_{OUT}	-0.3 to V_{CC}	V
Storage temperature under bias	T_{bias}	-50 to +95	°C
Storage temperature	T_{stg}	-65 to +150	°C

■ Recommended Operating Conditions

Table 3

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	S-2812A	1.8	—	5.5	V
		Read	2.7	—	5.5	V
		Write	—	—	—	V
High level input voltage	V_{IH}	S-2817A	4.5	5.0	5.5	V
		$V_{\text{CC}}=2.7$ to 5.5 V	2.2	—	$V_{\text{CC}}+0.3$	V
		$V_{\text{CC}}=1.8$ to 2.7 V	$0.8 \times V_{\text{CC}}$	—	$V_{\text{CC}}+0.3$	V
Low level input voltage	V_{IL}	$V_{\text{CC}}=5$ V $\pm 10\%$	-0.3	—	0.8	V
		$V_{\text{CC}}=2.7$ to 4.5 V	-0.3	—	0.4	V
		$V_{\text{CC}}=1.8$ to 2.7 V	-0.3	—	$0.2 \times V_{\text{CC}}$	V
Operating temperature	T_{opr}		-40	—	85	°C

■ DC Electrical Characteristics

1. S-2812A

Table 4

(Ta=-40°C to 85°C)

Parameter	Symbol	Conditions	5 V±10%			3 V±10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (Read)	I _{CC1}	$\overline{CE} \leq V_{IL}, V_{IN} \leq V_{IL} \text{ or } V_{IN} \geq V_{IH}$ I _{OUT} =0 mA, f=1/t _{RC}	—	—	30	—	—	15	mA
	I _{CC2}	$\overline{CE} \leq 0.2 \text{ V}, V_{IN} \leq 0.2 \text{ V or } V_{IN} \geq V_{CC}-0.2 \text{ V}$ I _{OUT} =0 mA, f=1/t _{RC}	—	—	25	—	—	10	mA
Current consumption (Program)	I _{CC3}	$\overline{CE} \leq V_{IL}, V_{IN} \leq V_{IL} \text{ or } V_{IN} \geq V_{IH}$	—	—	30	—	—	15	mA
	I _{CC4}	$\overline{CE} \leq 0.2 \text{ V}, V_{IN} \leq 0.2 \text{ V or } V_{IN} \geq V_{CC}-0.2 \text{ V}$	—	—	25	—	—	10	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{IH}$	—	—	1	—	—	0.5	mA
	I _{SB2}	$\overline{CE} \geq V_{CC}-0.2 \text{ V}$	—	—	1.0	—	—	1.0	μA
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}	—	—	1.0	—	—	1.0	μA
Output leakage current	I _{LO}	V _{I/O} =GND to V _{CC}	—	—	1.0	—	—	1.0	μA
High level output voltage	V _{OH}	5-V operation: I _{OH} =-400 μA 3-V operation: I _{OH} =-100 μA	2.4	—	—	2.4	—	—	V
Low level output voltage	V _{OL}	5-V operation: I _{OL} =2.1 mA 3-V operation: I _{OL} =400 μA	—	—	0.4	—	—	0.4	V

2. S-2817A

Table 5

(Ta=-40°C to 85°C, V_{CC}=5 V±10%)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption (Read)	I _{CC1}	$\overline{CE} \leq V_{IL}, V_{IN} \leq V_{IL} \text{ or } V_{IN} \geq V_{IH}$ I _{OUT} =0 mA, f=1/t _{RC}	—	—	30	mA
	I _{CC2}	$\overline{CE} \leq 0.2 \text{ V}, V_{IN} \leq 0.2 \text{ V or } V_{IN} \geq V_{CC}-0.2 \text{ V}$ I _{OUT} =0 mA, f=1/t _{RC}	—	—	25	mA
Current consumption (Program)	I _{CC3}	$\overline{CE} \leq V_{IL}, V_{IN} \leq V_{IL} \text{ or } V_{IN} \geq V_{IH}$	—	—	30	mA
	I _{CC4}	$\overline{CE} \leq 0.2 \text{ V}, V_{IN} \leq 0.2 \text{ V or } V_{IN} \geq V_{CC}-0.2 \text{ V}$	—	—	25	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{IH}$	—	—	1	mA
	I _{SB2}	$\overline{CE} \geq V_{CC}-0.2 \text{ V}$	—	—	1.0	μA
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}	—	—	1.0	μA
Output leakage current	I _{LO}	V _{I/O} =GND to V _{CC}	—	—	1.0	μA
High level output voltage	V _{OH}	I _{OH} =-400 μA	2.4	—	—	V
Low level output voltage	V _{OL}	I _{OL} =2.1 mA	—	—	0.4	V

■ Rewriting Times

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit
Rewriting times	N _W	10 ⁵	—	—	times/byte

■ Pin Capacitance

Table 7

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0 V	—	—	10	pF
Input / output capacitance	C _{I/O}	V _{I/O} =0 V	—	—	10	pF

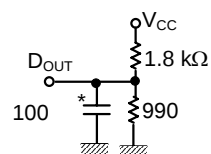
CMOS 16K-bit PARALLEL E²PROM

S-2812A/2817A

■ AC Electrical Characteristics

Table 8 Measuring conditions

Parameter	S-2812A	S-2817A
Input pulse levels	$V_{IL}=0.2\text{ V}$ $V_{IH}=2.4\text{ V}$	$V_{IL}=0.4\text{ V}$ $V_{IH}=2.4\text{ V}$
Input rise and fall time	10 ns	10 ns
I/O reference level	1.5 V	1.5 V
Output load	See Figure 3	See Figure 3



* (When measuring t_{CLZ} , t_{OLZ} , t_{CHZ} , t_{OHZ} , t_{WHZ} , t_{WLZ}) : 5pF

Figure 3 Output load measuring circuit

1. Read Cycle

(1) 5-V operation

Table 9

($V_{CC}=5\text{ V}\pm 10\%$)

Parameter	Symbol	0°C to 70°C		-40°C to 85°C		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	150	—	200	—	ns
$\overline{CE}$ access time	t_{CE}	—	150	—	200	ns
Address access time	t_{AA}	—	150	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	70	—	90	ns
Output enable time ($\overline{CE}$)	t_{CLZ}	10	—	10	—	ns
Output enable time ($\overline{OE}$)	t_{OLZ}	10	—	10	—	ns
Output disable time ($\overline{CE}$)	t_{CHZ}	10	70	10	90	ns
Output disable time ($\overline{OE}$)	t_{OHZ}	10	70	10	90	ns
Output data hold time	t_{OH}	5	—	5	—	ns

(2) 3-V operation (S-2812A only)

Table 10

($V_{CC}=3\text{ V}\pm 10\%$)

Parameter	Symbol	0°C to 70°C		-40°C to 85°C		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	400	—	500	—	ns
$\overline{CE}$ access time	t_{CE}	—	400	—	500	ns
Address access time	t_{AA}	—	400	—	500	ns
$\overline{OE}$ access time	t_{OE}	—	200	—	250	ns
Output enable time ($\overline{CE}$)	t_{CLZ}	25	—	30	—	ns
Output enable time ($\overline{OE}$)	t_{OLZ}	25	—	30	—	ns
Output disable time ($\overline{CE}$)	t_{CHZ}	25	200	30	250	ns
Output disable time ($\overline{OE}$)	t_{OHZ}	25	200	30	250	ns
Output data hold time	t_{OH}	10	—	15	—	ns

2. Write Cycle

(1) 5-V operation

Table 11

(V_{CC}=5 V±10%)

Parameter	Symbol	0°C to 70°C		-40°C to 85°C		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	—	10	—	10	ms
Address setup time	t _{AS}	0	—	0	—	ns
Address hold time	t _{AH}	120	—	150	—	ns
Write setup time	t _{CS}	0	—	0	—	ns
Write hold time	t _{CH}	0	—	0	—	ns
$\overline{\text{CE}}$ pulse width	t _{CW}	120	—	150	—	ns
$\overline{\text{OE}}$ setup time	t _{OES}	15	—	20	—	ns
$\overline{\text{OE}}$ hold time	t _{OEh}	15	—	20	—	ns
$\overline{\text{WE}}$ pulse width	t _{WP}	120	—	150	—	ns
Data setup time	t _{DS}	85	—	100	—	ns
Data hold time	t _{DH}	0	—	0	—	ns
Page load time (page data setting time)	t _{PL}	0.3	30	0.3	30	μs
Page load time (page data write start time)	t _{PDL}	100	—	100	—	μs
Time to device busy	t _{DB}	110	—	140	—	ns

(2) 3-V operation (S-2812A only)

Table 12

(V_{CC}=3 V±10%)

Parameter	Symbol	0°C to 70°C		-40°C to 85°C		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	—	10	—	10	ms
Address setup time	t _{AS}	0	—	0	—	ns
Address hold time	t _{AH}	300	—	350	—	ns
Write setup time	t _{CS}	0	—	0	—	ns
Write hold time	t _{CH}	0	—	0	—	ns
$\overline{\text{CE}}$ pulse width	t _{CW}	300	—	350	—	ns
$\overline{\text{OE}}$ setup time	t _{OES}	30	—	35	—	ns
$\overline{\text{OE}}$ hold time	t _{OEh}	30	—	35	—	ns
$\overline{\text{WE}}$ pulse width	t _{WP}	300	—	350	—	ns
Data setup time	t _{DS}	180	—	210	—	ns
Data hold time	t _{DH}	0	—	0	—	ns
Page load time (page data setting time)	t _{PL}	0.3	30	0.3	30	μs
Page load time (page data write start time)	t _{PDL}	100	—	100	—	μs
Time to device busy	t _{DB}	250	—	300	—	ns

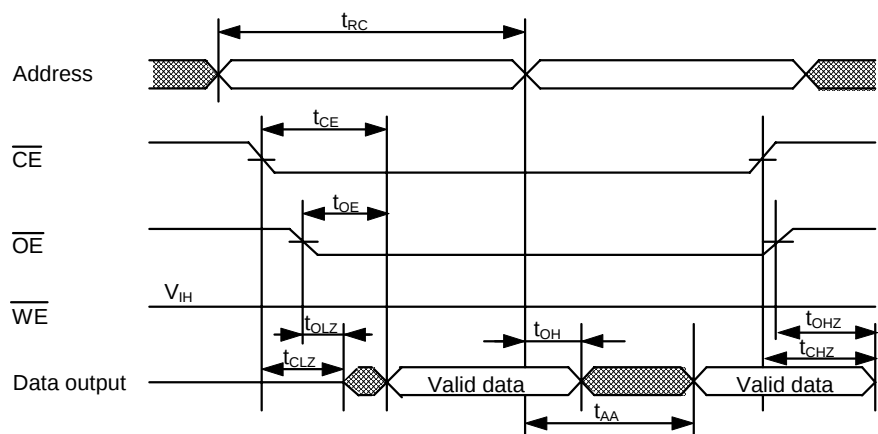


Figure 4 Read cycle

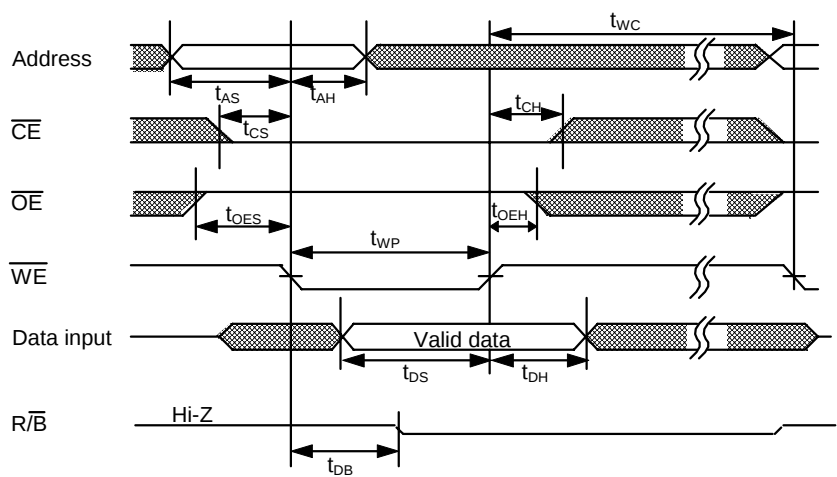


Figure 5 $\overline{WE}$ controlled write cycle

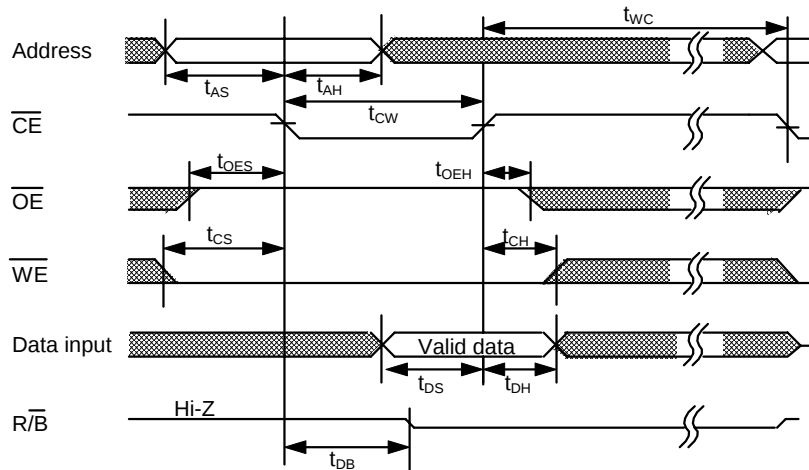


Figure 6 $\overline{\text{CE}}$ controlled write cycle

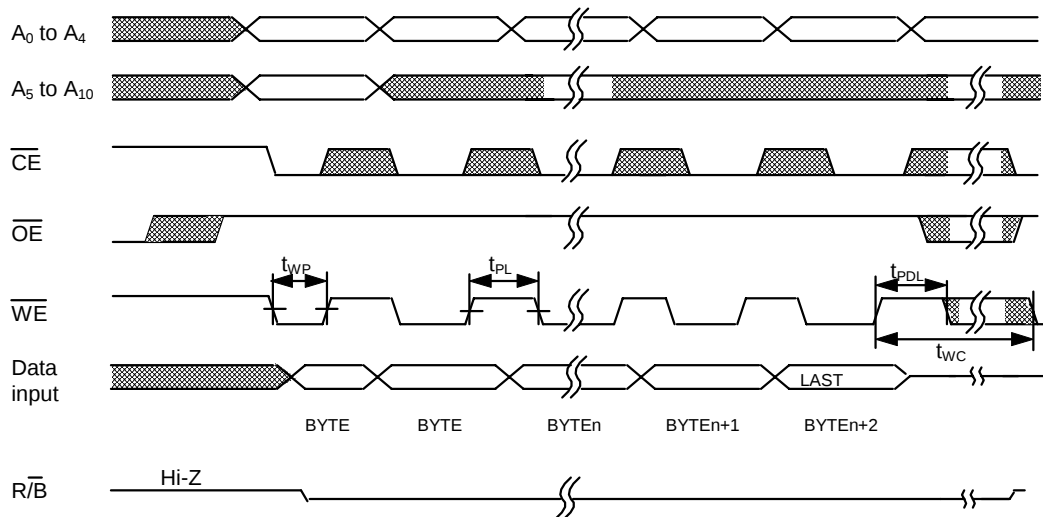


Figure 7 Page write cycle

CMOS 16K-bit PARALLEL E²PROM

S-2812A/2817A

■ Operation

(1) Read mode

This mode outputs data to I/O₀ to I/O₇ when both $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low and when $\overline{\text{WE}}$ is high. The data bus is high impedance when either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ is high.

(2) Byte write mode

A byte write cycle starts when both $\overline{\text{CE}}$ and $\overline{\text{WE}}$ are low and $\overline{\text{OE}}$ is high. $\overline{\text{CE}}$ - and $\overline{\text{WE}}$ -controlled write cycles are available. The address is latched at the falling of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ whichever occurs last, and the data is latched at the rising of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ whichever occurs first.

(3) Page write mode

In this mode, 1 page program operation of 32 bytes is completed in 10 ms, and all memory area is written within a second because the device organization is 64-page × 32-byte. When starting this mode, first, addresses A₅ to A₁₀ assign the page, then A₀ to A₄ assign the address to each byte within the page sequentially or at random. Less than 32 bytes of program is available. This address assignment is performed while $0.3 \mu\text{s} \leq t_{\text{PL}} \leq 30 \mu\text{s}$, and the program operation starts when $t_{\text{PDL}} \geq 100 \mu\text{s}$.

(4) Data polling

This function is to output the complement data written last on I/O₇ and to output low to I/O₀ to I/O₆. This operation is performed by read operation during write cycle. $\text{R}/\overline{\text{B}}$ outputs low during write cycle; it is in high impedance in other modes.

(5) Erase all mode

All data is erased when $\overline{\text{OE}}$ is 13 V and both $\overline{\text{CE}}$ and $\overline{\text{WE}}$ are low. During erase all mode, A₀ to A₁₀ and I/O₀ to I/O₇ must be fixed to either high or low.

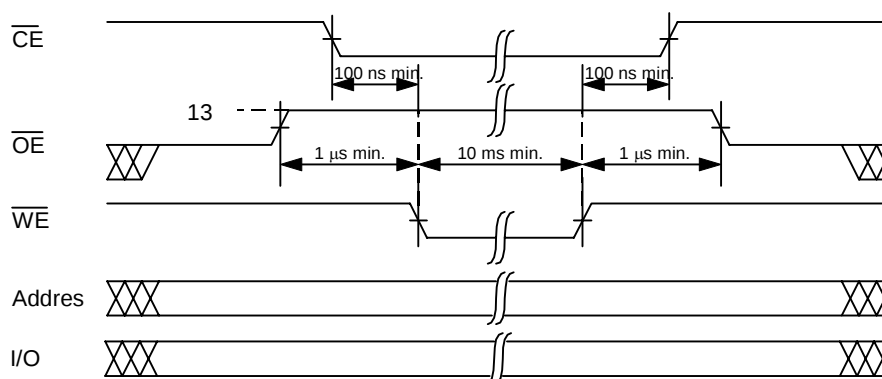


Figure 8

(6) Write inhibition

Write operation is inhibited in the following cases :

- When power supply voltage is under write inhibit voltage (V_{WI}).
S-2817A : $V_{\text{WI}}=3.5 \text{ V typ.}$
S-2812A : $V_{\text{WI}}=2.1 \text{ V typ.}$
- When $\overline{\text{OE}}$ is low, or $\overline{\text{WE}}$ is high.

(7) Program noise immunity

$\overline{\text{CE}}$, $\overline{\text{OE}}$ and $\overline{\text{WE}}$ are noise protected for preventing erroneous write operation at power on and off. Less than 20 ns write pulse will not activate a write cycle at 5-V operation, and less than 50 ns at 3-V operation. See Figure 9.

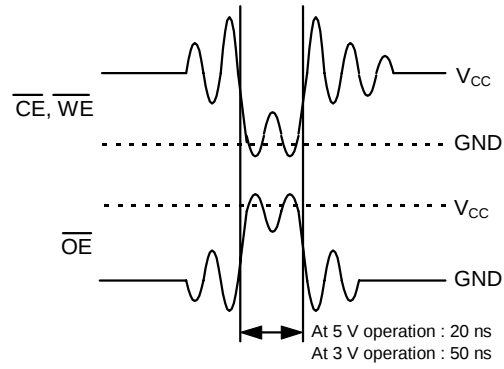


Figure 9

■ Dimensions (Unit : mm)

1. 28-pin DIP

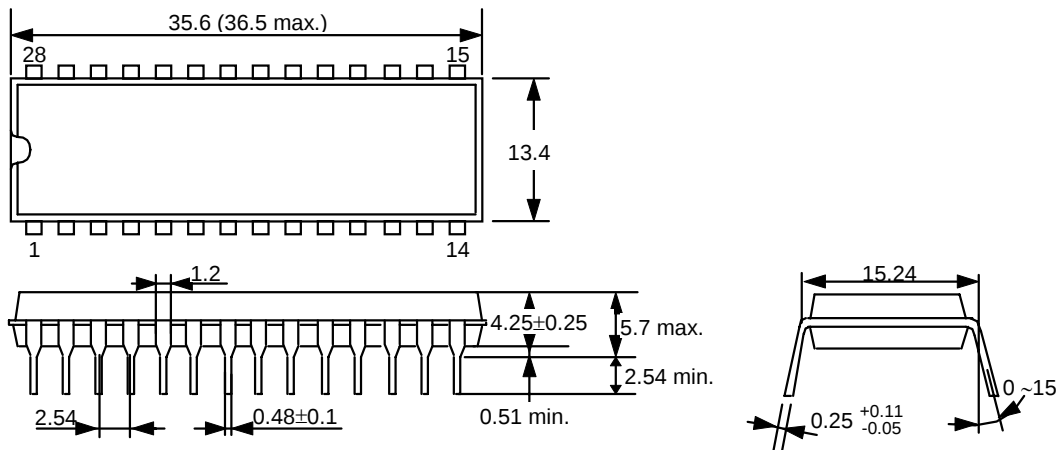


Figure 10

2. 28-pin SOP

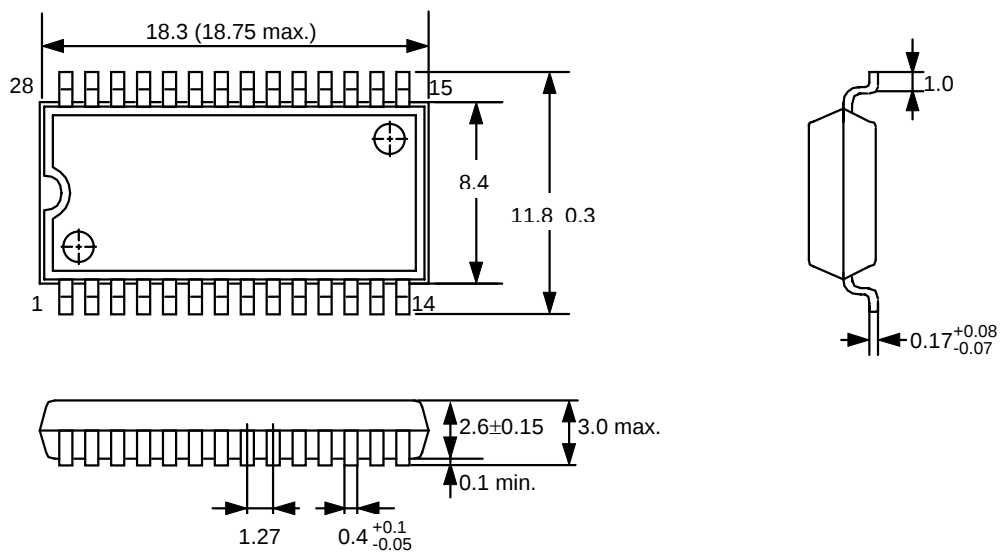


Figure 11

CMOS 16K-bit PARALLEL E²PROM
S-2812A/2817A

3. 28-pin TSOP

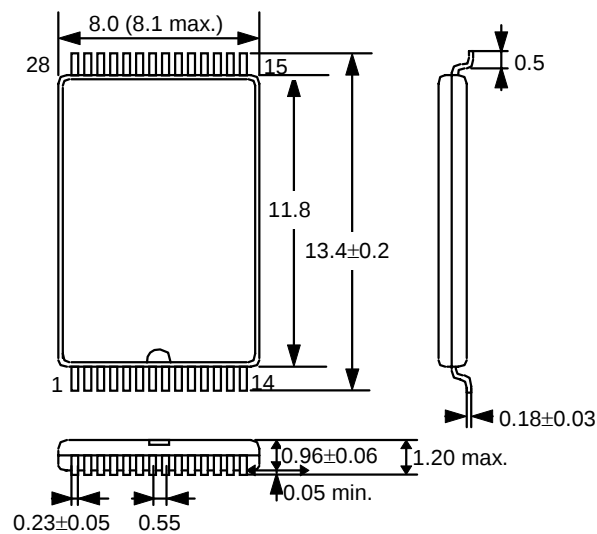


Figure 12

■ Ordering Information

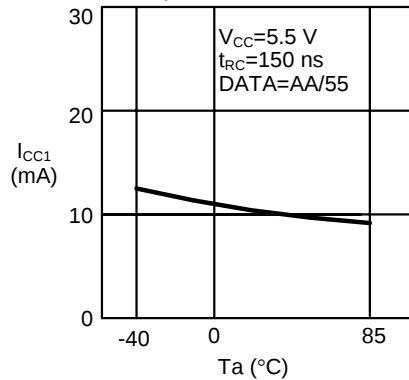
S-281XA	XX	-	XXX	
				Access time
				150 : 150 ns (5 V±10%, 0°C to 70°C)
				Package
				DP : DIP
				FE : SOP
				TF : TSOP
				CA : Bare chip
				Product name
				S-2812A : 1.8 V to 5.5 V (Read)
				: 2.7 V to 5.5 V (Write)
				S-2817A : 5 V±10%

Note: Each bit is set to 1 before delivery (except bare chip)

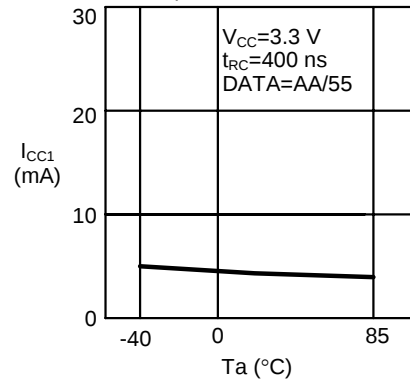
■ Characteristics

1. DC characteristics

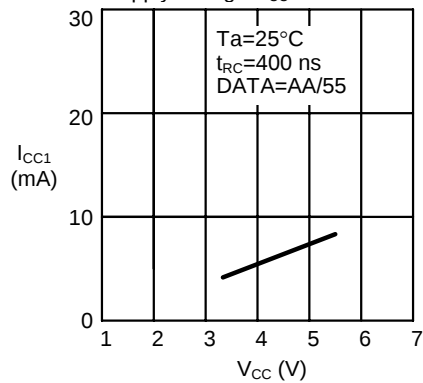
1.1 Current consumption (READ) I_{CC1} -
Ambient temperature T_a



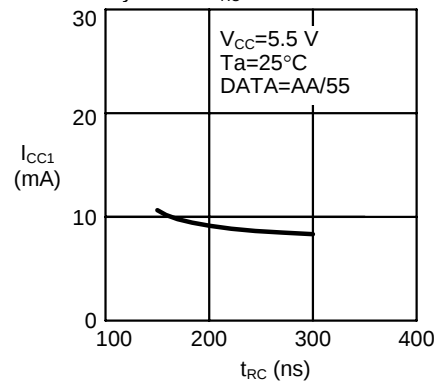
1.2 Current consumption (READ) I_{CC1} -
Ambient temperature T_a



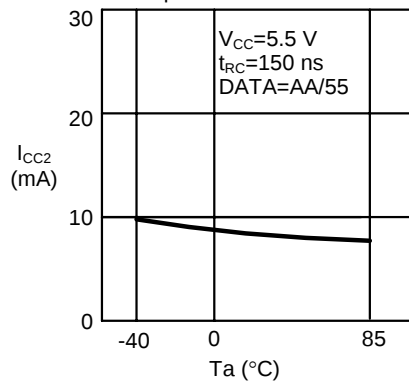
1.3 Current consumption (READ) I_{CC1} -
Power supply voltage V_{CC}



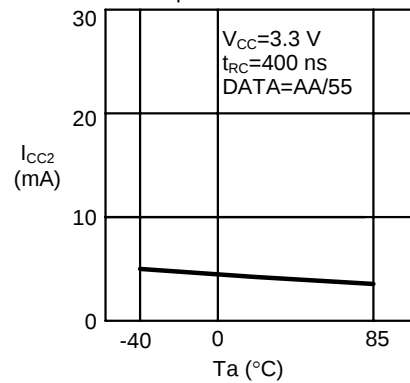
1.4 Current consumption (READ) I_{CC1} -
Read cycle time t_{RC}



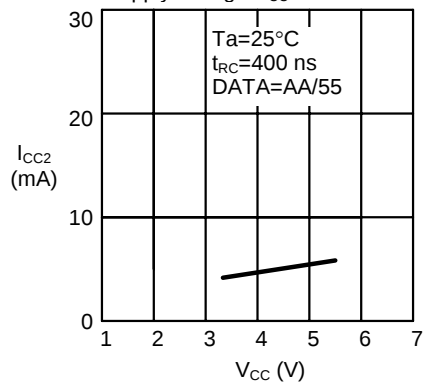
1.5 Current consumption (READ) I_{CC2} -
Ambient temperature T_a



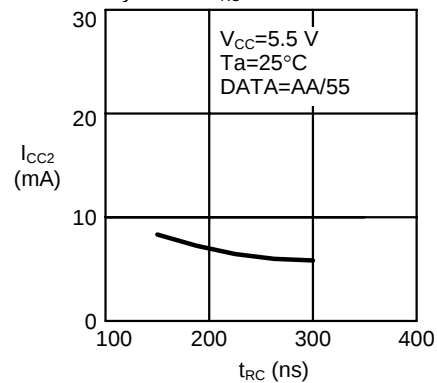
1.6 Current consumption (READ) I_{CC2} -
Ambient temperature T_a



1.7 Current consumption (READ) I_{CC2} -
Power supply voltage V_{CC}

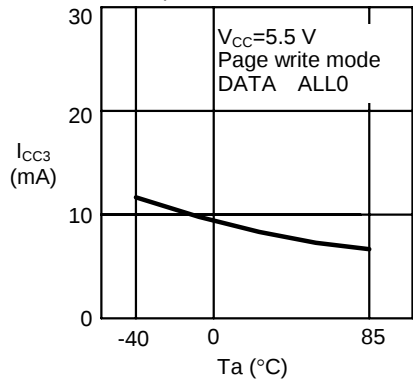


1.8 Current consumption (READ) I_{CC2} -
Read cycle time t_{RC}

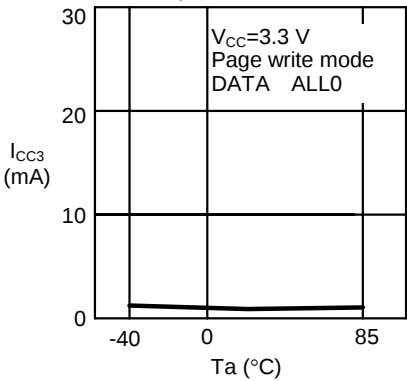


CMOS 16K-bit PARALLEL E²PROM
S-2812A/2817A

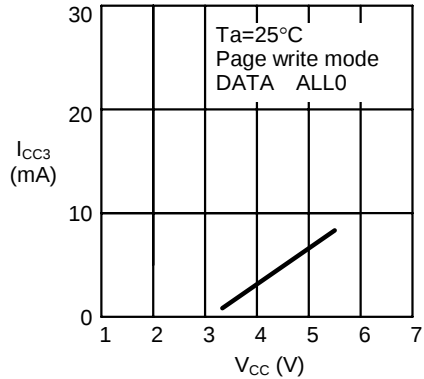
1.9 Current consumption (PROGRAM) I_{CC3} - Ambient temperature T_a



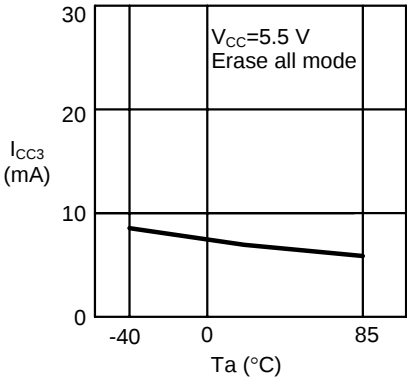
1.10 Current consumption (PROGRAM) I_{CC3} - Ambient temperature T_a



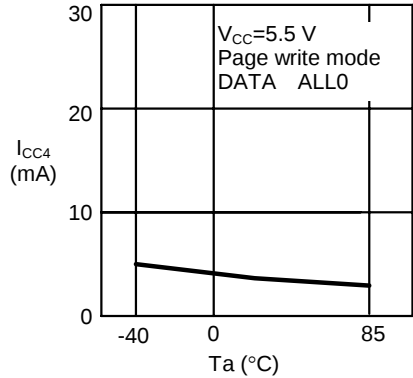
1.11 Current consumption (PROGRAM) I_{CC3} - Power Supply Voltage V_{CC}



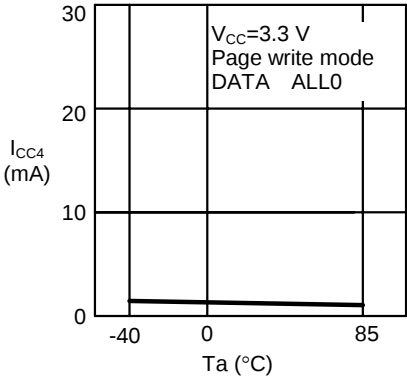
1.12 Current consumption (PROGRAM) I_{CC3} - Ambient temperature T_a



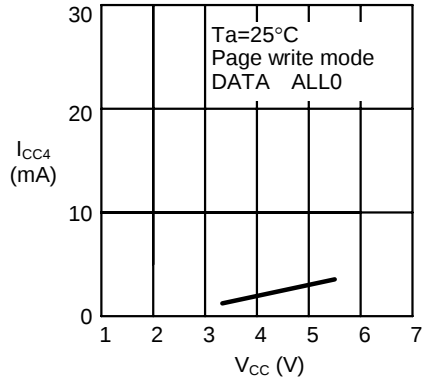
1.13 Current consumption (PROGRAM) I_{CC4} - Ambient temperature T_a



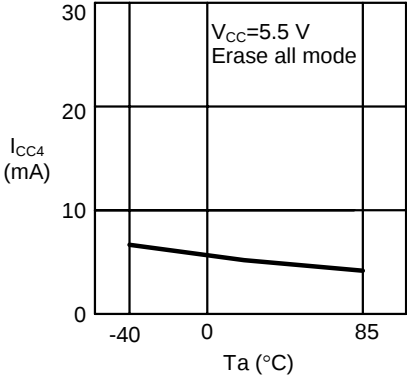
1.14 Current consumption (PROGRAM) I_{CC4} - Ambient temperature T_a



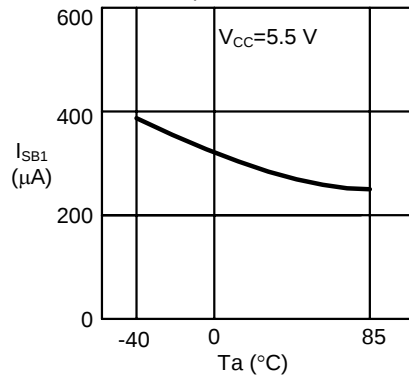
1.15 Current consumption (PROGRAM) I_{CC4} - Power Supply Voltage V_{CC}



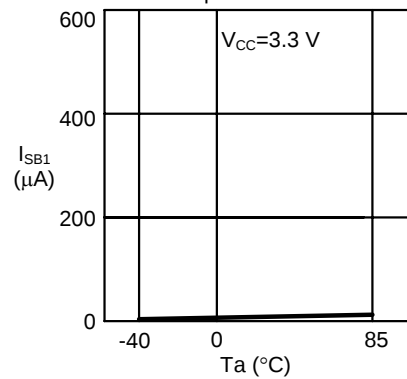
1.16 Current consumption (PROGRAM) I_{CC4} - Ambient temperature T_a



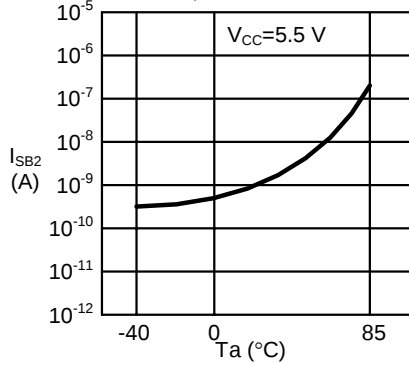
1.17 Standby current I_{SB1} -
Ambient temperature T_a



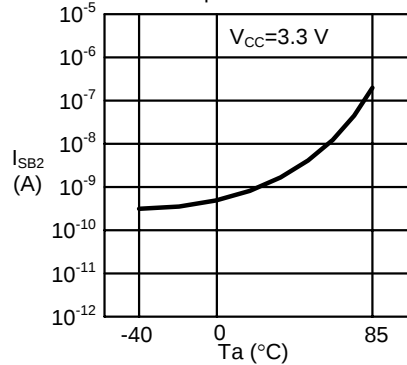
1.18 Standby current I_{SB1} -
Ambient temperature T_a



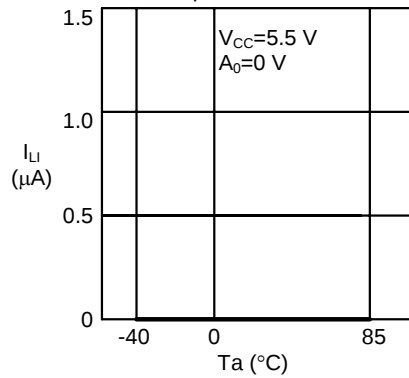
1.19 Standby current I_{SB2} -
Ambient temperature T_a



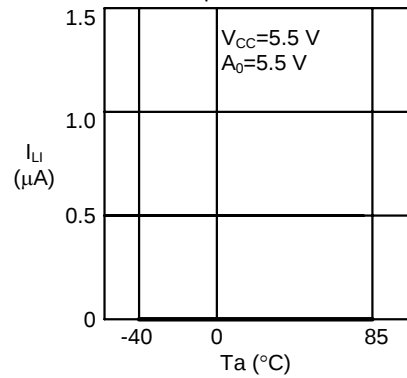
1.20 Standby current I_{SB2} -
Ambient temperature T_a



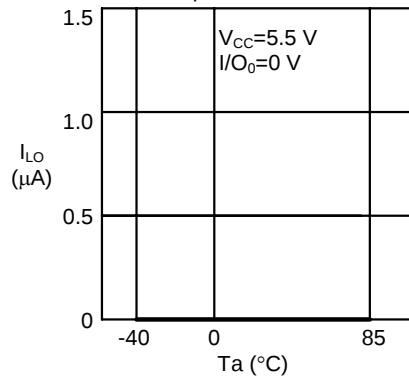
1.21 Input leakage current I_{LI} -
Ambient temperature T_a



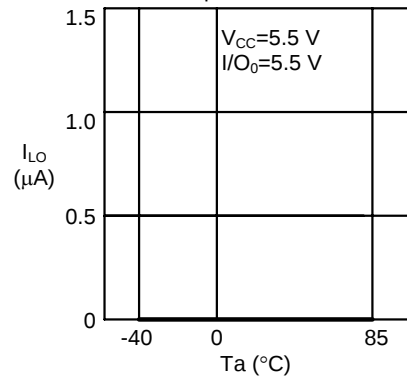
1.22 Input leakage current I_{LI} -
Ambient temperature T_a



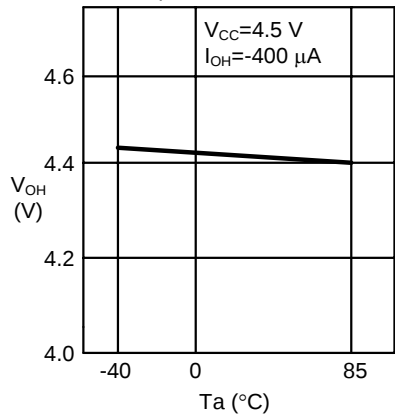
1.23 Output leakage current I_{LO} -
Ambient temperature T_a



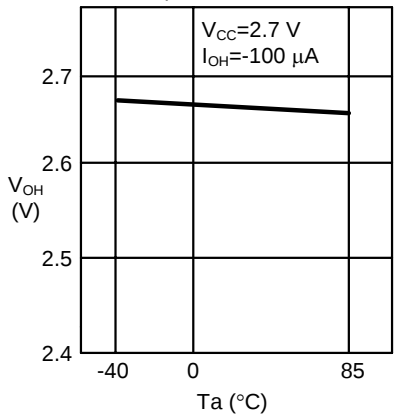
1.24 Output leakage current I_{LO} -
Ambient temperature T_a



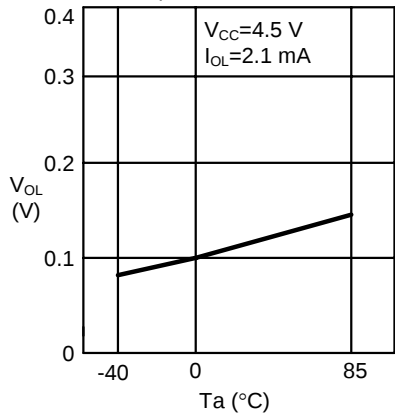
1.25 High level output voltage V_{OH} -
Ambient temperature T_a



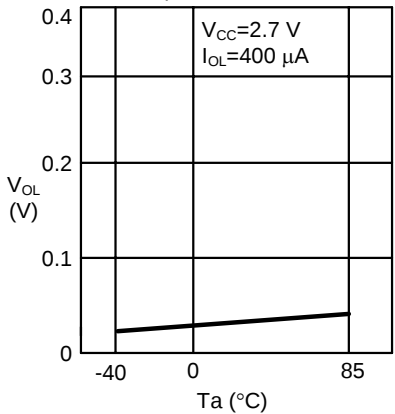
1.26 High level output voltage V_{OH} -
Ambient temperature T_a



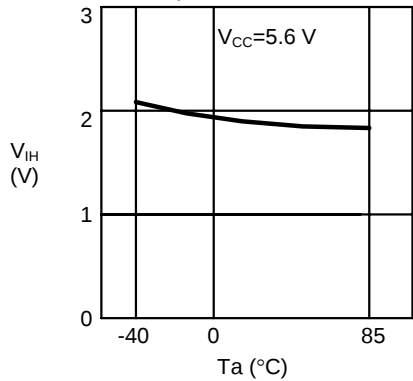
1.27 Low level output voltage V_{OL} -
Ambient temperature T_a



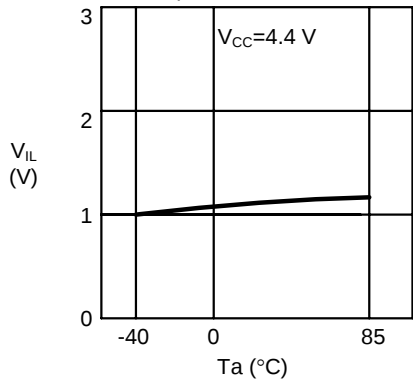
1.28 Low level output voltage V_{OL} -
Ambient temperature T_a



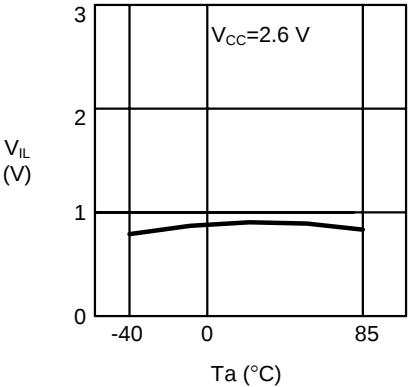
1.29 High level input voltage V_{IH} -
Ambient temperature T_a



1.30 Low level input voltage V_{IL} -
Ambient temperature T_a

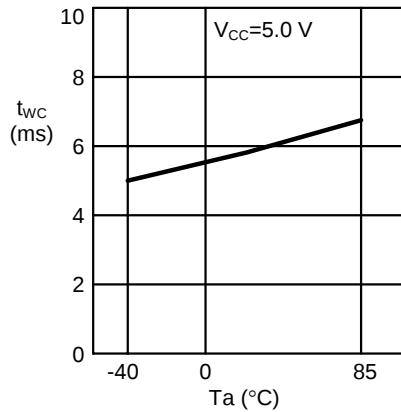


1.31 Low level input voltage V_{IL} -
Ambient temperature T_a

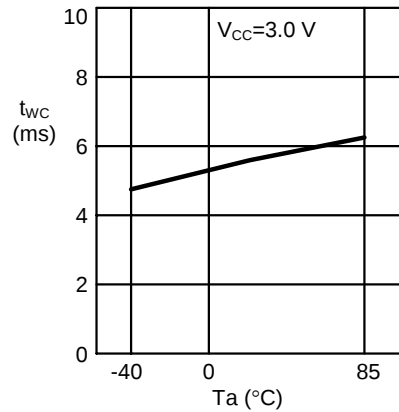


2. AC characteristics

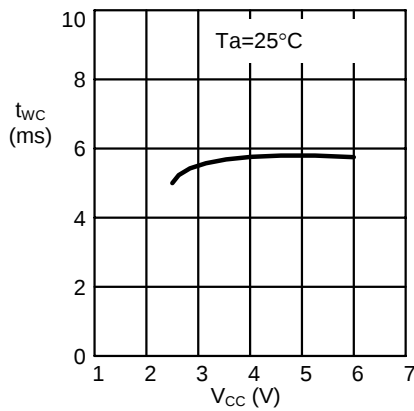
2.1 Write cycle time t_{WC} - Ambient temperature T_a



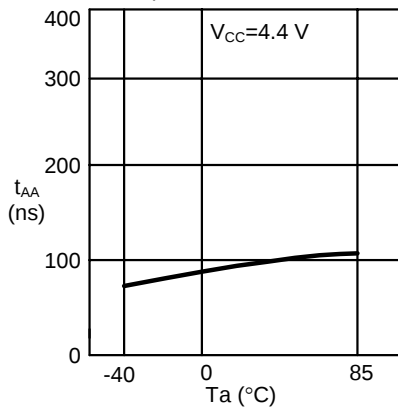
2.2 Write cycle time t_{WC} - Ambient temperature T_a



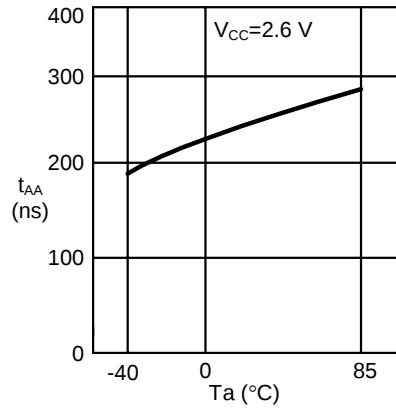
2.3 Write cycle time t_{WC} - Power supply voltage V_{CC}



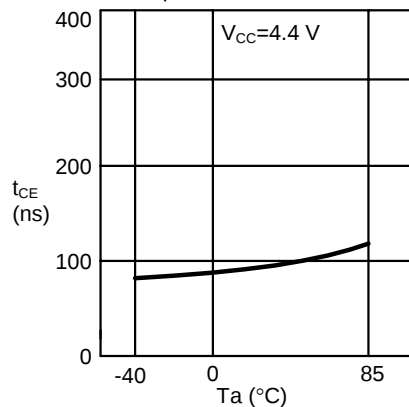
2.4 Address access time t_{AA} - Ambient temperature T_a



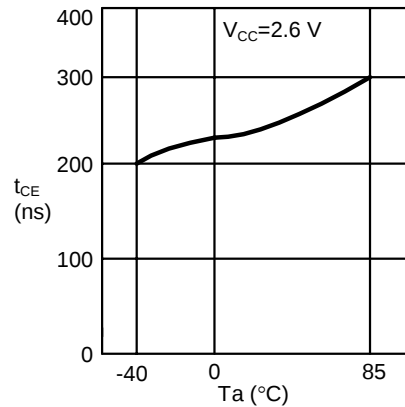
2.5 Address access time t_{AA} - Ambient temperature T_a



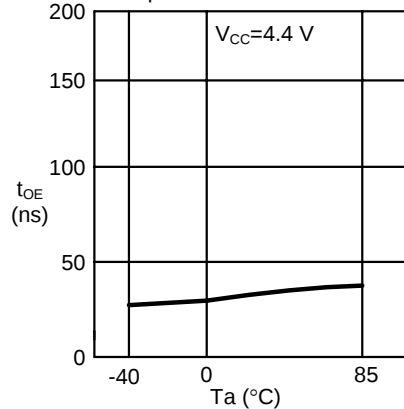
2.6 $\overline{CE}$ access time t_{CE} - Ambient temperature T_a



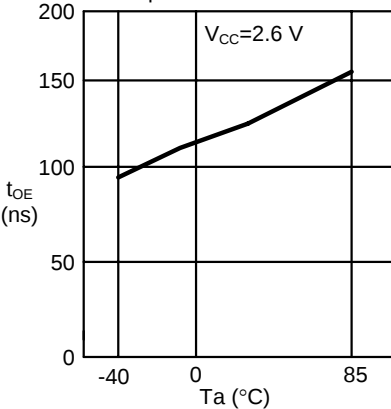
2.7 $\overline{CE}$ access time t_{CE} - Ambient temperature T_a



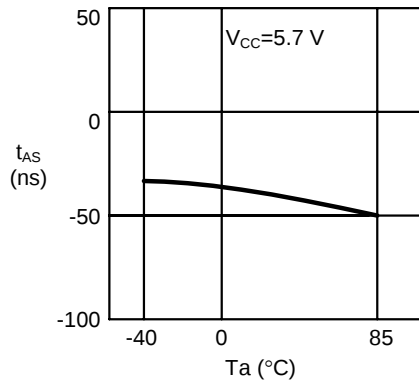
2.8 $\overline{OE}$ access time t_{OE} -
Ambient temperature T_a



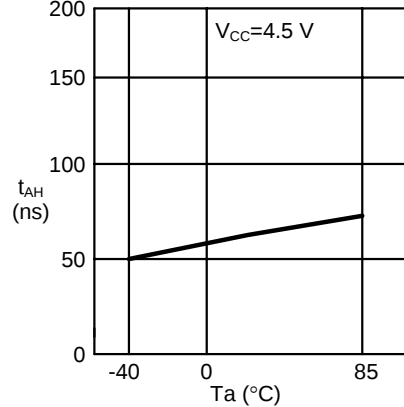
2.9 $\overline{OE}$ access time t_{OE} -
Ambient temperature T_a



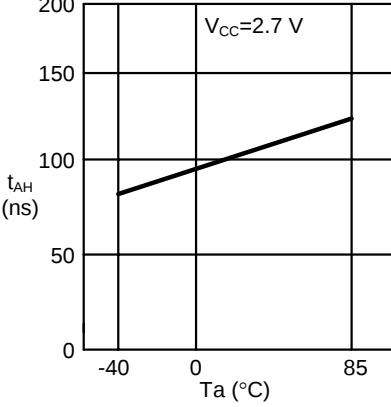
2.10 Address setup time t_{AS} -
Ambient temperature T_a



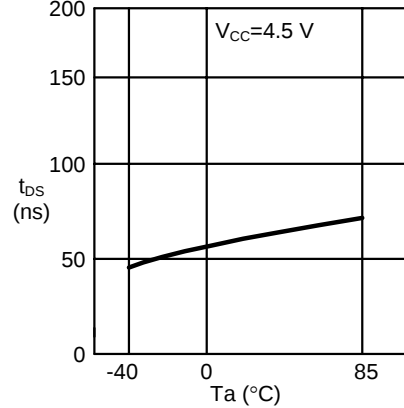
2.11 Address hold time t_{AH} -
Ambient temperature T_a



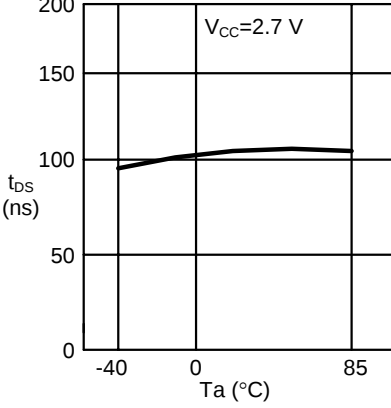
2.12 Address hold time t_{AH} -
Ambient temperature T_a



2.13 Data setup time t_{DS} -
Ambient temperature T_a



2.14 Data setup time t_{DS} -
Ambient temperature T_a



2.15 Data hold time t_{DH} -
Ambient temperature T_a

