SECTION III — OPERATIONAL DATA

POWER SUPPLY CONSIDERATIONS

MECL circuits are characterized with the V_{CC} point at ground potential and the V_{EE} point at –5.2 V. While this MECL convention is not necessarily mandatory, it does result in maximum noise immunity. This is so because any noise induced on the V_{EE} line is applied to the circuit as a common–mode signal which is rejected by the differential action of the MECL input circuit. Noise induced into the V_{CC} line is not cancelled out in this fashion. Hence, a good system ground at the V_{CC} bus is required for best noise immunity. Also, MECL 10H circuits may be operated with V_{EE} at –4.5 V with a negligible loss of noise immunity.

Power supply regulation which will achieve 10% regulation or better at the device level is recommended. The –5.2 V power supply potential will result in best circuit speed. Other values for V_{EE} may be used. A more negative voltage will increase noise margins at a cost of increased power dissipation. A less negative voltage will have just the opposite effect. (Noise margins and performance specifications of MECL 10H are unaffected by variations in V_{EE} because of the internal voltage regulation.)

On logic cards, a ground plane or ground bus system should be used. A bus system should be wide enough to prevent significant voltage drops between supply and device and to produce a low source inductance.

Although little power supply noise is generated by MECL logic, power supply bypass capacitors are recommended to handle switching currents caused by stray capacitance and asymmetric circuit loading. A parallel combination of a 1.0 µF and a 100 pF capacitor at the power entrance to the board, and a 0.01 µF low–inductance capacitor between ground and the –5.2 V line every four to six packages, are recommended.

Most MECL 10H, MECL 10K and MECL III circuits have two V_{CC} leads. V_{CC1} supplies current to the output transistors and V_{CC2} is connected to the circuit logic transistors. The separate V_{CC} pins reduce cross–coupling between individual circuits within a package when the outputs are driving heavy loads. Circuits with large drive capability, similar to the MC10110, have two V_{CC1} pins. All V_{CC} pins should be connected to the ground plane or ground bus as close to the package as possible.

For further discussion of MECL power supply considerations to be made in system designing, see MECL System Design Handbook, HB205.

POWER DISSIPATION

The power dissipation of MECL functional blocks is specified on their respective data sheets. This specification does not include power dissipated in the output devices due to output termination. The omission of internal output pulldown resistors permits the use of external terminations designed to yield best system performance. To obtain total operating power dissipation of a particular functional block in a system, the dissipation of the output transistor, under load, must be added to the circuit power dissipation.

Table 1 lists the power dissipation in the output transistors plus that in the external terminating resistors, for the more commonly used termination values and circuit configurations. To obtain true package power dissipation, one output–transistor power–dissipation value must be added to the specified package power dissipation for each external termination resistor used in conjunction with that package. To obtain system power dissipation, the stated dissipation in the external terminating resistors must be added as well. Unused outputs draw no power and may be ignored.

Table 1 — AVERAGE POWER DISSIPATION IN OUTPUT CIRCUIT WITH EXTERNAL TERMINATING RESISTORS

Terminating Resistor Value	Output Transistor Power Dissipation (mW)	Terminating Resistor Power Dissipation (mW)
150 ohms to –2.0 Vdc	5.0	4.3
100 ohms to –2.0 Vdc	7.5	6.5
75 ohms to –2.0 Vdc	10	8.7
50 ohms to –2.0 Vdc	15	13
2.0 k ohms to V_{EE}	2.5	7.7
1.0 k ohm to V_{EE}	4.9	15.4
680 ohms to V_{EE}	7.2	22.6
510 ohms to V_{EE}	9.7	30.2
270 ohms to V_{EE}	18.3	57.2
82 ohms to V_{CC} and 130 ohms to V_{EE}	15	140

LOADING CHARACTERISTICS

The differential input to MECL circuits offers several advantages. Its common–mode–rejection feature offers immunity against power–supply noise injection, and its relatively high input impedance makes it possible for any circuit to drive a relatively large number of inputs without deterioration of the guaranteed noise margin. Hence, dc fanout with MECL circuits does not normally present a design problem.

Graphs showing typical output voltage levels as a function of load current for MECL 10H, MECL 10K and MECL III shown in Figure 1. These graphs can be used to determine the actual output voltages for loads exceeding normal operation.

While dc loading causes a change in output voltage levels, thereby tending to affect noise margins, ac loading increases the capacitances associated with the circuit and, therefore, affects circuit speed, primarily rise and fall times.

MECL circuits typically have a 7 ohm output impedance and a relatively unaffected by capacitive loading on a positive–going output signal. However, the negative–going edge is dependent on the output pulldown or termination resistor. Loading close to a MECL output pin will cause an additional propagation delay of 0.1 ns per fanout load with a 50 ohm resistor to –2.0 Vdc or 270 ohms to –5.2 Vdc. A 100

ohm resistor to –2.0 Vdc or 510 ohms to –5.2 Vdc results in an additional 0.2 ns propagation delay per fanout load.
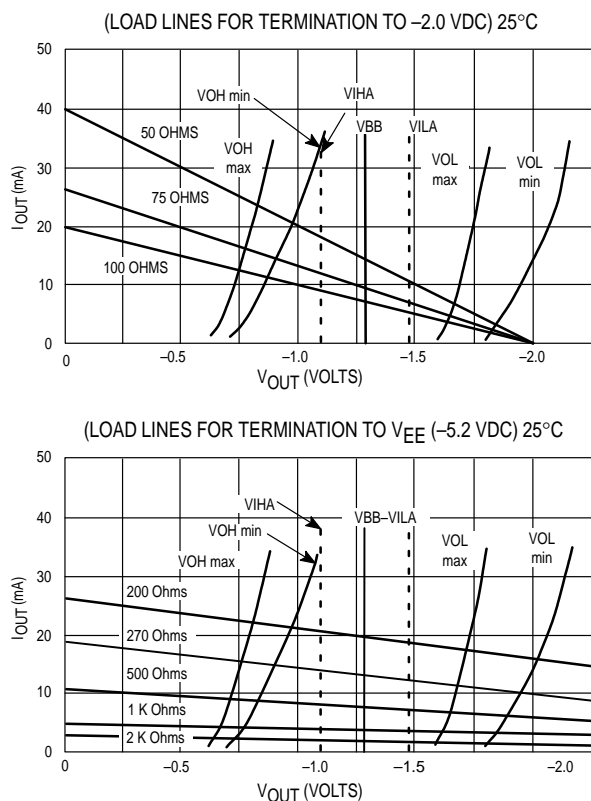
Terminated transmission line signal interconnections are used for best system performance. The propagation delay and rise time of a driving gate are affected very little by capacitance loading along a matched parallel–terminated transmission line. However, the delay and characteristic impedance of the transmission line itself are affected by the distributed capacitance. Signal propagation down the line will be increased by a factor, $\sqrt{1 + C_d/C_O}$. Here C_O is the normal intrinsic line

Figure 1 — OUTPUT VOLTAGE LEVELS versus DC LOADING

(LOAD LINES FOR TERMINATION TO –2.0 VDC) 25°C

(LOAD LINES FOR TERMINATION TO V_{EE} (–5.2 VDC) 25°C

capacitance, and C_d is the distributed capacitance due to loading and stubs off the line.

Maximum allowable stub lengths for loading off of a MECL 10K transmission line vary with the line impedance. For example, with Z_O = 50 ohms, maximum stub length would be 4.5 inches (1.8 in. for MECL III). But when Z_O = 100 ohms, the maximum allowable stub length is decreased to 2.8 inches (1.0 in. for MECL III).

The input loading capacitance of a MECL 10H and MECL 10K gate is about 2.9 pF and 3.3 pF for MECL III. To allow for the IC connector or solder connection and a short stub length, 5 to 7 pF is commonly used in loading calculations.

UNUSED MECL INPUTS

The input impedance of a differential amplifier, as used in the typical MECL input circuit, is very high when the applied signal level is low. Under low–signal conditions, therefore, any leakage to the input capacitance of the gate could cause a gradual buildup of voltage on the input lead, thereby adversely affecting the switching characteristics at low repetition rates.

All single–ended input MECL logic circuits contain input pulldown resistors between the input transistor bases and V_{EE}. As a result, unused inputs may be left unconnected (the resistor provides a sink for I_{CBO} leakage currents, and inputs are held sufficiently negative that circuits will not trigger due to noise coupled into such inputs). Input pulldown resistor values are typically 50 kΩ and are not to be used as pulldown resistors for preceding open–emitter outputs.

Some MECL devices do not have input pulldowns. Examples are the differential line receivers. If a single differential receiver within a package is unused, one input of that receiver must be tied to the V_{BB} pin provided, and the other input goes to V_{EE} or is left open.

MECL circuits do not operate properly when inputs are connected to V_{CC} for a HIGH logic level. Proper design practice is to set a HIGH level about –0.9 volts below V_{CC} with a resistor divider, a diode drop, or an unused gate output.