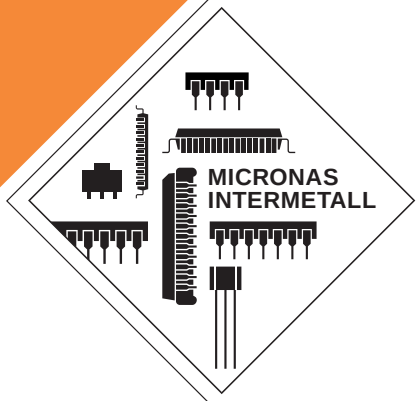


PRELIMINARY DATA SHEET

MSP 3400 C
Multistandard
Sound Processor

Edition Dec. 8, 1997
6251-377-3PD

MICRONAS
INTERMETALL

Contents

Contents, continued

Contents, continued

Multistandard Sound Processor

Release Notes: The hardware description in this document is valid for the MSP 3400C – C8 and newer codes. Revision bars indicate significant changes to the previous version.

1. Introduction

The **MSP 3400C** is designed as single-chip Multistandard Sound Processor for applications in analog and digital TV sets, satellite receivers and video recorders.

The MSP-family, which is based on the MSP 2400, demonstrates the progressive development towards highly integrated multi-functional ICs.

The **MSP 3400C,** again, improves function integration: The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed in a single chip. The IC is produced in 0.8 µm CMOS technology, combined with high performance digital signal processing.

The MSP 3400C 0.8 µ CMOS version is fully pin and software compatible to the 1.0 µ MSP 3400 and MSP 3410. The main difference between the MSP 3400C and the MSP 3410, consists of the MSP 3410 being able to decode NICAM signals.

The MSP 3400C is available in PLCC68, PSDIP64, PSDIP52, and PQFP80 package.

Note: To achieve compatibility with the functions of MSP 3400 and MSP 3410 (except NICAM), the load sequences must be programmed as described in the data sheet of MSP 3410.

MSP 3400C Integrated Functions:

- FM-demodulation of all terrestrial standards (incl. identification decoding)
- FM-demodulation of all satellite standards
- various deemphasis types (incl. Panda1)
- volume, balance, bass, treble, loudness for loudspeaker and headphone output
- automatic volume correction (A.V.C.)
- 5 band graphic equalizer
- subwoofer output alternatively with headphone output
- spatial effect (pseudostereo/basewidth enlargement)
- ADR together with DRP 3510 A
- Dolby ProLogic together with DPL 3418/19/20 A
- 3 pairs of D/A converters
- 1 pair of A/D converters
- SCART switches

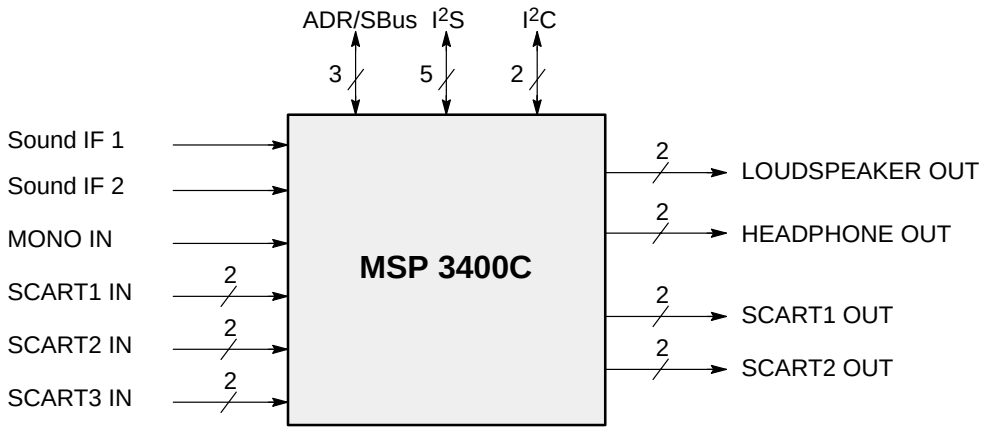


Fig. 1–1: Main I/O Signals MSP 3400C

2. Features of the MSP 3400C

2.1. Features of the Demodulator and Decoder Sections

The MSP 3400C is designed to perform demodulation of FM-mono TV sound and two carrier FM systems according to the German or Korean terrestrial specs. With certain constraints, it is also possible to do AM-demodulation according to the SECAM system. Alternatively, the satellite specs can be processed with the MSP 3400C.

For FM carrier detection in satellite operation, the AM-demodulation offers a powerful feature to calculate the carrier field strength, which can be used for automatic search algorithms. So, the IC facilitates a first step towards multistandard capability with its very flexible application and may be used in TV-sets, satellite tuners, and video recorders.

The MSP 3400C facilitates profitable multistandard capability, offering the following advantages:

– two selectable analog inputs (TV and SAT-IF sources)

– Automatic Gain Control (AGC) for analog input: input range: 0.14 – 3 Vpp

– integrated A/D converter for sound-IF inputs

– all demodulation and filtering is performed on chip and is individually programmable

– no external filter hardware is required

– only one crystal clock (18.432 MHz) is necessary

– FM carrier level calculation for automatic search algorithms and carrier mute function

– high deviation FM-mono mode (max. deviation: approx. ± 360 kHz)

2.2. Features of the DSP-Section

– flexible selection of audio sources to be processed

– digital input and output interfaces via I^2S-Bus for external DSP-processors, surround sound, ADR etc.

– digital interface to process ADR (Astra Digital Radio) together with DRP 3510 A

– performance of all deemphasis systems including adaptive Wegener Panda 1 without external components or controlling

– digitally performed FM-identification decoding and dematrixing

– digital baseband processing: volume, bass, treble, 5-band equalizer, loudness, pseudostereo, and basewidth enlargement

– simple controlling of volume, bass, treble, equalizer etc.

– increased audio bandwidth for FM-Audio-signals (20 Hz – 15 kHz, ± 1 dB)

2.3. Features of the Analog Section

– three selectable analog pairs of audio baseband inputs (= three SCART inputs)
input level: ≤2 V RMS,
input impedance: ≥25 kΩ

– one selectable analog mono input (i.e. AM sound),
input level: ≤2 V RMS,
input impedance: ≥10 kΩ

– two high quality A/D converters, S/N-Ratio: ≥85 dB

– 20 Hz to 20 kHz Bandwidth for SCART-to-SCART-Copy facilities

– MAIN (loudspeaker) and AUX (headphones): two pairs of 4-fold oversampled D/A-converters
output level per channel: max. 1.4 V RMS
output resistance: max. 5 kΩ
S/N-Ratio: ≥85 dB at maximum volume
max. noise voltage in mute mode: ≤10 µV (BW: 20 Hz ...16 kHz)

– one pair of four-fold oversampled D/A-converters supplying two selectable pairs of SCART-Outputs. Output level per channel: max. 2 V RMS, output resistance: max. 0.5 kΩ, S/N-Ratio: ≥85 dB
(20 Hz...16 kHz)

3. Application Fields of the MSP 3400C

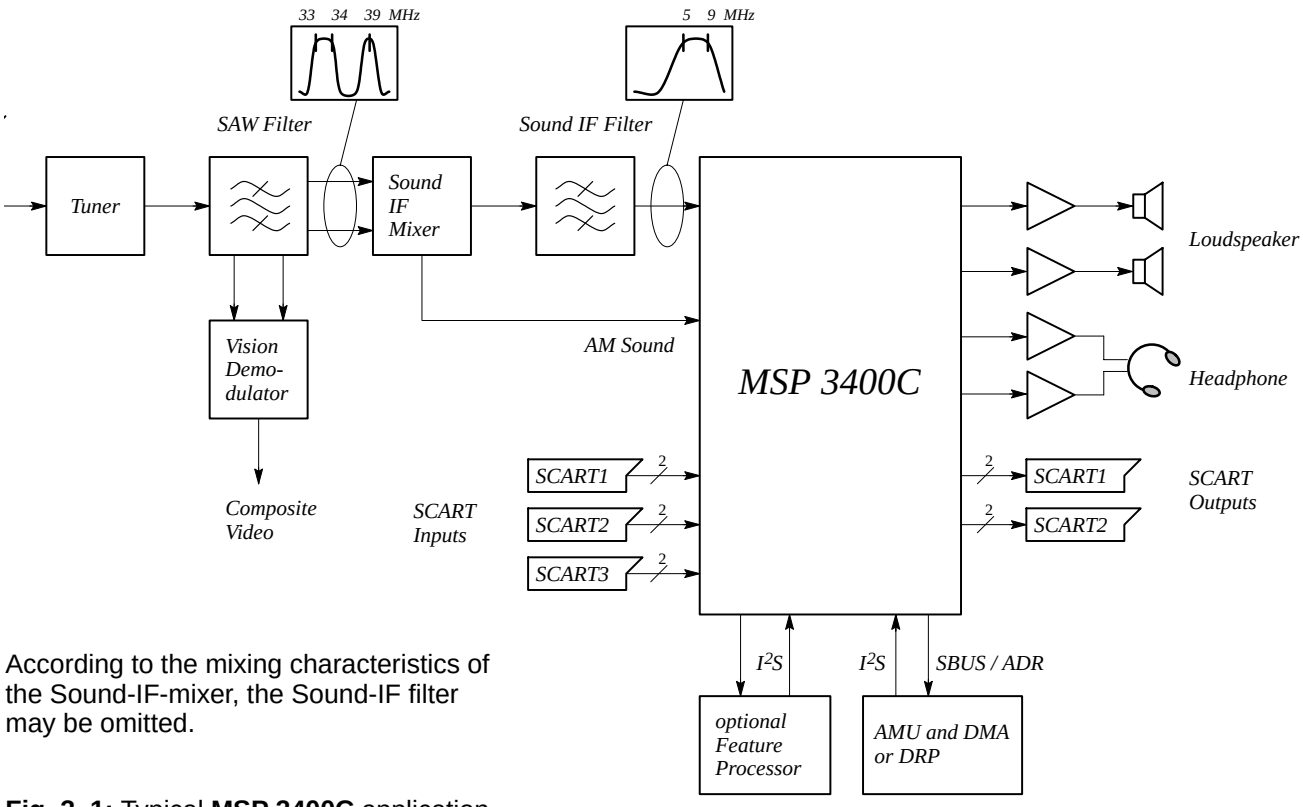
The **MSP 3400C** processes TV sound according to the German and Korean two carrier system and the commonly used satellite systems. In the following sections, a brief overview on the German FM-Stereo system shows what is required of a multistandard audio IC.

3.1. German 2-Carrier System (DUAL FM System)

Since September 1981, stereo and dual sound programs have been transmitted in Germany using the 2-carrier system. Sound transmission consists of the already existing first sound carrier and a second sound carrier additionally containing an identification signal. More details of this standard are given in Table 3–1.

Table 3–1: European TV standards

TV-System	Position of Sound Carrier /MHz	Sound Modulation	Color System	Country
B/G	5.5/5.7421875	FM-Stereo	PAL	Germany
B/G	5.5/5.85	FM-Mono/NICAM	PAL	Scandinavia,Spain
L	6.5/5.85	AM-Mono/NICAM	SECAM-L	France
I	6.0/6.552	FM-Mono/NICAM	PAL	UK
D/K	6.5 /6.2578125 D/K1 6.5/6.7421875 D/K2 6.5/5.85 D/K-NICAM	FM-Stereo FM-Mono/NICAM	SECAM-East	USSR Hungary
M M-Korea	4.5 4.5/4.724212	FM-Mono FM-Stereo	NTSC	USA Korea
Satellite Satellite	6.5 7.02/7.2	FM-Mono FM-Stereo	PAL PAL	Europe (ASTRA) Europe (ASTRA)



According to the mixing characteristics of the Sound-IF-mixer, the Sound-IF filter may be omitted.

Fig. 3–1: Typical **MSP 3400C** application

Table 3–2: Key parameters for B/G, D/K, and M 2-carrier sound system

Sound Carriers	**Carrier FM1**			**Carrier FM2**		
	B/G	D/K	M	B/G	D/K	M
Vision/sound power difference	13 dB			20 dB		
Sound bandwidth	40 Hz to 15 kHz					
Pre-emphasis	50 µs		75 µs	50 µs		75 µs
Frequency deviation	±50 kHz		±25 kHz	±50 kHz		±25 kHz
Sound Signal Components						
Mono transmission	mono			mono		
Stereo transmission	(L+R)/2		(L+R)/2	R		(L–R)/2
Dual sound transmission	language A			language B		
Identification of Transmission Mode on Carrier FM2						
Pilot carrier frequency in kHz				54.6875		55.0699
Type of modulation				AM		
Modulation depth				50%		
Modulation frequency				mono: unmodulated stereo: 117.5 Hz dual: 274.1 Hz		 149.9 Hz 276.0 Hz

Note: NICAM decoding can be achieved by using the MSP 3410 instead of the MSP 3400C. Since the MSP 3400C and the MSP 3410 are fully pin and software downwards compatible (concerning all features of MSP 3410), it is possible to decide in the assembly line, whether the application should be able to decode NICAM or not.

4. Architecture of the MSP 3400C

Fig. 4–1 shows a simplified block diagram of the IC. Its architecture is split into three functional blocks:

1. demodulator section

2. digital signal processing (DSP) section performing audio baseband processing

3. analog section containing two A/D-converters, 6 D/A-converters, and SCART switching facilities

4.1. Demodulator Block

4.1.1. Analog Sound IF – Input Section

The input pins ANA_IN1+, ANA_IN2+, and ANA_IN– offer the possibility to connect two different sound IF sources to the MSP 3400C. By means of bit [8] of AD_CV (see Table 6–3), either terrestrial or satellite sound IF signals can be selected. The analog-to-digital conversion of the preselected sound IF signal is done by a flash-converter, whose output can be used to control an automatic gain circuit (AGC), providing optimum level for a wide range of input levels. It is possible to switch between automatic gain control and a fixed (setable) input gain. In the optimum case, the input range of the A/D converter is completely covered by the sound IF source. Some combinations of SAW filters and sound IF mixer ICs, however, show large picture components on their outputs. In this case, filtering is recommended. It was found that the high pass filters formed by the coupling capacitors at pins ANA_IN1+ and ANA_IN2+ as shown in the application diagram are sufficient in most cases.

4.1.2. Quadrature Mixers

The digital input coming from the integrated A/D converter may contain audio information at a frequency range of theoretically 0 to 9 MHz corresponding to the selected standards. By means of two programmable quadrature mixers two different audio sources, for example FM1 and FM2, may be shifted into baseband position. In the following, the two main channels are provided to process either:

– FM mono (channel 2) or

– FM2 (channel 1) and FM1 (channel 2).

Two independent digital oscillators are provided to generate two pairs of sin/cos-functions. Two programmable increments, to be divided up into Low- and High Part, determine frequency of the oscillator, which corresponds to the frequency of the desired audio carrier. In section 6.1., format and values of the increments are listed.

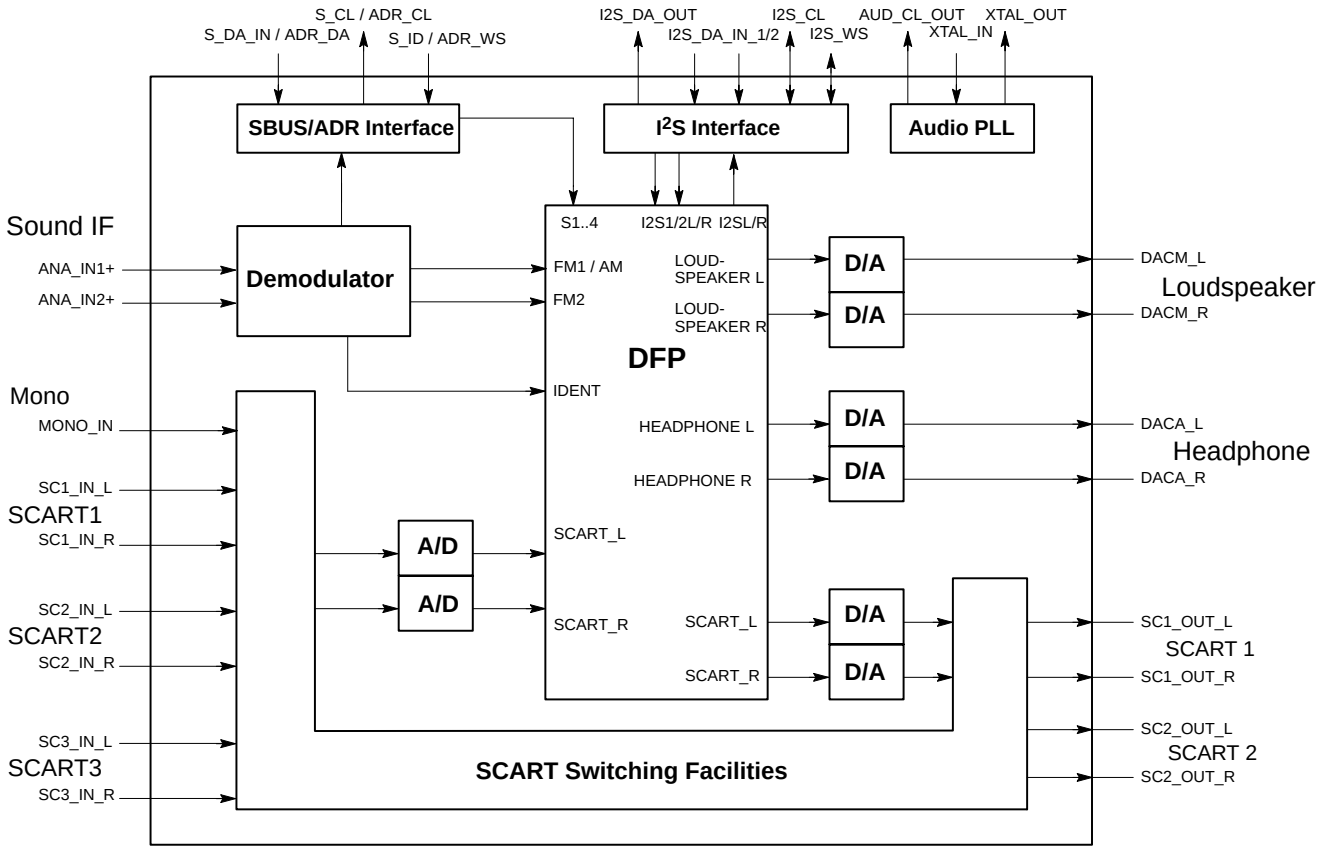


Fig. 4–1: Architecture of the MSP 3400C

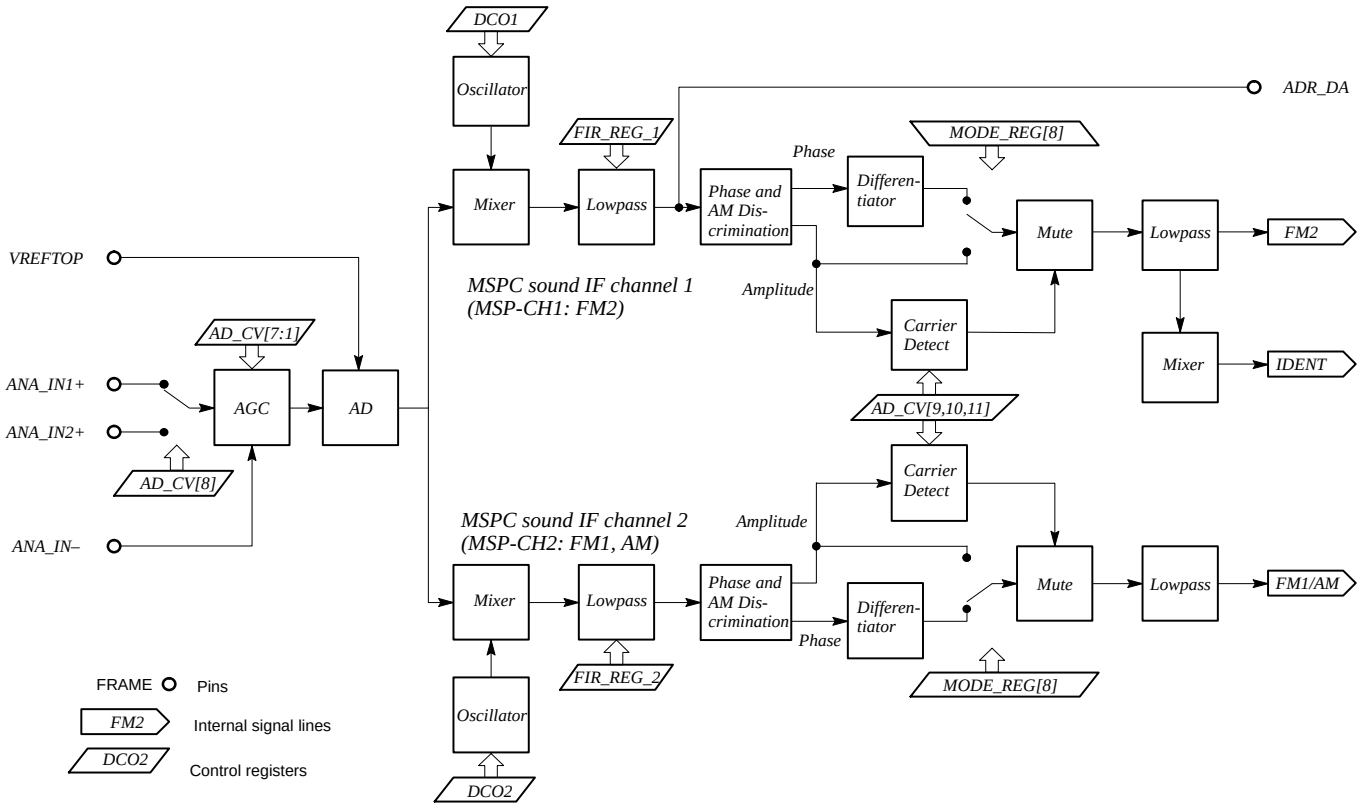


Fig. 4–2: Demodulator architecture

4.1.3. Lowpass Filtering Block for Mixed Sound IF Signals

FM bandwidth limitation is performed by a linear phase Finite Impulse Response (FIR-filter). Just like the oscillators' increments, the filter coefficients are programmable and are written into the IC by the CCU via the control bus. Two not necessarily different sets of coefficients are required, one for channel 1 (FM2) and one for channel 2 (FM1=FM-mono). In section 6.2.4., several coefficient sets are proposed.

4.1.4. Phase and AM Discrimination

The filtered sound IF signals are demodulated by means of the phase and amplitude discriminator block. On the output, the phase and amplitude is available for further processing. AM signals are derived from the amplitude information, whereas the phase information serves for FM demodulation.

4.1.5. Differentiators

FM demodulation is completed by differentiating the phase information output.

4.1.6. Lowpass Filter Block for Demodulated Signals

The demodulated FM and AM signals are further lowpass filtered and decimated to a final sampling frequency of 32 kHz. The usable bandwidth of the final baseband signals is about 15 kHz.

4.1.7. High Deviation FM Mode

By means of MODE_REG [9], the maximum FM-deviation can be extended to approximately ±360 kHz. Since this mode can be applied only for the MSPC sound IF channel 2, the corresponding matrices in the baseband processing must be set to sound A. Apart from this, the coefficient sets 380 kHz FIR_REG2 or 500 kHz FIR_REG2 must be chosen for the FIR_REG_2. For a given deviation, in relation to the normal FM-mode, the audio level of the high-deviation mode is reduced by 6 dB.

4.1.8. MSPC-Mute Function in the Dual Carrier FM Mode

To prevent noise effects or FM identification problems in the absence of one of the two FM carriers, the MSP 3400 C offers a carrier detection feature, which must be activated by means of AD_CV[9]. The mute level may be programmed by means of AD_CV[10,11]. (see section 6.2.1.) If no FM carrier is available at the MSPC channel 1, the corresponding channel FM2 is muted. If no FM carrier is available at the MSPC channel 2, the corresponding channel FM1 is muted. In case of the absence of both FM carriers, pure noise will be amplified by the input AGC. Therefore, a proper mute function depends on the noise quality of the TV set's IF part and cannot be guaranteed. The mute function is not recommended for the satellite mode.

4.2. Analog Section and SCART Switching Facilities

The analog input and output sections offer a wide range of switching facilities, which are shown in Fig. 4–3. To design a TV-set with 3 pairs of SCART-inputs and two pairs of SCART-outputs, no external switching hardware is required.

The switches are controlled by the ACB bits defined in the audio processing interface (see section 7. Programming the Audio Processing Part).

If the MSP 3400C is switched off by first pulling STANDBYQ low, and then disconnecting the 5 V, but keeping the 8 V power supply (**'Standby'-mode**), the switches S1, S2, and S3 maintain their position and function. This facilitates the copying from selected SCART-inputs to SCART-outputs in the TV-sets standby mode.

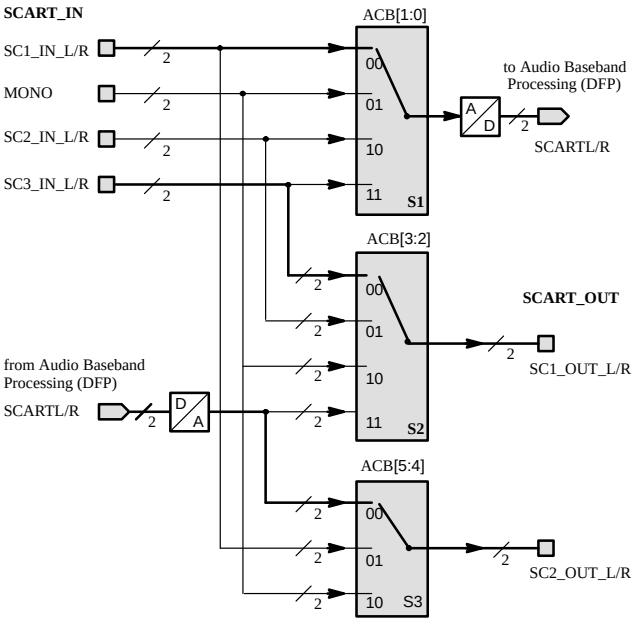


Fig. 4–3: SCART-Switching Facilities
Bold lines determine the default configuration

In case of power-on start or starting from standby, the IC switches automatically to the default configuration, shown in Fig. 4–3. This takes place after the first I^2C transmission into the DFP part. By transmitting the ACB register first, the default setting mode can be changed.

4.3. MSP 3400C Audio Baseband Processing

By means of the DFP processor, all audio baseband functions are performed by digital signal processing (DSP). The DSP functions are grouped into three processing parts: input preprocessing, channel selection, and channel postprocessing.

The input preprocessing is intended to prepare the various signals of all input sources in order to form a standardized signal at the input to the channel selector. The signals can be adjusted in volume, are processed with the appropriate deemphasis, and are dematrixed if necessary.

Having prepared the signals that way, the channel selector makes it possible to distribute all possible source signals to the desired output channels.

The ability to route in an external coprocessor for special effects like surround and sound field processing is of special importance. Routing can be done with each input source and output channel via the I^2S inputs and outputs.

All input and output signals can be processed simultaneously. Note that the NICAM input signals are only available in the MSP 3410 version. While processing the adaptive deemphasis, no dual carrier stereo (German or Korean) is possible. Identification values are not valid either.

4.3.1. Dual Carrier FM Stereo/Bilingual Detection

In the German and Korean TV standard, audio information can be transmitted in three modes: mono, stereo, or bilingual. To obtain information about the current audio operation mode, the MSP 3400C detects the so-called identification signal. Information is supplied via the Stereo Detection Register to an external CCU.

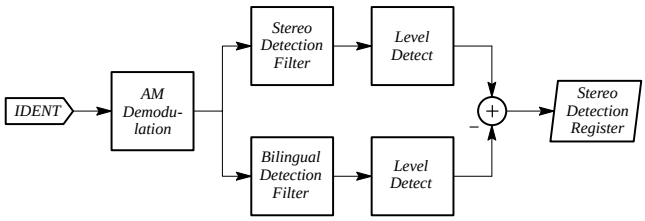


Fig. 4–4: Stereo/bilingual detection

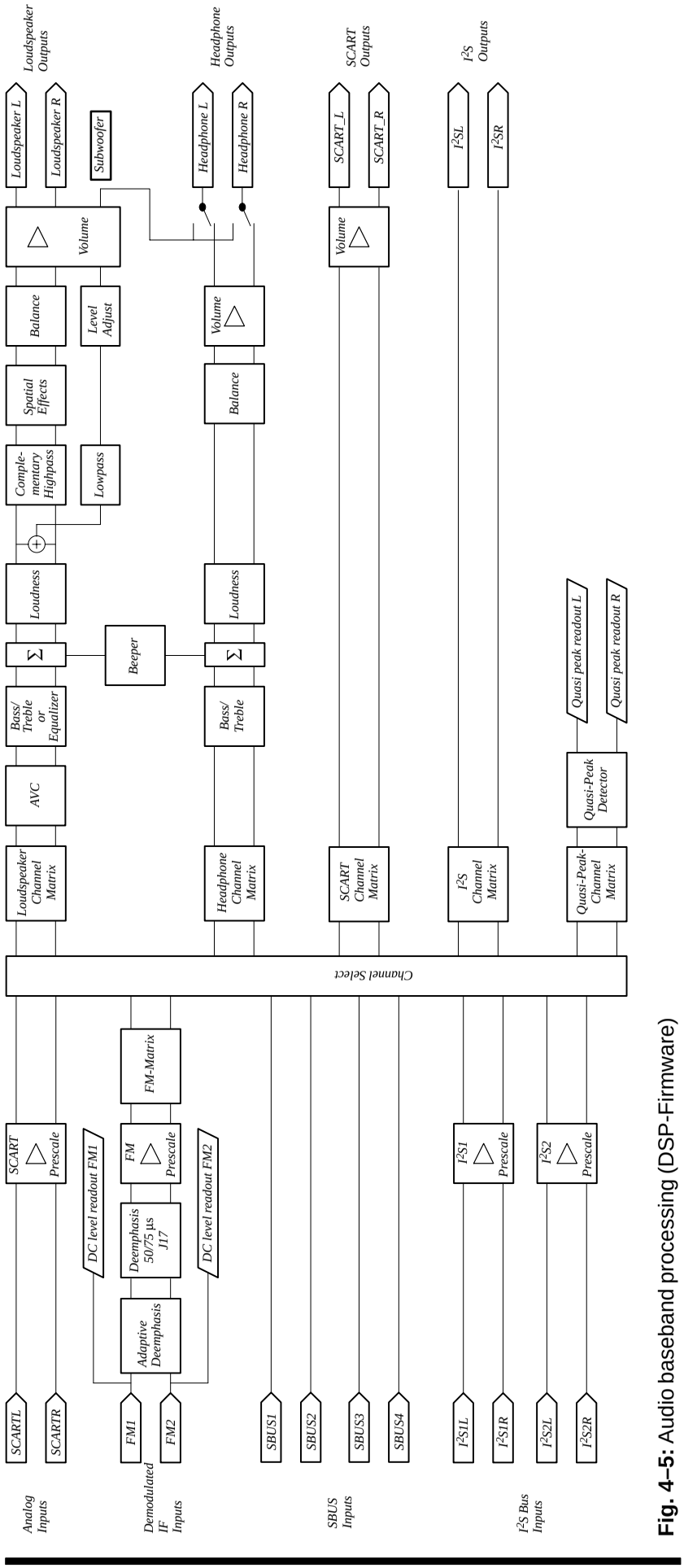


Fig. 4–5: Audio baseband processing (DSP-Firmware)

Table 4–1: Several examples for recommended channel assignments for demodulator and audio processing part

Mode	MSPC Sound IF-Channel 1 / FM2	MSPC Sound IF-Channel 2 / FM1	FM-Matrix	Channel Select	Channel Matrix
B/G-Stereo	FM2 (5.74 MHz): R	FM1 (5.5 MHz): (L+R)/2	B/G Stereo	Speakers: FM	Stereo
B/G-Bilingual	FM2 (5.74 MHz): Sound B	FM1 (5.5 MHz): Sound A	No Matrix	Speakers: FM H.Phone : FM	Speakers: Sound A H.Phone : Sound B
Sat-Mono	not used	FM (6.5 MHz): mono	No Matrix	Speakers: FM	Sound A
Sat-Stereo	7.20 MHz: R	7.02 MHz: L	No Matrix	Speakers: FM	Stereo
Sat-Bilingual	7.38 MHz: Sound C	7.02 MHz: Sound A	No Matrix	Speakers: FM H.Phone : FM	Speakers: Sound A H.Phone :Sound B=C
Sat High Dev. Mode (e.g. EutelSat)	don't care	6.552 MHz	No Matrix	Speakers: FM H.Phone : FM	Speakers: Sound A H.Phone : Sound A

4.4. Audio PLL and Crystal Specifications

The MSP 3400C runs at 18.432 MHz. A detailed specification of the required crystal for different packages and master/slave applications can be found in Table 8.5.2. The clock supply of the entire system depends on the MSP 3400C operation mode:

1. FM-Stereo/I^2S Master operation:
The system clock runs free on the crystal's 18.432 MHz.

2. I^2S Slave operation:
In this case, the system clock is synchronizing on the I^2S_WS signal, which is fed into the MSP 3400C (Mode_Reg[3] = 1).

3. D2-MAC operation:
In this case, the system clock is locked to a synchronizing signal (DMA_SYNC) supplied by the D2-MAC chip (Mode_Reg[0] = 1). The DMA and the AMU chips can be driven by the MSP 3400C audio clock (AUD_CL_OUT).

Remark on using the crystal:
External capacitors at each crystal pin to ground are required. They are necessary for tuning the open-loop frequency of the internal PLL and for stabilizing the frequency in closed-loop operation. The higher the capacitors, the lower the clock frequency results. The nominal free running frequency should match the center of the tolerance range between 18.433 and 18.431 MHz as closely as possible. Due to different layouts of customer PCBs, the matching capacitor size should be defined in the application (see also Table 8.5.2.).

4.5. ADR Bus

To be able to process ADR, the MSPC has a special designed interface to work together with DRP 3510A. To be prepared for an upgrade to ADR with an additional DRP board, the following lines of MSP 3400C should be provided on a feature connector:

– AUD_CL_OUT

– I^2S_DA_IN1 or I^2S_DA_IN2

– I^2S_DA_OUT

– I^2S_WS

– I^2S_CLK

– S_CL = ADR_CL

– S_ID = ADR_WS

– S_DA_IN = ADR_DA

4.6. S-Bus Interface

Digital audio information provided by the DMA 2381 via the AMU is serially transmitted to the MSP 3400C via the S-Bus. The MSP 3400C is always in S-Bus master mode.

The S-Bus interface consists of three pins:

1. S_DA_IN:
Four channels (4*16 bits) per sampling cycle (32 kHz) are transmitted.

2. S_CL:
Gives the timing for the transmission of S-DATA (4.608 MHz).

3. S_ID:
After 64 S-CLOCK cycles, the S_ID determines the end of one sampling period.

A detailed timing diagram is shown in Fig. 4–6.

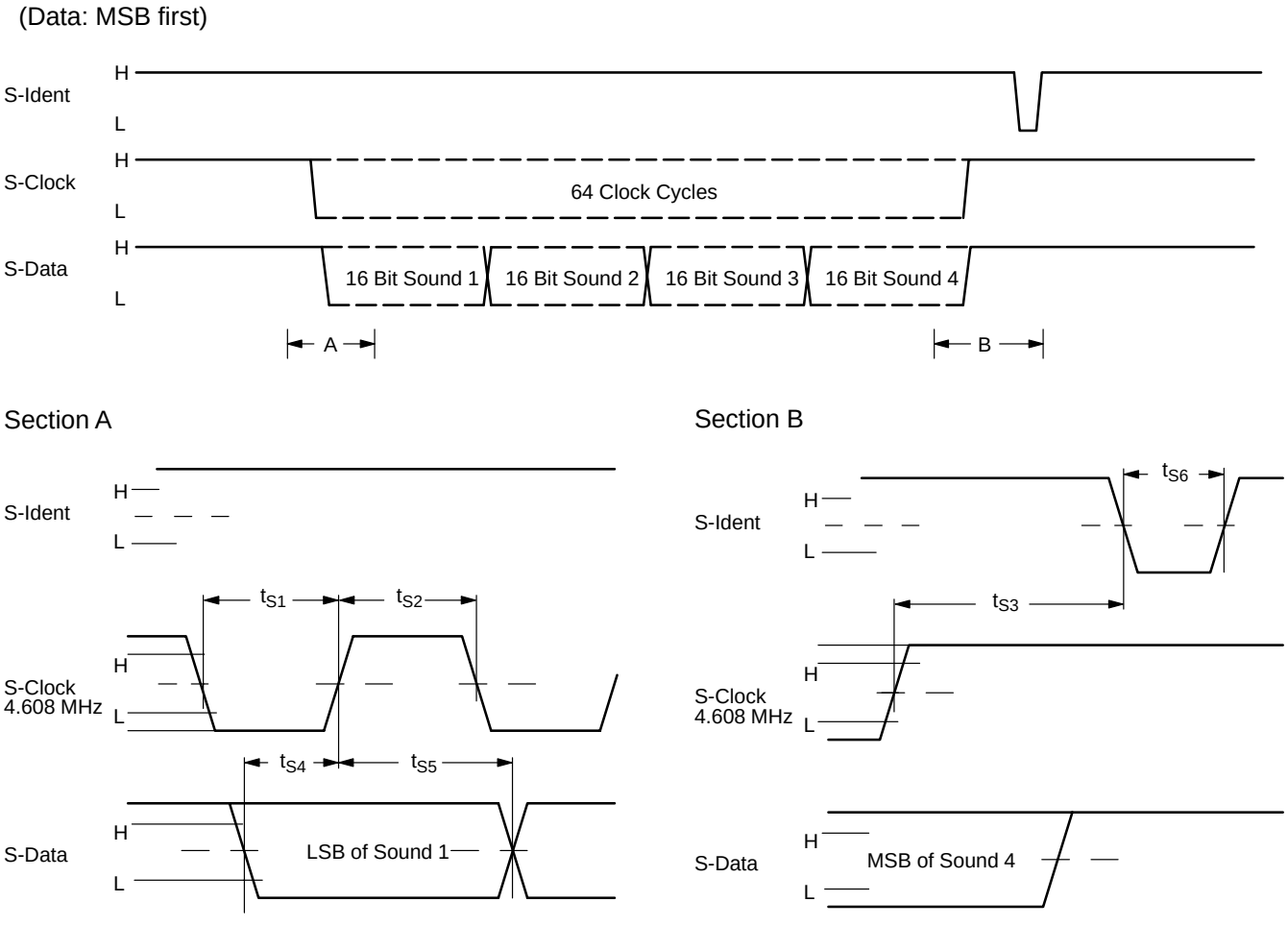


Fig. 4–6: S-Bus timing diagram

4.7. I²S Bus Interface

By means of this standardized interface, additional feature processors can be connected to the MSP 3400C. Two possible formats are supported: The standard mode (MODE_REG[4]=0) selects the SONY format, where the I2S_WS signal changes at the word boundaries. The so-called PHILIPS format, which is characterized by a change of the I2S_WS signal, one I2S_CL period before the word boundaries, is selected by setting MODE_REG[4]=1.

The MSP 3400C normally serves as the master on the I²S interface. Here, the clock and word strobe lines are driven by the MSP 3400C. By setting MODE_REG[3]=1, the MSP 3400C is switched to a slave mode. Now, these lines are input to the MSP 3400 C, and the master clock is synchronized to 576 times the I2S_WS rate (32 kHz). No D2MAC operation is possible in this mode.

The I²S bus interface consists of five pins:

1. I2S_DA_IN1:
For input, two channels (2*16 bits) per sampling cycle (32 kHz) are transmitted.

2. I2S_DA_IN2:
For input, two channels (2*16 bits) per sampling cycle (32 kHz) are transmitted.

3. I2S_DA_OUT:
For output, two channels (2*16 bits) per sampling cycle (32 kHz) are transmitted.

4. I2S_CL:
Gives the timing for the transmission of I²S serial data (1.024 MHz).

5. I2S_WS:
The I2S_WS word strobe line defines the left and right sample.

A detailed timing diagram is shown in Fig. 4–7.

Data: MSB first)

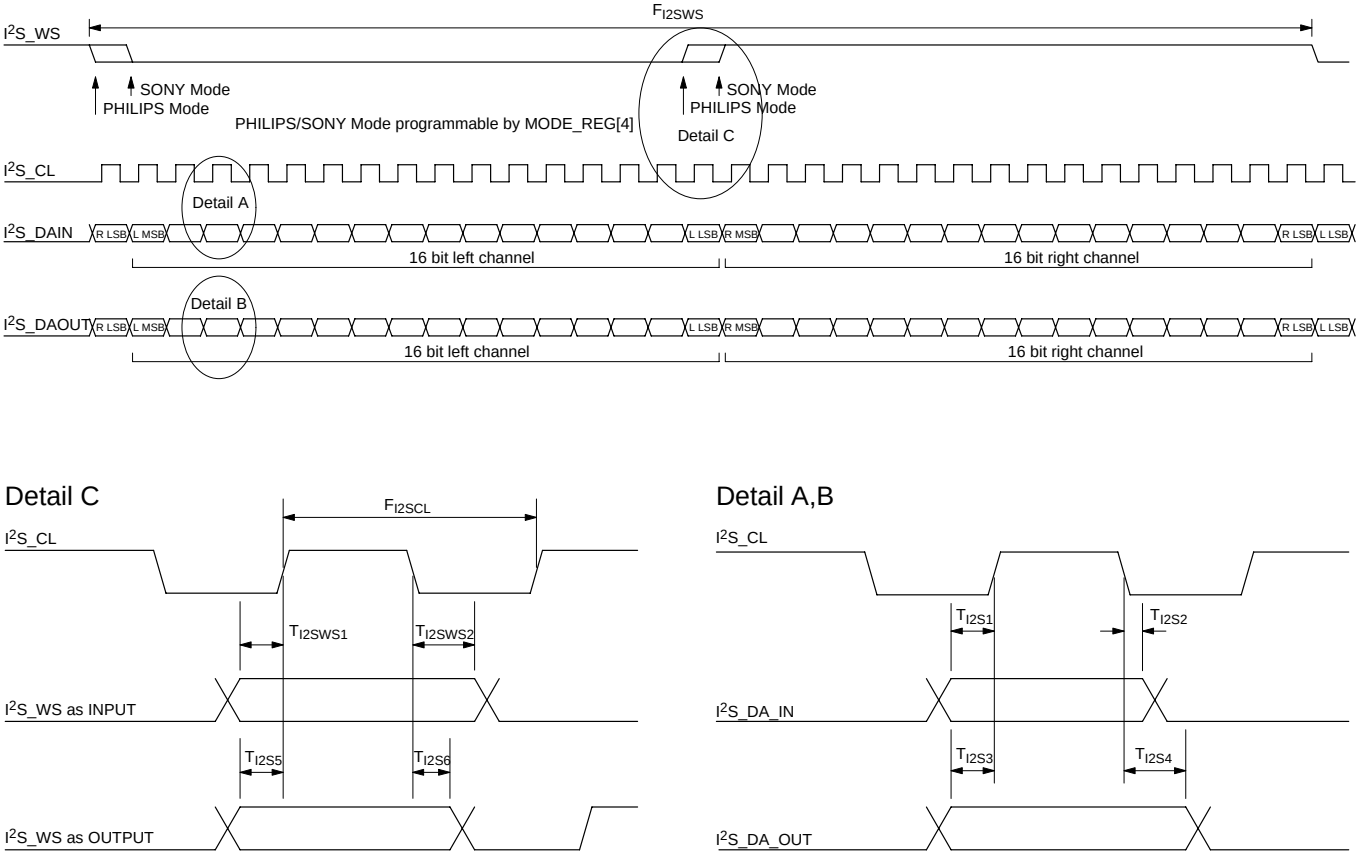


Fig. 4–7: I²S Bus timing diagram

5. I²C Bus Interface: Device and Subaddresses

As a slave receiver, the MSP 3400C can be controlled via I²C bus. Access to internal memory locations is achieved by subaddressing. The demodulator part and the audio processor part (DFP) have two separate subaddressing register banks.

In order to allow for more MSP 3400C ICs to be connected to the control bus, an ADR_SEL pin has been implemented. With ADR_SEL pulled to high, the MSP 3400C responds to changed device addresses, thus two identical devices can be selected. Other devices of the same family will have different subaddresses (e.g. 34x0)

By means of the RESET bit in the CONTROL register, all devices with the same device address are reset.

The IC is selected by asserting a special device address in the address part of an I²C transmission. A device address pair is defined as a write address (80 hex or 84 hex) and a read address (81 hex or 85 hex). Writing is done by sending the device write address first, followed by the subaddress byte, two address bytes, and two data bytes. For reading, the read address has to be transmitted first by sending the device write address (80 hex or 84 hex), followed by the subaddress byte, and two address bytes. Without sending a stop condition, reading of the addressed data is done by sending the device read address (81 hex or 85 hex) and reading two bytes of data. Refer to Fig. 5–1 I²C Bus Protocol and section 5.2. Proposal for MSP 3400C I²C Telegrams.

Due to the internal architecture of the MSP 3400C, the IC cannot react immediately to an I²C request. The typical response time is about 0.3 ms. If the addressed processor is not ready for further transmissions on the I²C bus, the clock line I2C_CL is pulled low. This puts the current transmission into a wait state. After a certain period of time, the MSP 3400C releases the clock, and the interrupted transmission is carried on.

The I²C Bus lines can be set tristate by switching the IC into “Standby”-mode.

I²C-Bus error conditions:
In case of any internal error, the MSP’s wait-period is extended to 1.77 ms. Afterwards, the MSP does not acknowledge (NAK) the device address. The data line will be left HIGH by the MSP, and the clock line will be released. The master can then generate a STOP condition to abort the transfer.

By means of NAK, the master is able to recognize the error state and to reset the IC via I²C-Bus. While transmitting the reset protocol (section. 5.2.4.) to ‘CONTROL’, the master must ignore the not acknowledge bits (NAK) of the MSP.

A detailed timing diagram is shown in Fig. 5–1 and Fig. 5–2.

Table 5–1: I²C Bus Device Addresses

ADR_SEL	Low		High		Left Open	
Mode	**Write**	**Read**	**Write**	**Read**	**Write**	**Read**
MSP device address	80 hex	81 hex	84 hex	85 hex	88 hex	89 hex

Table 5–2: I²C Bus Device and Subaddresses

Name	Binary Value	Hex Value	Function
CONTROL	0000 0000	00	software reset
TEST1	0000 0001	01	only for internal use
TEST2	0000 0010	02	only for internal use
WR_DEM	0001 0000	10	write address demodulator
RD_DEM	0001 0001	11	read address demodulator
WR_DFP	0001 0010	12	write address DFP
RD_DFP	0001 0011	13	read address DFP
AGC	0001 1110	1E	read AGC RMS
PLL_CAP	0001 1111	1F	read / write PLL_Cap

Table 5–3: Control Register

Name	15	14..0
CONTROL	RESET	0

5.1. Protocol Description

Write to DFP or Demodulator Part (long protocol)

S	daw	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	data-byte high	ACK	data-byte low	ACK	P

Read from DFP Part (long protocol)

S	daw	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	S	dar	Wait	ACK	data-byte high	ACK	data-byte low	NAK	P

Write to Control / Test / AGC / PLL_Cap Registers (short protocol)

S	daw	Wait	ACK	sub-addr	ACK	data-byte high	ACK	data-byte low	ACK	P

Read from Control / Test / AGC / PLL_Cap Registers (short protocol)

S	daw	Wait	ACK	sub-addr	ACK	S	dar	Wait	ACK	data-byte high	ACK	data-byte low	NAK	P

Note: S = I^2C-Bus Start Condition from master
P = I^2C-Bus Stop Condition from master
daw = Device Address Write
dar = Device Address Read
ACK = Acknowledge-Bit: LOW on I2C_DA from slave (= MSPC, grey) or master (= CCU, hatched)
NAK = Not Acknowledge-Bit: HIGH on I2C_DA from master (= CCU, hatched) to indicate 'End of Read' or from MSPC indicating internal error state (not illustrated)
Wait = I^2C-Clock line held low by the slave (= MSPC) while interrupt is serviced (<1.77 ms)

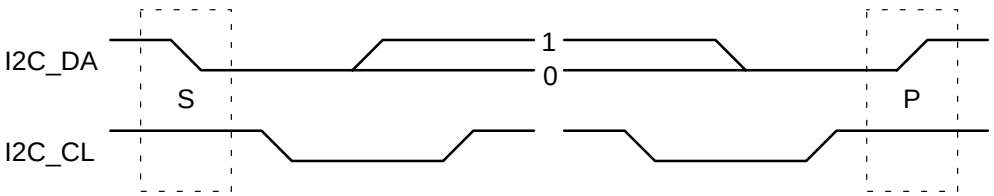


Fig. 5–1: I^2C bus protocol (MSB first; data must be stable while clock is high)

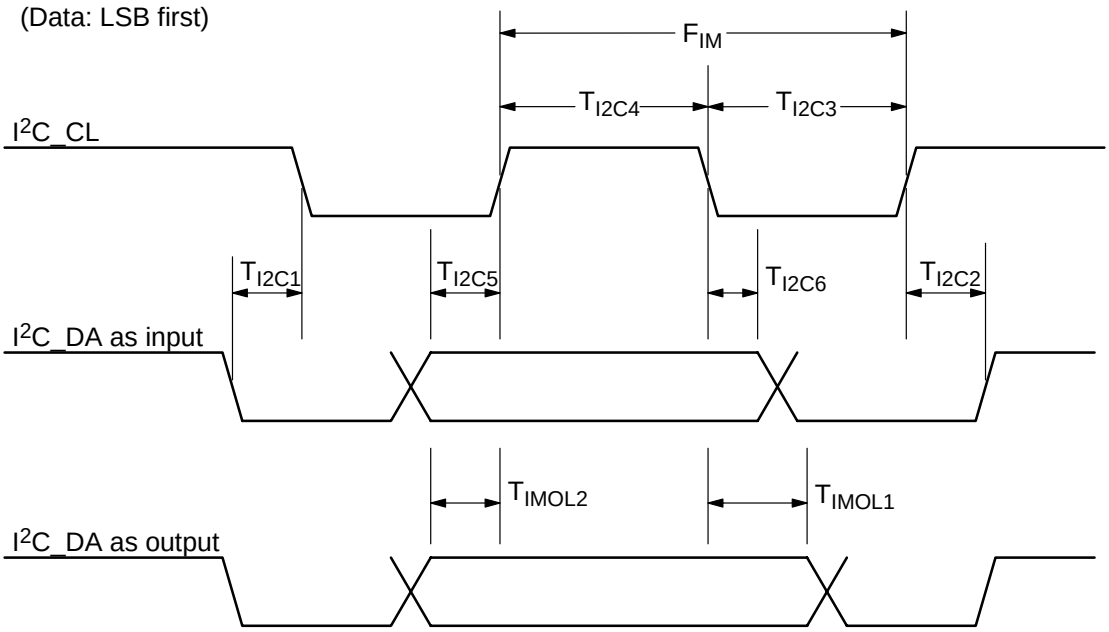


Fig. 5–2: I²C bus timing diagram

5.2. Proposal for MSP 3400C I²C Telegrams

5.2.1. Symbols

daw	device address write
dar	device address read
<	Start Condition
>	Stop Condition
aa	Address Byte
dd	Data Byte

5.2.2. Write Telegrams

`<daw 00 dd dd>`	software RESET
`<daw 10 aa aa dd dd>`	write data into demodulator register
`<daw 12 aa aa dd dd>`	write data into DFP register

5.2.3. Read Telegrams

`<daw 11 aa aa <dar dd dd>`	read data from demodulator
`<daw 13 aa aa <dar dd dd>`	read data from DSP

5.2.4. Examples

`<daw 00 80 00>`	RESET MSPC statically
`<daw 00 00 00>`	clear RESET
`<daw 12 00 08 00 20>`	set loudspeaker channel source to FM and Matrix to STEREO

5.3. Start Up Sequence

After power on or RESET, the IC is in an inactive state. The CCU has to transmit the required coefficient set for a given operation via the I^2C bus. Initialization must start with the demodulator part. If required for any reason, the audio processing part can be loaded before the demodulator part.

The reset pin should not be >0.45 DVSUP (see recommended operation conditions) before the 5 Volt digital power supply (DVSUP) and the analog power supply (AVSUP) are >4.75 Volt **and** the MSP-Clock is running (Delay: 2 ms max, 0.5 ms typ.).

This means, if the reset low-high edge starts with a delay of 2 ms after DVSUP>4.75 Volt and AVSUP>4.75 Volt, even under worst case conditions, the reset is ok.

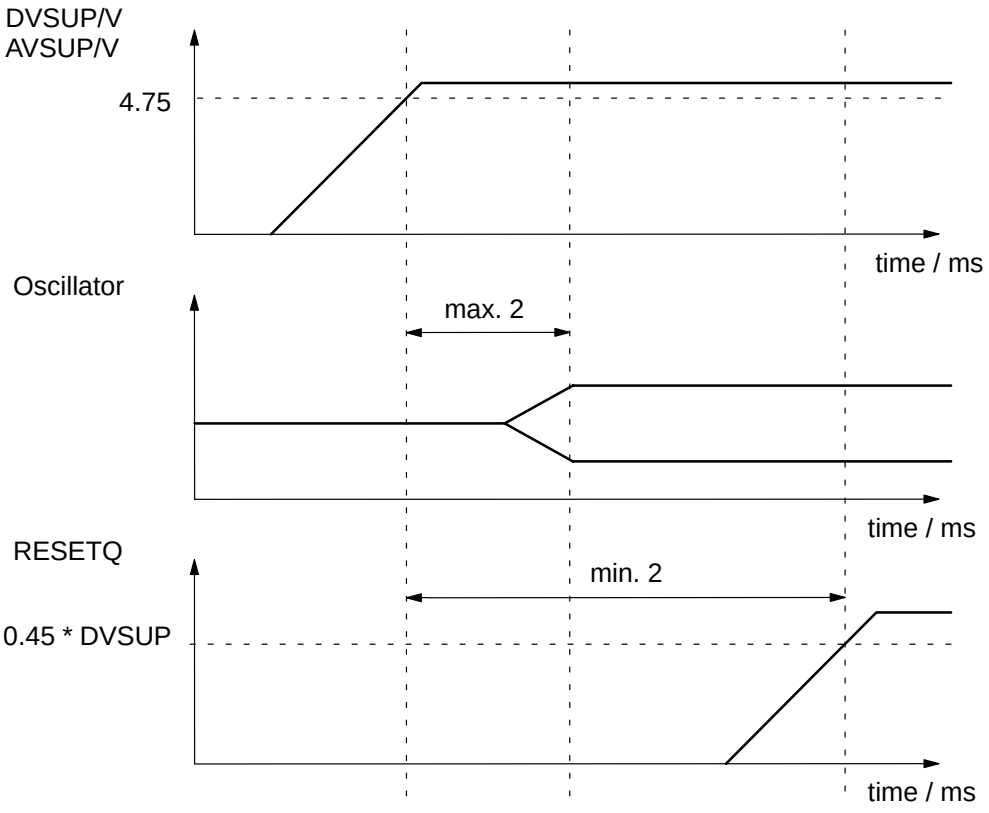


Fig. 5–3: Power-up sequence

Note: The reset should not reach high level before the oscillator has started. This requires a reset delay of >2 ms

6. Programming the Demodulator Part

6.1. Registers: Table and Addresses

In Table 6–1, all Write Registers are listed.

All transmissions on the control bus are 16 bits wide. Data for the demodulator part has 8 or 12 significant bits. These data have to be inserted LSB bound and filled with zero bits into the 16 bit transmission word. If channel 1 or channel 2 is selected in the channel matrix while any of the parameters are changed, the corresponding output must be muted. Click and crack noise may occur during coefficient changes. Table 4–1 explains how to assign FM carriers to the MSPC-Sound IF channels and the corresponding matrix modes in the audio processing part.

Table 6–1: MSP 3400C demodulator write registers

Register	Protocol	Write Address (hex)	Function
AD_CV	long	00BB	input selection, configuration of AGC and Mute Function, and selection of A/D-converter
MODE_REG	long	0083	mode register
FIR_REG_1 FIR_REG_2	long long	0001 0005	serial shift register for 6 · 8 bit, filter coefficient channel 1 (48 bit) serial shift register for 6 · 8 bit, + 2 · 12 bit off set (total 72 bit)
DCO1_LO DCO1_HI DCO2_LO DCO2_HI	long long long long	0093 009B 00A3 00AB	increment channel 1 Low Part increment channel 1 High Part increment channel 2 Low Part increment channel 2 High Part
PLL_CAP[1)]	short	1F	switchable PLL capacities

Table 6–2: MSP 3400C demodulator read registers

Register	Protocol	Read Address (hex)	Function
PLL_CAP[1)]	short	1F	switchable PLL capacities
AGC_RMS[1)]	short	1E	RMS value, comparable with reference value
C_AD_BITS	long	0023	A read from this address always responds with 0. This ensures software compatibility with the MSP 3410 readout. Reading 0 from this register signals “No NICAM”.

[1)] The registers PLL_CAP and AGC_RMS are only available in MSP 3400C. In MSP 3410 and MSP 34x0D, this register cannot be accessed.

6.2. Registers: Functions and Values

In the following, the functions of several registers are explained and their (default) values are defined.

6.2.1. Setting of Parameter AD_CV

Table 6–3: AD_CV Register

AD_CV Bit Range	Meaning	Settings
AD_CV [0]	not used	must be set to 0
AD_CV [6:1]	Reference level in case of Automatic Gain Control = on. Constant gain factor when Automatic Gain Control = off .	see Table 6–5 see Table 6–6
AD_CV [7]	Determination of Automatic Gain or Constant Gain	0 = constant gain 1 = automatic gain
AD_CV [8]	Selection of analog input	0 = ANALOG IN1 1 = ANALOG IN2
AD_CV [9]	MSPC-Carrier-Mute Function	0 = off: no mute 1 = on: mute (see section 4.1.8.)
AD_CV [11–10]	Programmable Carrier-Mute Level	see Table 6–4
AD_CV [15–12]	not used	must be set to 0

Table 6–4: Carrier Mute Level

Step	AD_CV [11:10] binary	AD_CV [11:10] decimal	Internal reference level for mute active (dBr: relative to MSP 3410)
0	00	0	0 dBr
1	01	1	–3 dBr
2	10	2	–6 dBr
3	11	3	–12 dBr

Table 6–5: Reference values AD_CV [6:1] for active AGC (AD_CV[7] = 1)

Application	Input Signal Contains	Ref. Value binary	Ref. Value decimal	Range of Input Signal at pin ANA_IN_1+ and ANA_IN_2+
Terrestrial TV	2 FM Carriers	101000	40	0.14 – 3 V_{pp}[1)]
SAT	1 or more FM Carriers	100011	35	0.14 – 3 V_{pp}[1)]
ADR	1 or more FM Carriers and 1 or more ADR Carriers	010100	20	0.14 – 3 V_{pp}[1)]

[1)] For signals above 1.4 Vpp, the minimum gain of 3 dB is switched and overflow of the AD converter may result. Due to the robustness of the internal processing in FM mode, the IC works properly up to and even more than 3 Vpp. In AM mode, of course, no AD converter overflow is allowed. As a consequence, in the AM-mode, the maximum input at pins 41 or 43 must not exceed 1.4 Vpp.

Table 6–6: AD_CV parameters for constant input gain (AD_CV[7]=0)

Step	AD_CV [6:1] Constant Gain	Gain	Input Level at pin ANA_IN1+ and ANA_IN2+
0	000000	3.00 dB	maximum input level[1)]: 3 V_{pp} (FM) or 1.4 V_{pp} (AM)
1	000001	3.85 dB	
2	000010	4.70 dB	
3	000011	5.55 dB	
4	000100	6.40 dB	
5	000101	7.25 dB	
6	000110	8.10 dB	
7	000111	8.95 dB	
8	001000	9.80 dB	
9	001001	10.65 dB	
10	001010	11.50 dB	
11	001011	12.35 dB	
12	001100	13.20 dB	
13	001101	14.05 dB	
14	001110	14.90 dB	
15	001111	15.75 dB	
16	010000	16.60 dB	
17	010001	17.45 dB	
18	010010	18.30 dB	
19	010011	19.15 dB	
20	010100	20.00 dB	maximum input level: 0.14 V_{pp}[1)]

[1)] For signals above 1.4 Vpp, the minimum gain of 3 dB is switched and overflow of the AD converter may result. Due to the robustness of the internal processing in FM mode, the IC works properly up to and even more than 3 Vpp. In AM mode, of course, no AD converter overflow is allowed. As a consequence, in the AM-mode, the maximum input at pins 41 or 43 must not exceed 1.4 Vpp.

6.2.2. Control Register ‘MODE_REG’

The register ‘MODE_REG’ contains the control bits determining the operation mode of the MSP 3400C; Table 6–7 explains all bit positions.

Table 6–7: Control word ‘MODE_REG’: All bits are “0” after power-on-reset

Bit	Function	Comment	Definition	Recommendation
[0]	DMA_SYNC[1)]	Synchronization to DMA	0 : off 1 : on	X
[1]	DCTR_TRI	Digital control out 0/1 tristate	0 : active 1 : tristate	0
[2]	I2S_TRI	I^2S outputs tristate (I2S_CL, I2S_WS, I2S_DA_OUT)	0 : active 1 : tristate	0
[3]	I^2S Mode[1)]	Master/Slave mode of the I^2S bus	0 : Master 1 : Slave	X
[4]	I^2S_WS Mode	WS due to the Sony or Philips-Format	0 : Sony 1 : Philips	X
[5]	Audio_CL_OUT	switch Audio_Clock_Output to tristate	0 : on 1 : tristate	X
[6]	not used		must be 0	0
[7]	FM1 FM2	MSPC-channel 1 mode		s.Table 6–8
[8]	AM	MSPC-channel 1/2 mode	0 : FM 1 : AM	s.Table 6–8
[9]	HDEV	High Deviation Mode (channel matrix must be sound A)	0 : normal mode 1 : high deviation mode	s.Table 6–8
[10]	not used		must be 1	1
[11]	S-Bus Mode[2)]	mode of Pins S_CL and S_ID	0 : Tristate 1 : Active	0
[12]	FM2 FIR Filter Gain (FM2 = Ch1)	see table 6–10	0 : Gain = 6 dB 1 : Gain = 0 dB	0
[13]	FM2 FIR Filter Coeff. Set (FM2 = Ch1)	see table 6–10	0 : use FIR_REG_1 1 : use FIR_REG_2	0
[14]	ADR	Mode of ADR Interface	0 : normal mode 1 : ADR mode	X
[15]	AM-Gain	additional gain in AM-mode	0 : 0 dB 1 : +12 dB	0
1) In case of synchronization to DMA, no I^2S-slave mode possible. In case of I^2S-slave mode, no synchronization to DMA allowed. I^2S-Slave mode dominates. 2) The normal operation mode is ‘Tristate’; SBUS is only used in conjunction with DMA.				X: Depending on mode

Table 6–8: Channel modes ‘MODE_REG [7–9]‘

FM1 FM2 bit[7]	AM bit[8]	HDEV bit[9]	channel 1	channel 2
0	0	0	mute	FM-Mono (FM1)
1	0	0	FM2	FM1
X	1	0	AM	AM
X	X	1	FM-Mono (high deviation)	FM-Mono (high deviation)

6.2.3. FIR-Filter Switches

To simplify programming of the MSP 3400C, two additional switches have been implemented.

The FIR filter for channel1/FM2 can use either FIR_REG_1 coefficients or FIR_REG_2 coefficients by means of MODE_REG[13]. Herewith, it is no longer necessary to transmit both coefficient sets in FM-terrestrial mode. The loading sequence for FIR_REG_2 is sufficient.

The additional gain of +6 dB in channel1/FM2 can be switched to 0 dB by means of MODE_REG[12]. Together with MODE_REG[13] set to 1, in satellite mode, it is no longer necessary to transmit both FIR filter coefficient sets. The loading sequence for FIR_REG_2 is sufficient.

6.2.4. FIR-Parameter

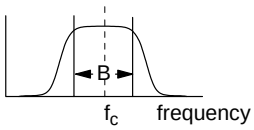
The following data values (see Table 6–9) are to be transferred **8 bits at a time embedded LSB-bound in a 16 bit word**. These sequences must be obeyed. To change a coefficient set, the complete block FIR_REG_1 or FIR_REG_2 must be transmitted. The new coefficient set will be active without a load_reg routine.

Table 6–9: Loading sequence for FIR-coefficients

WRITE_ADR = FIR_REG_1(Channel 1: FM2)			
No.	**Symbol Name**	**Bits**	**Value**
1	FM2_Coeff. (5)	8	see Table 6–10.
2	FM2_Coeff. (4)	8	
3	FM2_Coeff. (3)	8	
4	FM2_Coeff. (2)	8	
5	FM2_Coeff. (1)	8	
6	FM2_Coeff. (0)	8	

WRITE_ADR = FIR_REG_2 (Channel 2: FM1/FM mono)			
No.	**Symbol Name**	**Bits**	**Value**
1	* IMREG1 (8 LSBS)	8	04 HEX
2	* IMREG1 / IMREG2 (4 MSBs / 4 LSBs)	8	40 HEX
3	* IMREG2 (8 MSBs)	8	00 HEX
4	FM_Coef (5)	8	see Table 6–10.
5	FM_Coef (4)	8	
6	FM_Coef (3)	8	
7	FM_Coef (2)	8	
8	FM_Coef (1)	8	
9	FM_Coef (0)	8	
* IMREG_1/2: Two 12-bit off-set constants			

Table 6–10: 8-bit FIR-coefficients (decimal integer) for MSP 3410D; reset status: all coefficients are “0”

Coefficients for FIR1 0001_{hex} and FIR2 0005_{hex}								
	Terrestrial TV-Standards	**FM - Satellite** FIR filter corresponds to a bandpass with a bandwidth of B = 130 to 500 kHz 						
	B/G-,D/K-,M-Dual FM	**130 kHz**	**180 kHz**	**200 kHz**	**280 kHz**	**380 kHz**	**500 kHz**	**Autosearch**
Coef(i)	**FIR2**	**FIR2**	**FIR2**	**FIR2**	**FIR2**	**FIR2**	**FIR2**	**FIR2**
0	3	73	9	3	–8	–1	–1	75
1	18	53	18	18	–8	–9	–1	19
2	27	64	28	27	4	–16	–8	36
3	48	119	47	48	6	5	2	35
4	66	101	55	66	78	65	59	39
5	72	127	64	72	107	123	126	40
MODE-REG[12]	0	1	1	1	1	1	1	0
MODE-REG[13]	1	1	1	1	1	1	1	0
MODE_REG[12] should be set to 0 (= 6 dB gain) if the level of the FM2-carrier processed in MSP-Ch1 is appr. 7 dB below the FM1-carrier of MSP-Ch2. If both carriers have the same level, MODE_REG[12] must be set to 1 (=0 dB gain).								
MODE_REG[13]**:** If in MSP-Channel 1 and 2 the same bandwidth is required, it is sufficient to transmit FIR_REG2 only and to set MODE_REG[13] to 1.								
For compatibility (besides the above programming), the FIR-filter programming as used for the MSP 3410B is also possible.								
ADR coefficients are listed in the DRP-data sheet.								
The 130 kHz coefficients are based on subcarriers, which are 7 dB below an existent main carrier.								

6.2.5. DCO-Increments

For a chosen TV standard, a corresponding set of 24-bit increments determining the mixing frequencies of the quadrature mixers, has to be written into the IC. In Table 6–11, several examples of DCO increments are listed. It is necessary to divide them into low part and high part. The formula for the calculation of the increments for any chosen IF-Frequency is as follows:

$INCR_{dez} = int(f/fs \cdot 2^{24})$

with: int = integer function
f = IF-frequency in MHz
f_S = sampling frequency (18.432 MHz)

Conversion of INCR into hex-format and separation of the 12-bit low and high parts lead to the required increments. (DCO1_HI or _LO for channel 1, DCO2_HI or LO for channel 2).

Table 6–11: DCO increments for the MSP 3400C; frequency in MHz, increments in Hex

Frq. MHz	DCO_HI	DCO_LO	Frq. MHz	DCO_HI	DCO_LO
4.5	03E8	0000			
5.04 5.5 5.58 5.7421875	0460 04C6 04D8 04FC	0000 038E 0000 00AA	5.76 5.85 5.94	0500 0514 0528	0000 0000 0000
6.0 6.2 6.5 6.552	0535 0561 05A4 05B0	0555 0C71 071C 0000	6.6 6.65 6.8	05BA 05C5 05E7	0AAA 0C71 01C7
7.02	0618	0000	7.2	0640	0000
7.38	0668	0000	7.56	0690	0000

6.3. Sequences to Transmit Parameters and to Start Processing

After having been switched on, the MSPC must be initialized by transmitting the parameters according to the LOAD_SEQ_1/2 of Table 6–12. In the MSPC, the initialization sequence must no longer be terminated by transmitting LOAD_REG_1/2. The transmitted data are active as soon as the corresponding I^2C telegram has finished. Therefore, while changing parameters of the demodulator section, a mute is recommended for the affected channel (LOAD_SEQ_1/2: mute all FM, LOAD_SEQ_1: switch audio processing to channel2/FM1 or mute channel1/FM2). Otherwise, distorted sound may occur while switching.

For FM-stereo operation, the evaluation of the identification signal must be performed. For positive identification check, the MSP 3400C sound channels have to be switched corresponding to the detected operation mode.

6.4. Software Proposals for Multistandard TV-Sets

To familiarize the reader with the programming scheme of the MSP 3400C, two examples in the shape of flow diagrams are shown in the following sections.

6.4.1. Multistandard System B/G German DUAL FM

Fig. 6–1 shows a flow diagram for the CCU software, applied for the MSP 3400C in a TV set, which facilitates all standards according to System B/G. For the instructions used in the diagram, please refer to Table 6–12.

After having switched on the TV-set and having initialized the MSP 3400C (LOAD_SEQ_1/2), FM-mono sound is available.

Fig. 6–1 shows how to check for any stereo or bilingual audio information in channel 1. If successful, the MSP 3400C must be switched to the desired audio mode.

Table 6–12: Sequences to initialize and start the MSP 3400C

LOAD_SEQ_1/2: General Initialization	
1. AD_CV 2. FIR_REG_1 3. FIR_REG_2 4. MODE_REG 5. DCO1_LO 6. DCO1_HI 7. DCO2_LO 8. DCO2_HI	
FM_IDENT_CHECK: Decoding of the identification signal	
1. Evaluation of the stereo detection register (DFP register 0018_{hex}, high part) 2. If necessary, switch the corresponding sound channels within the audio processing part	
LOAD_SEQ_1: Reinitialization of Channel 1 without affecting Channel 2	
1. FIR_REG_1 2. MODE_REG 3. DCO1_LO 4. DCO1_HI	(6 · 8 bit) (12 bit) (12 bit)

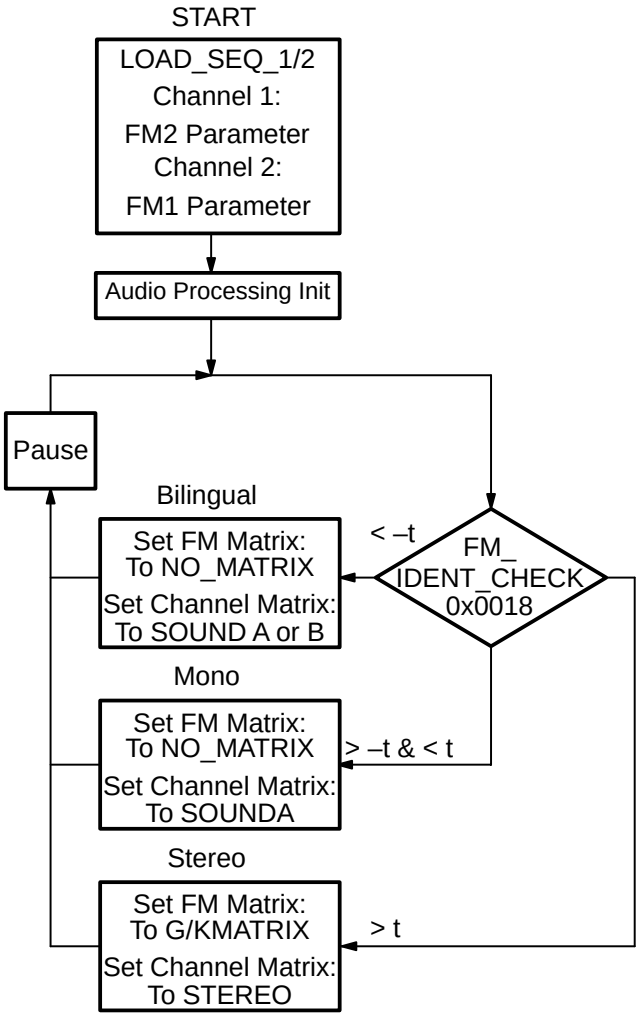


Fig. 6–1: CCU software flow diagram: Standard B/G, t = threshold value for stereo/bilingual detection

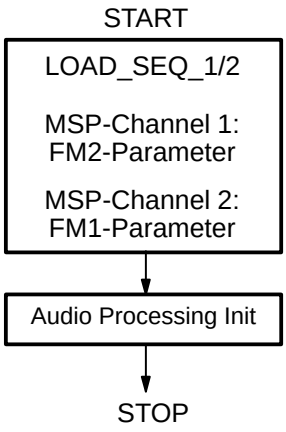


Fig. 6–2: CCU software flow diagram: SAT-mode

6.4.2. Satellite Mode

Fig. 6–2 shows the simple flow diagram to be used for the MSP 3400C in a satellite receiver. For FM-mono operation, the corresponding FM carrier should preferably be processed at the MSPC-channel 2 or at the MSPC-channel 1 with FIR gain = 0 dB.

6.4.3. Automatic Search Function for FM-Carrier Detection

The AM demodulation ability of the MSP 3400C offers the possibility to calculate the “field strength” of the momentarily selected FM carrier, which can be read out by the CCU. In SAT receivers, this feature can be used to make automatic FM carrier search possible.

Therefore, the MSPC has to be switched to AM-mode (MODE_REG[8]), FM-Prescale must be set to $7F_{hex}$=+127_{dez}, and the FM DC Notch must be switched off. The sound-IF frequency range must now be “scanned” in the MSPC-channel 2 by means of the programmable quadrature mixer with an appropriate incremental frequency (i.e. 10 kHz).

After each incrementation, a field strength value is available at the quasi-peak detector output (quasi-peak detector source must be set to FM), which must be examined for relative maxima by the CCU. This results in either continuing search or switching the MSP 3400C back to FM demodulation mode.

During the search process, the FIR_REG_2 must be loaded with the coefficient set “AUTOSEARCH”, which enables small bandwidth, resulting in appropriate field strength characteristics. The absolute field strength value (can be read out of “quasi peak detector output FM1”) also gives information on whether a main FM carrier or a subcarrier was detected, and as a practical consequence, the FM bandwidth (FIR_REG_1/2) and the deemphasis (50 µs or adaptive) can be switched automatically.

Due to the fact that a constant demodulation frequency offset of a few kHz, leads to a DC-level in the demodulated signal, a further fine tuning of the found carrier can be achieved by evaluating the “DC Level Readout FM1”. Therefore, the FM DC Notch must be switched on, and the demodulator part must be switched back to FM-demodulation mode.

For a detailed description of the automatic search function, please refer to the corresponding MSP 3400C Windows software.

Note: The automatic search is still possible by evaluating only the DC Level Readout FM1 (DC Notch On) as it is described with the MSP 3410, but the above mentioned method is faster.

6.4.4. Automatic Standard Detection

The AM demodulation ability of the MSP 3400 C enables a simple method of deciding between standard B/G (FM-carrier at 5.5 MHz) and standard I (FM-carrier at 6.0 MHz). It is achieved by tuning the MSP 3400C in the AM-mode to the two discrete frequencies and evaluating the field strength via the DC level register or the quasi-peak detector output (Mode_Reg, DC Notch, FM Prescale as described in section 6.4.3.).

7. Programming the Audio Processing Part

7.1. Summary of the DSP Control Registers

Control registers are 16 bit wide. Transmissions via I^2C bus have to take place in 16 bit words. Single data entries are 8 bit. Some of the defined 16 bit words are divided into low and high byte, thus holding two different control entities. All control registers are readable.
Note: Unused parts of the 16 bit registers must be zero.

Table 7–1: DSP Control Registers

Name	I^2C Bus Address	High/ Low	Adjustable Range, Operational Modes	Reset Mode
Volume loudspeaker channel	0000_{hex}	H	[+12 dB ... –114 dB, MUTE]	MUTE
Volume / Mode loudspeaker channel		L	1/8 dB Steps, Reduce Volume / Tone Control	00_{hex}
Balance loudspeaker channel [L/R]	0001_{hex}	H	[0..100 / 100 % and vv][–127..0 / 0 dB and vv]	100%/100%
Balance Mode loudspeaker		L	[Linear mode / logarithmic mode]	linear mode
Bass loudspeaker channel	0002_{hex}	H	[+20 dB ... –12 dB]	0 dB
Treble loudspeaker channel	0003_{hex}	H	[+15 dB ... –12 dB]	0 dB
Loudness loudspeaker channel	0004_{hex}	H	[0 dB ... +17 dB]	0 dB
Loudness Filter Characteristic		L	[NORMAL, SUPER_BASS]	NORMAL
Spatial effect strength loudspeaker ch.	0005_{hex}	H	[–100%...OFF...+100%]	OFF
Spatial effect mode/customize		L	[SBE, SBE+PSE]	SBE+PSE
Volume headphone channel	0006_{hex}	H	[+12 dB ... –114 dB, MUTE]	MUTE
Volume / Mode headphone channel		L	1/8 dB Steps, Reduce Volume / Tone Control	00_{hex}
Volume SCART channel	0007_{hex}	H	[00_{hex} ... $7F_{hex}$],[+12 dB ... –114 dB, MUTE]	00_{hex}
Volume / Mode SCART channel		L	[Linear mode / logarithmic mode]	linear mode
Loudspeaker channel source	0008_{hex}	H	[FM, NICAM, SCART, I^2S1, I^2S2]	FM
Loudspeaker channel matrix		L	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA
Headphone channel source	0009_{hex}	H	[FM, NICAM, SCART, I^2S1, I^2S2]	FM
Headphone channel matrix		L	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA
SCART1 channel source	$000a_{hex}$	H	[FM, NICAM, SCART, I^2S1, I^2S2]	FM
SCART1 channel matrix		L	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA
I^2S channel source	$000b_{hex}$	H	[FM, NICAM, SCART, I^2S1, I^2S2]	FM
I^2S channel matrix		L	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA
Quasi-peak detector source	$000c_{hex}$	H	[FM, NICAM, SCART, I^2S1, I^2S2]	FM
Quasi-peak detector matrix		L	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA
Prescale SCART	$000d_{hex}$	H	[00_{hex} ... $7F_{hex}$]	00_{hex}
Prescale FM	$000e_{hex}$	H	[00_{hex} ... $7F_{hex}$]	00_{hex}
FM matrix		L	[NO_MAT, GSTEREO, KSTEREO]	NO_MAT

Name	I²C Bus Address	High/ Low	Adjustable Range, Operational Modes	Reset Mode
Deemphasis FM	$000f_{hex}$	H	[OFF, 50 µs, 75 µs, J17]	50 µs
Adaptive Deemphasis FM		L	[OFF, WP1]	OFF
Prescale I²S2	0012_{hex}	H	[00_{hex} ... $7F_{hex}$]	10_{hex}
ACB Register (SCART Switches and DIG_OUT Pins)	0013_{hex}	H/L	Bits [15..0]	00_{hex}
Beeper	0014_{hex}	H/L	[00_{hex} ... $7F_{hex}$]/[00_{hex} ... $7F_{hex}$]	0/0
Identification Mode	0015_{hex}	L	[B/G, M]	B/G
Prescale I²S1	0016_{hex}	H	[00_{hex} ... $7F_{hex}$]	10_{hex}
FM DC Notch	0017_{hex}	L	[ON, OFF]	ON
Mode Tone Control	0020_{hex}	H	[BASS/TREBLE, EQUALIZER]	BASS/TREB
Equalizer loudspeaker ch. band 1	0021_{hex}	H	[+12 dB ... –12 dB]	0 dB
Equalizer loudspeaker ch. band 2	0022_{hex}	H	[+12 dB ... –12 dB]	0 dB
Equalizer loudspeaker ch. band 3	0023_{hex}	H	[+12 dB ... –12 dB]	0 dB
Equalizer loudspeaker ch. band 4	0024_{hex}	H	[+12 dB ... –12 dB]	0 dB
Equalizer loudspeaker ch. band 5	0025_{hex}	H	[+12 dB ... –12 dB]	0 dB
Automatic Volume Correction	0029_{hex}	H	[off, on, decay time]	off
Volume Subwoofer channel	002Chex	H	[0dB ... –30 dB, mute]	0 dB
Subwoofer Channel Corner Frequency	002Dhex	H	[50 Hz ... 400 Hz]	
Subwoofer: Complementary Highpass		L	[off, on]	off
Balance headphone channel [L/R]	0030_{hex}	H	[0...100 / 100% and vv][–127...0 / 0 dB and vv]	100%/100%
Balance Mode headphone		L	[Linear mode / logarithmic mode]	linear mode
Bass headphone channel	0031_{hex}	H	[+20 dB ... –12 dB]	0 dB
Treble headphone channel	0032_{hex}	H	[+15 dB ... –12 dB]	0 dB
Loudness headphone channel	0033_{hex}	H	[0 dB ... +17 dB]	0 dB
Loudness filter characteristic		L	[NORMAL, SUPER_BASS]	NORMAL

Note: For compatibility to new technical codes of the MSP 3400C, please consider the following compatibility restrictions:
If adaptive deemphasis is switched on, 75 µs deemphasis must be activated.

7.1.1. Volume Loudspeaker Channel and Headphone Channel

Volume loudspeaker	**0000_{hex}**	**11 MSBs**
Volume headphone	**0006_{hex}**	**11 MSBs**
+12 dB	0111 1111 000x	$7F0_{hex}$
+11.875 dB	0111 1110 111x	$7EE_{hex}$
+0.125 dB	0111 0011 001x	732_{hex}
0 dB	0111 0011 000x	730_{hex}
–0.125 dB	0111 0010 111x	$72E_{hex}$
–113.875dB	0000 0001 001x	012_{hex}
–114 dB	0000 0001 000x	010_{hex}
Mute	0000 0000 xxxx RESET	$00x_{hex}$
Fast Mute	1111 1111 111x	FFE_{hex}

The highest given positive 11-bit number ($7F0_{hex}$) yields in a maximum possible gain of 12 dB. Decreasing the volume register by 1 LSB decreases the volume by 0.125 dB. Volume settings lower than the given minimum mute the output. With large scale input signals, positive volume settings may lead to signal clipping.

With Fast Mute, volume is reduced to mute position by digital volume only. Analog volume is not changed. This reduces any audible DC plops. Going back from Fast Mute should be done to the volume step before Fast Mute was activated.

Clipping Mode loudspeaker	**0000_{hex}**	**3 LSBs**
Clipping Mode headphone	**0006_{hex}**	**3 LSBs**
Reduce Volume	x000 RESET	0_{hex}
Reduce Tone Control	x001	1_{hex}
Compromise Mode	x010	2_{hex}

If the clipping mode is set to “Reduce Volume”, the following clipping procedure is used: To prevent severe clipping effects with bass, treble, or equalizer boosts, the internal volume is automatically limited to a level where, in combination with either bass, treble, or equalizer setting, the amplification does not exceed 12 dB.

If the clipping mode is “Reduce Tone Control”, the bass or treble value is reduced if amplification exceeds 12 dB. If the equalizer is switched on, the gain of those bands is reduced, where amplification together with volume exceeds 12 dB.

If the clipping mode is “Compromise Mode”, the bass or treble value and volume are reduced half and half if amplification exceeds 12 dB (see example below). If the equalizer is switched on, the gain of those bands is reduced half and half, where amplification together with volume exceeds 12 dB.

Example:	**Vol.: +6 dB**	**Bass: +9 dB**	**Treble: +5 dB**
Red. Volume	3	9	5
Red. Tone Con.	6	6	5
Compromise	4.5	7.5	5

7.1.2. Balance Loudspeaker and Headphone Channel

Positive balance settings reduce the left channel without affecting the right channel; negative settings reduce the right channel leaving the left channel unaffected. In linear mode, a step by 1 LSB decreases or increases the balance by about 0.8% (exact figure: 100/127). In logarithmic mode, a step by 1 LSB decreases or increases the balance by 1 dB.

Balance Mode loudspeaker	**0001_{hex}**	**LSB**
Balance Mode headphone	**0030_{hex}**	**LSB**
linear	xxx0 RESET	0_{hex}
logarithmic	xxx1	1_{hex}

Linear Mode		
Balance loudspeaker channel [L/R]	**0001_{hex}**	**H**
Balance headphone channel [L/R]	**0030_{hex}**	**H**
Left muted, Right 100%	0111 1111	$7F_{hex}$
Left 0.8%, Right 100%	0111 1110	$7E_{hex}$
Left 99.2%, Right 100%	0000 0001	01_{hex}
Left 100%, Right 100%	0000 0000 RESET	00_{hex}
Left 100%, Right 99.2%	1111 1111	FF_{hex}
Left 100%, Right 0.8%	1000 0010	82_{hex}
Left 100%, Right muted	1000 0001	81_{hex}

Logarithmic Mode		
Balance loudspeaker channel [L/R]	**0001_{hex}**	**H**
Balance headphone channel [L/R]	**0030_{hex}**	**H**
Left –127 dB, Right 0 dB	0111 1111	$7F_{hex}$
Left –126 dB, Right 0 dB	0111 1110	$7E_{hex}$
Left –1 dB, Right 0 dB	0000 0001	01_{hex}
Left 0 dB, Right 0 dB	0000 0000 RESET	00_{hex}
Left 0 dB, Right –1 dB	1111 1111	FF_{hex}
Left 0 dB, Right –127 dB	1000 0001	81_{hex}
Left 0 dB, Right –128 dB	1000 0000	80_{hex}

7.1.3. Bass Loudspeaker and Headphone Channel

Bass loudspeaker	**0002_{hex}**	**H**
Bass headphone	**0031_{hex}**	**H**
+20 dB	0111 1111	$7F_{hex}$
+18 dB	0111 1000	78_{hex}
+16 dB	0111 0000	70_{hex}
+14 dB	0110 1000	68_{hex}
+12 dB	0110 0000	60_{hex}
+11 dB	0101 1000	58_{hex}
+1 dB	0000 1000	08_{hex}
+1/8 dB	0000 0001	01_{hex}
0 dB	0000 0000 RESET	00_{hex}
–1/8 dB	1111 1111	FF_{hex}
–1 dB	1111 1000	$F8_{hex}$
–11 dB	1010 1000	$A8_{hex}$
–12 dB	1010 0000	$A0_{hex}$

With positive bass settings, internal overflow may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass to a value that, in conjunction with volume, would result in an overall positive gain.

Loudspeaker channel: Bass and Equalizer cannot work simultaneously (see Table: Mode Tone Control). If Equalizer is used, Bass and Treble coefficients must be set to zero and vice versa.

7.1.4. Treble Loudspeaker and Headphone Channel

Treble loudspeaker	**0003_{hex}**	**H**
Treble headphone	**0032_{hex}**	**H**
+15 dB	0111 1000	78_{hex}
+14 dB	0111 0000	70_{hex}
+1 dB	0000 1000	08_{hex}
+1/8 dB	0000 0001	01_{hex}
0 dB	0000 0000 RESET	00_{hex}
–1/8 dB	1111 1111	FF_{hex}
–1 dB	1111 1000	$F8_{hex}$
–11 dB	1010 1000	$A8_{hex}$
–12 dB	1010 0000	$A0_{hex}$

With positive treble settings, internal overflow may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set treble to a value that, in conjunction with volume, would result in an overall positive gain.

Loudspeaker channel: Treble and Equalizer cannot work simultaneously (see Table: Mode Tone Control). If Equalizer is used, Bass and Treble coefficients must be set to zero and vice versa.

7.1.5. Loudness Loudspeaker and Headphone Channel

Loudness loudspeaker	**0004_{hex}**	**H**
Loudness headphone	**0033_{hex}**	**H**
+17 dB	0100 0100	44_{hex}
+16 dB	0100 0000	40_{hex}
+1 dB	0000 0100	04_{hex}
0 dB	0000 0000 RESET	00_{hex}

Mode Loudness loudspeaker	**0004_{hex}**	**L**
Mode Loudness headphone	**0033_{hex}**	**L**
Normal (constant volume at 1 kHz)	0000 0000 RESET	00_{hex}
Super Bass (constant volume at 2 kHz)	0000 0100	04_{hex}

Loudness increases the volume of low and high frequency signals, while keeping the amplitude of the 1 kHz reference frequency constant. The intended loudness has to be set according to the actual volume setting. Because loudness introduces gain, it is not recommended to set loudness to a value that ,in conjunction with volume, would result in an overall positive gain.

By means of ‘Mode Loudness’, the corner frequency for bass amplification can be set to two different values. In Super Bass mode, the corner frequency is shifted up. The point of constant volume is shifted from 1 kHz to 2 kHz.

7.1.6. Spatial Effects Loudspeaker Channel

Spatial effect strength loudspeaker channel	**0005_{hex}**	**H**
Enlargement 100%	0111 1111	$7F_{hex}$
Enlargement 50%	0011 1111	$3F_{hex}$
Enlargement 1.5%	0000 0001	01_{hex}
Effect off	0000 0000 RESET	00_{hex}
Reduction 1.5%	1111 1111	FF_{hex}
Reduction 50%	1100 0000	$C0_{hex}$
Reduction 100%	1000 0000	80_{hex}
Spatial Effect Mode	**0005_{hex}**	**[7:4]**
Stereo Basewidth Enlargement (SBE) and Pseudo Stereo Effect (PSE). (Mode A)	0000 RESET 0000	0_{hex} 0_{hex}
Stereo Basewidth Enlargement (SBE) only. (Mode B)	0010	2_{hex}
Spatial Effect Customize Coefficient	**0005_{hex}**	**[3:0]**
max high pass gain	0000 RESET	0_{hex}
2/3 high pass gain	0010	2_{hex}
1/3 high pass gain	0100	4_{hex}
min high pass gain	0110	6_{hex}
automatic	1000	8_{hex}

There are several spatial effect modes available:

Mode A (low byte = 00_{hex}) is compatible to the formerly used spatial effect. Here, the kind of spatial effect depends on the source mode. If the incoming signal is in mono mode, Pseudo Stereo Effect is active; for stereo signals, Pseudo Stereo Effect and Stereo Basewidth Enlargement is effective. The strength of the effect is controllable by the upper byte. A negative value reduces the stereo image. A rather strong spatial effect is recommended for small TV sets where loudspeaker spacing is rather close. For large screen TV sets, a more moderate spatial effect is recommended. In mode A, even in case of stereo input signals, Pseudo Stereo Effect is active, which reduces the center image.

In Mode B, only Stereo Basewidth Enlargement is effective. For mono input signals, the Pseudo Stereo Effect has to be switched on.

It is worth mentioning, that all spatial effects affect amplitude and phase response. With the lower 4 bits, the frequency response can be customized. A value of 0000_{bin} yields a flat response for center signals (L = R) but a high pass function of L or R only signals. A value of 0110_{bin} has a flat response for L or R only signals but a lowpass function for center signals. By using 1000_{bin}, the frequency response is automatically adapted to the sound material by choosing an optimal high pass gain.

7.1.7. Volume SCART

Volume Mode SCART	**0007_{hex}**	**LSB**
linear	xxx0 RESET	0_{hex}
logarithmic	xxx1	1_{hex}

Linear Mode		
Volume SCART	**0007_{hex}**	**H**
OFF	0000 0000 RESET	00_{hex}
0 dB gain (digital full scale (FS) to 2 V_{RMS} output)	0100 0000	40_{hex}
+6 dB gain (–6 dBFS to 2 V_{RMS} output)	0111 1111	$7F_{hex}$

Logarithmic Mode		
Volume SCART	**0007_{hex}**	**11 MSBs**
+12 dB	0111 1111 000x	$7F0_{hex}$
+11.875 dB	0111 1110 111x	$7EE_{hex}$
+0.125 dB	0111 0011 001x	732_{hex}
0 dB	0111 0011 000x	730_{hex}
–0.125 dB	0111 0010 111x	$72E_{hex}$
–113.875 dB	0000 0001 001x	012_{hex}
–114 dB	0000 0001 000x	010_{hex}
Mute	0000 0000 0000 RESET	000_{hex}

7.1.8. Channel Source Modes

Loudspeaker channel source	**0008_{hex}**	**H**
Headphone channel source	**0009_{hex}**	**H**
SCART channel source	**$000a_{hex}$**	**H**
I^2S channel source	**$000b_{hex}$**	**H**
Quasi-peak detector source	**$000c_{hex}$**	**H**
FM	0000 0000 RESET	00_{hex}
NONE (MSP3410: NICAM)	0000 0001	01_{hex}
SCART	0000 0010	02_{hex}
SBUS12	0000 0011	03_{hex}
SBUS34	0000 0100	04_{hex}
I^2S1	0000 0101	05_{hex}
I^2S2	0000 0110	06_{hex}

Note: For Headphone output it is also possible to select a subwoofer signal derived from the Loudspeaker channel. For more details see section 7.1.23.

7.1.9. Channel Matrix Modes (see also Table 4–1)

Loudspeaker channel matrix	**0008_{hex}**	**L**
Headphone channel matrix	**0009_{hex}**	**L**
SCART channel matrix	**$000a_{hex}$**	**L**
I^2S channel matrix	**$000b_{hex}$**	**L**
Quasi-peak detector-matrix	**$000c_{hex}$**	**L**
SOUNDA / LEFT / MSP-IF-CHANNEL2	0000 0000 RESET	00_{hex}
SOUNDB / RIGHT / MSP-IF-CHANNEL1	0001 0000	10_{hex}
STEREO	0010 0000	20_{hex}
MONO	0011 0000	30_{hex}
SUM/DIFF	0100 0000	40_{hex}
AB_XCHANGE	0101 0000	50_{hex}
INVERT_B	0110 0000	60_{hex}

The sum/difference mode can be used together with the quasi-peak detector to determine the sound material mode. If the difference signal on channel B (right) is near to zero, and the sum signal on channel A (left) is high, the incoming audio signal is mono. If there is a significant level on the difference signal, the incoming audio is stereo.

7.1.10. SCART Prescale

Volume Prescale SCART	**$000d_{hex}$**	**H**
OFF	0000 0000 RESET	00_{hex}
0 dB gain (2 V_{RMS} input to digital full scale)	0001 1001	19_{hex}
+14 dB gain (400 mV_{RMS} input to digital full scale)	0111 1111	$7F_{hex}$

7.1.11. FM Prescale

Volume Prescale FM (normal FM mode)	**$000e_{hex}$**	**H**
OFF	0000 0000 RESET	00_{hex}
Maximum Volume (28 kHz deviation [1] recommended FIR-bandwidth: 130 kHz)	0111 1111	$7F_{hex}$
Deviation 50 kHz[1] recommended FIR-bandwidth: 200 kHz	0100 1000	48_{hex}
Deviation 75 kHz[1] recommended FIR-bandwidth: 200 or 280 kHz	0011 0000	30_{hex}
Deviation 150 kHz[1] recommended FIR-bandwidth: 380 kHz	0001 1000	18_{hex}
Maximum deviation 192 kHz[1] recommended FIR-bandwidth: 380 kHz	0001 0011	13_{hex}
Prescale for adaptive deemphasis WP1 recommended FIR-bandwidth: 130 kHz	0001 0000	10_{hex}
Volume Prescale FM (High Deviation Mode)	**$000e_{hex}$**	**H**
Deviation 150 kHz[1] recommended FIR-bandwidth: 380 kHz	0011 0000	30_{hex}
Maximum deviation 384 kHz[1] recommended FIR-bandwidth: 500 kHz	0001 0011	13_{hex}

For the **High Deviation Mode,** the FM prescaling values can be used in the range between 13_{hex} to 30_{hex}. Please consider the internal reduction of 6 dB for this mode. The FIR-bandwidth should be selected to 500 kHz.

[1] Given deviations will result in internal digital full scale signals. Appropriate clipping headroom has to be set by the customer. This can be done by decreasing the listed values by a specific factor.

7.1.12. FM Matrix Modes (see also Table 4–1)

FM matrix	$000e_{hex}$	L
NO MATRIX	0000 0000 RESET	00_{hex}
GSTEREO	0000 0001	01_{hex}
KSTEREO	0000 0010	02_{hex}

NO_MATRIX is used for terrestrial mono or satellite stereo sound. GSTEREO dematrixes (L+R, 2R) to (2L, 2R) and is used for German dual carrier stereo system (Standard B/G). KSTEREO dematrixes (L+R, L–R) to (2L, 2R) and is used for the Korean dual carrier stereo system (Standard M).

7.1.13. FM Fixed Deemphasis

Deemphasis FM	$000f_{hex}$	H
50 µs	0000 0000 RESET	00_{hex}
75 µs	0000 0001	01_{hex}
J17	0000 0100	04_{hex}
OFF	0011 1111	$3F_{hex}$

7.1.14. FM Adaptive Deemphasis

FM Adaptive Deemphasis WP1	$000f_{hex}$	L
OFF	0000 0000 RESET	00_{hex}
WP1	0011 1111	$3F_{hex}$

Must be set to ‘OFF’ in case of dual carrier stereo (German or Korean). If ‘ON’, FM fixed deemphasis must be set to 75 µs.

7.1.15. I^2S1 and I^2S2 Prescale

Prescale I^2S1	0016_{hex}	H
Prescale I^2S2	**0012_{hex}**	**H**
OFF	00_{hex}	
0 dB gain	10_{hex} RESET	
+18 dB gain	$7F_{hex}$	

7.1.16. ACB Register, Definition of the SCART-Switches and DIG_CTR_OUT Pins

ACB Register	0013_{hex}	H
DSP In Selection of Source: SC_1_IN MONO_IN SC_2_IN SC_3_IN	 xxxx xx00 xxxx xx01 xxxx xx10 xxxx xx11	 RESET
SC_1_OUT_L/R Selection of Source: SC_3_IN SC_2_IN MONO_IN DA_SCART	 xxxx 00xx xxxx 01xx xxxx 10xx xxxx 11xx	 RESET
SC_2_OUT_L/R Selection of Source: DA_SCART SC_1_IN MONO_IN	 xx00 xxxx xx01 xxxx xx10 xxxx	 RESET
DIG_CTR_OUT1 low high	 x0xx xxxx x1xx xxxx	 RESET
DIG_CTR_OUT2 low high	 0xxx xxxx 1xxx xxxx	 RESET
RESET: The RESET state is taken at the time of the first write transmission on the control bus to the audio processing part (DSP). By writing to the ACB register first, the RESET state can be redefined.		

7.1.17. Beeper

Beeper Volume	**0014_{hex}**	**H**
OFF	0000 0000 RESET	00_{hex}
Maximum Volume (full digital scale FDS)	0111 1111	$7F_{hex}$
Beeper Frequency	**0014_{hex}**	**L**
16 Hz (lowest)	0000 0001	01_{hex}
1 kHz	0100 0000	40_{hex}
4 kHz (highest)	1111 1111	FF_{hex}

A squarewave beeper can be added to the loudspeaker channel and the headphone channel. The addition point is just before loudness and volume adjustment.

7.1.18. Identification Mode

Identification Mode	**0015_{hex}**	**L**
Standard B/G (German Stereo)	0000 0000 RESET	00_{hex}
Standard M (Korean Stereo)	0000 0001	01_{hex}
Reset of Ident-Filter	0011 1111	$3F_{hex}$

To shorten the response time of the identification algorithm after a program change between two FM-stereo capable programs, the reset of ident-filter can be applied.

Sequence:

1. Program change
2. Reset ident-filter
3. Wait at least 1 msec.
4. Set identification mode back to standard B/G or M
5. Wait approx. 1 sec.
6. Read stereo detection register

7.1.19. FM DC Notch

FM DC Notch	**0017_{hex}**	**L**
ON	0000 0000 Reset	00_{hex}
OFF	0011 1111	$3F_{hex}$

The DC compensation filter (FM DC Notch) for FM input can be switched off. This is used to speed up the automatic search function (see sector 6.4.3.). In normal FM-mode, the FM DC Notch should be switched on.

7.1.20. Mode Tone Control

Mode Tone Control	**00020_{hex}**	**H**
Bass and Treble	0000 0000 RESET	00_{hex}
Equalizer	1111 1111	FF_{hex}

By means of ‘Mode Tone Control’, Bass/Treble or Equalizer may be activated.

7.1.21. Equalizer Loudspeaker Channel

Band 1 (below 120 Hz)	**0021_{hex}**	**H**
Band 2 (Center: 500 Hz)	**0022_{hex}**	**H**
Band 3 (Center: 1.5 kHz)	**0023_{hex}**	**H**
Band 4 (Center: 5 kHz)	**0024_{hex}**	**H**
Band 5 (above 10kHz)	**0025_{hex}**	**H**
+12 dB	0110 0000	60_{hex}
+11 dB	0101 1000	58_{hex}
+1 dB	0000 1000	08_{hex}
+1/8 dB	0000 0001	01_{hex}
0 dB	0000 0000 RESET	00_{hex}
–1/8 dB	1111 1111	FF_{hex}
–1 dB	1111 1000	$F8_{hex}$
–11dB	1010 1000	$A8_{hex}$
–12 dB	1010 0000	$A0_{hex}$

With positive equalizer settings, internal overflow may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set equalizer bands to a value that, in conjunction with volume, would result in an overall positive gain.

Equalizer must not be used simultaneously with Bass and Treble (Mode Tone Control must be set to FF to use the Equalizer).

7.1.22. Automatic Volume Correction (AVC)

AVC	**on/off**	**0029hex**	**[15:12]**
AVC	off and Reset of int. variables	0000 RESET	0hex
AVC	on	1000	8hex
AVC	**Decay Time**	**0029hex**	**[11:8]**
8 sec	(long)	1000	8hex
4 sec	(middle)	0100	4hex
2 sec	(short)	0010	2hex
20 ms	(very short)	0001	1hex

Different sound sources (e.g. Terrestrial channels, SAT channels or SCART) fairly often don't have the same volume level. Advertisement during movies as well has mostly a different (higher) volume level, than the movie itself. The Automatic Volume Correction (AVC) solves this problem and equalizes the volume levels.

The absolute value of the incoming signal is fed into a filter with 16ms attack time and selectable decay time. The decay time must be adjusted as shown in the table above. This attack/decay filter block works similar to a peak hold function. The volume correction value with it's quasi continuous step width is calculated using the attack/decay filter output.

The Automatic Volume Correction works with an internal reference level of –18 dBFS. This means, input signals with a volume level of –18 dBFS will not be affected by the AVC. If the input signals vary in a range of –24 dB to 0 dB the AVC compensates this.

Example: A static input signal of 1 kHz on Scart has an output level as shown in the table below.

Scart Input 0dbr = 2 Vrms	**Volume Correction**	**Main Output 0dBr = 1.4 Vrms**
0 dBr	–18 dB	–18 dBr
–6 dBr	–12 dB	–18 dBr
–12 dBr	–6 dB	–18 dBr
–18 dBr	–0 dB	–18 dBr
–24 dBr	+ 6 dB	–18 dBr
–30 dBr	+ 6 dB	–24 dBr
Loudspeaker Volume = 73h = 0 dBFS Scart Prescale = 20h i.e. 2.0 Vrms = 0dBFS		

To reset the internal variables, the AVC should be switched off and on during any channel or source change. For standard applications, the recommended decay time is 4sec.

Note: AVC should not be used in any Dolby Prologic modes, except PANORAMA, where no other than the loudspeaker output is active.

7.1.23. Subwoofer on Headphone Output

The subwoofer channel is created by combining the left and right loudspeaker channels ((L+R)/2) directly behind the tone control filter block. A third order lowpass filter with programmable corner frequency and volume adjustment respectively to the loudspeaker channel output is performed to the bass-signal. Additionally, at the loudspeaker channels, a complementary high pass filter can be switched on. The subwoofer channel output can be switched to the headphone D/A converter alternatively with the headphone output.

Subwoofer Channel Volume Adjust	**002Chex**	**H**
0 dB	0000 0000 RESET	00hex
–1 dB	1111 1111	FFhex
–29 dB	1110 0011	E3hex
–30 dB	1110 0010	E2hex
Mute	1000 0000	80hex

Subwoofer Channel Corner Frequency	**002Dhex**	**H**
50 Hz .... 400 Hz e.g. 50 Hz = 5 int 400 Hz = 40int	 0000 0101 0010 1000	 05hex 28hex
Headphone Output	**002Dhex**	**[7:4]**
Headphone	0000	0hex
Subwoofer	1000	8hex
Subwoofer: Complementary Highpass	**002Dhex**	**[3:0]**
HP off	0000	0hex
HP on	0001	1hex

Note: If subwoofer is chosen for headphone output, the corner frequency must be set to the desired value, before the loudspeaker volume is set. This is to avoid plop noise.

7.2. Exclusions

In general, all functions can be switched independently of the others. One exception exists:

1. If the adaptive deemphasis is activated (Reg. 000f_{hex} L), the FM fixed deemphasis (Reg. 000f_{hex} H) must be set to 75 µs.

7.3. Summary of Readable Registers

All readable registers are 16 bit wide. Transmissions via I^2C bus have to take place in 16 bit words. Single data entries are 8 bit. Some of the defined 16 bit words are divided into low and high byte, thus holding two different control entities.

These registers are not writeable.

Name	Address	High/Low	Output Range	
Stereo detection register	0018_{hex}	H	$[80_{hex}$ ... $7F_{hex}]$	8 bit two's complement
Quasi peak readout left	0019_{hex}	H&L	$[00_{hex}$ ... $7FFF_{hex}]$	16 bit binary
Quasi peak readout right	$001a_{hex}$	H&L	$[00_{hex}$ ... $7FFF_{hex}]$	16 bit binary
DC level readout FM1/Ch2–L	$001b_{hex}$	H&L	$[00_{hex}$ ... $7FFF_{hex}]$	16 bit binary
DC level readout FM2/Ch1–R	$001c_{hex}$	H&L	$[00_{hex}$ ... $7FFF_{hex}]$	16 bit binary
MSP hardware version code	$001e_{hex}$	H	$[00_{hex}$ ... $FF_{hex}]$	
MSP major revision code		L	$[00_{hex}$ ... $FF_{hex}]$	
MSP product code	$001f_{hex}$	H	$[00_{hex}$ ... $0A_{hex}]$	
MSP ROM version code		L	$[00_{hex}$ ... $FF_{hex}]$	

7.3.1. Stereo Detection Register

Stereo Detection Register	**0018_{hex} H**
Stereo Mode	Reading (two's complement)
MONO	near zero
STEREO	positive value (ideal reception: $7F_{hex}$)
BILINGUAL	negative value (ideal reception: 80_{hex})

7.3.2. Quasi Peak Detector

Quasi peak readout left	**0019_{hex} H+L**
Quasi peak readout right	**$001a_{hex}$ H+L**
Quasi peak readout	$[0_{hex}$ ... $7FFF_{hex}]$ values are 16 bit binary

The quasi peak readout register can be used to read out the quasi peak level of any input source, in order to adjust all inputs to the same normalized listening level. The refresh rate is 32 kHz. The feature is based on a filter time constant:

attack-time: 1.3 ms
decay-time: 37 ms

7.3.3. DC Level Register

DC level readout FM1	**001b$_{hex}$** **H+L**
DC level readout FM2	**001c$_{hex}$** **H+L**
DC Level	[0$_{hex}$ ... 7FFF$_{hex}$] values are 16 bit binary

The DC level register measures the DC component of the incoming FM signals (FM1 and FM2). This can be used for seek functions in satellite receivers and for IF FM frequencies fine tuning. For further processing, the DC content of the demodulated FM signals is suppressed. The time constant τ, defining the transition time of the DC Level Register, is approximately 28 ms.

7.3.4. MSP Hardware Version Code

Hardware Version	**001e$_{hex}$** **H**
Hardware Version	[00$_{hex}$ ... FF$_{hex}$]
MSP 3400C – **C**8	03$_{hex}$

A change in the hardware version code defines hardware optimizations that may have influence on the chip's behavior. The readout of this register is identical to the hardware version code in the chip's imprint.

7.3.5. MSP Major Revision Code

Major Revision	**001e$_{hex}$** **L**
MSP 3400C	03$_{hex}$

The MSP 3400C is the third generation of ICs in the MSP family.

7.3.6. MSP Product Code

Product	**001f$_{hex}$**	**H**
MSP 3400C	0000 0000	00$_{hex}$
MSP 3400	0000 1010	0A$_{hex}$[1)]
MSP 34**10**	0000 1010	0A$_{hex}$

1) Note: The MSP 3400 hardware is identical to the MSP 3410. Therefore, the family code readout will show 'MSP 3410' instead of its label 'MSP 3400'.

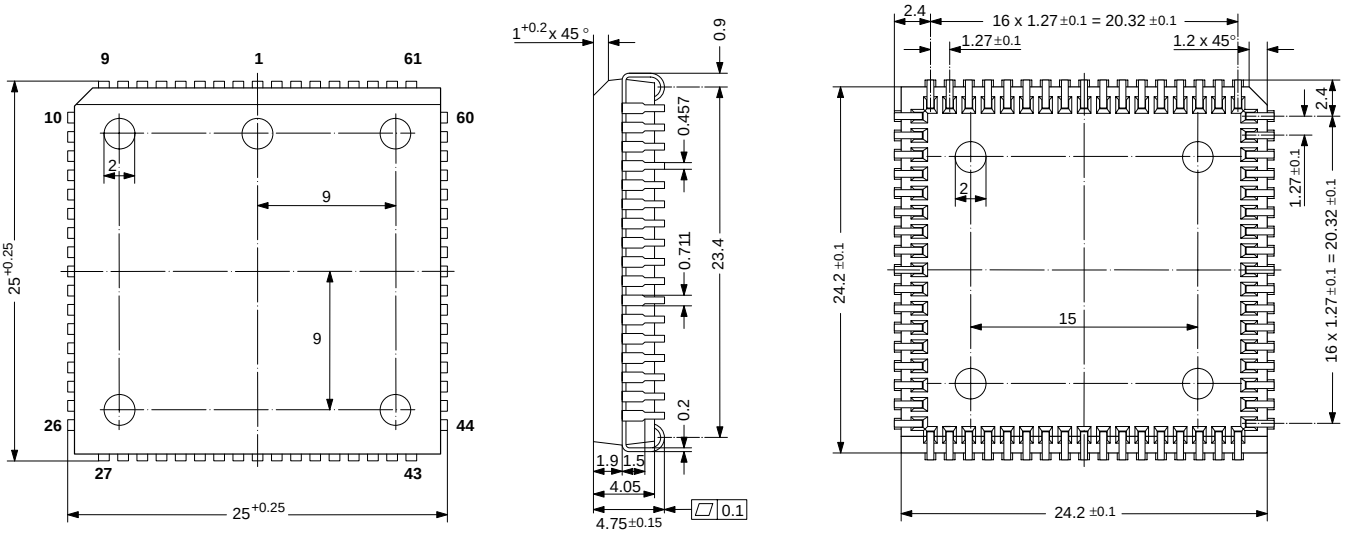
7.3.7. MSP ROM Version Code

ROM Version	**001f$_{hex}$**	**L**
Major software revision	[00$_{hex}$ ... FF$_{hex}$]	
MSP 3400C – B**5**	0000 0101	05$_{hex}$
MSP 3400C – C**6**	0000 0110	06$_{hex}$
MSP 3400C – C**8**	0000 1000	08$_{hex}$

A change in the ROM version code defines internal software optimizations, that may have influence on the chip's behavior, e.g. new features may have been included. While a software change is intended to create no compatibility problems, customers that want to use the new functions can identify new MSP 3400C versions according to this number. The readout of this register is identical to the ROM version code in the chip's imprint.

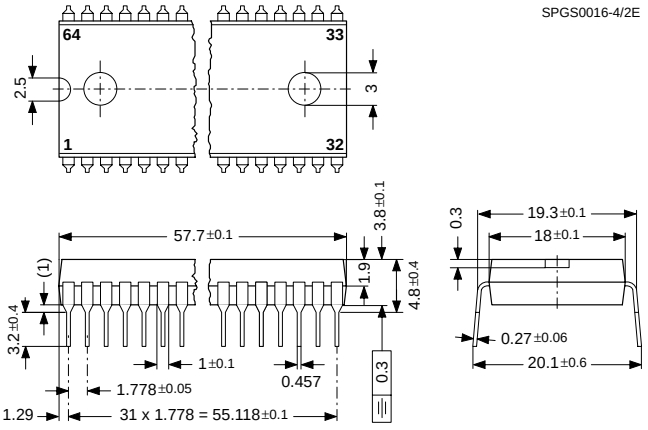
8. Specifications

8.1. Outline Dimensions



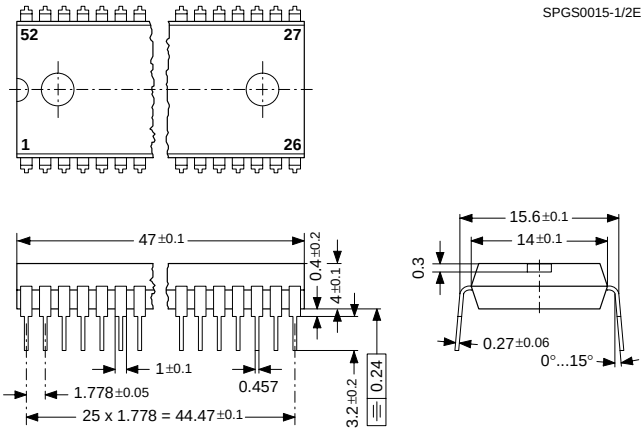
SPGS7004-3/4E

Fig. 8–1:
68-Pin Plastic Leaded Chip Carrier Package
(PLCC68)
Weight approximately 4.8 g
Dimensions in mm



SPGS0016-4/2E

Fig. 8–2:
64-Pin Plastic Shrink Dual Inline Package
(PSDIP64)
Weight approximately 9.0 g
Dimensions in mm



SPGS0015-1/2E

Fig. 8–3:
52-Pin Plastic Shrink Dual In Line Package
(PSDIP52)
Weight approximately 5.5 g
Dimensions in mm

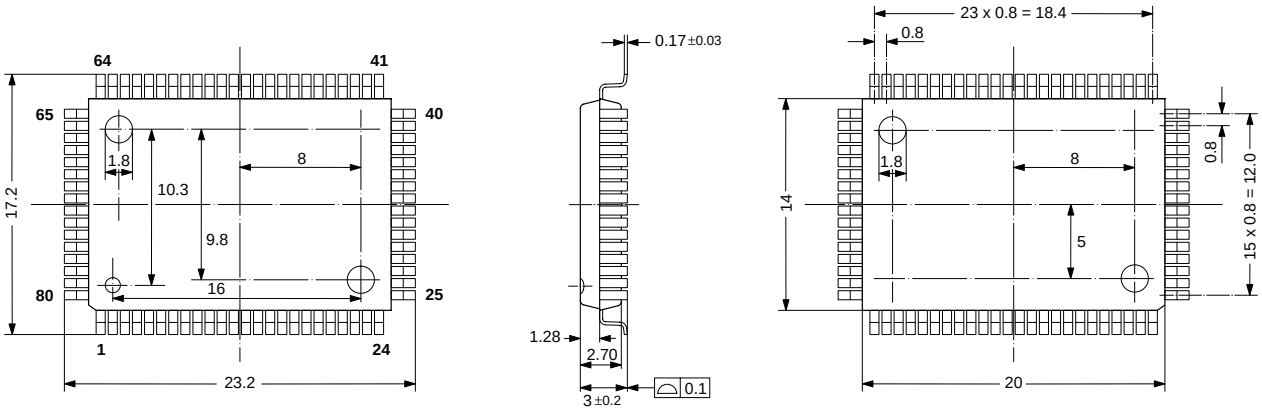


Fig. 8–4:
80-Pin Plastic Quad Flat Pack Package
(PQFP80)
Weight approximately 1.61 g
Dimensions in mm

8.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram

AHVSS = connect to AHVSS
DVSS = if not used, connect to DVSS
– = pin does not exist in this package

Pin No. PLCC 68-pin	Pin No. PSDIP 64-pin	Pin No. PSDIP 52-pin	Pin No. PQFP 80-pin	Pin Name 3410D in ( )	Type	Connection (if not used)	Short Description
1	16	14	9	S_ID (ADR_WS)	OUT	LV	SBUS Ident or ADR wordstrobe[1)]
2	–	–	–	NC		LV	Not connected
3	15	13	8	S_DA_IN (ADR_DA)	OUT	LV	SBUS Data input or ADR data output[1)]
4	14	12	7	I^2S_DA_IN1	IN	LV	I^2S1 data input
5	13	11	6	I^2S_DA_OUT	OUT	LV	I^2S data output
6	12	10	5	I^2S_WS	IN/OUT	LV	I^2S wordstrobe
7	11	9	4	I^2S_CL	IN/OUT	LV	I^2S clock
8	10	8	3	I^2C_DA	IN/OUT	X	I^2C data
9	9	7	2	I^2C_CL	IN/OUT	X	I^2C clock
10	8	–	1	NC		LV	Not connected
11	7	6	80	STANDBYQ	IN	X	Standby (low-active)
12	6	5	79	ADR_SEL	IN	X	I^2C Bus address select

1) Depending on MODE_REG[14], the SBUS Interface can be switched into ADR_MODE with S_CL becoming ADR_CL, S_ID becoming ADR_WS and S_DA_IN becoming ADR_DA (see also section 4.5.).
2) Due to compatibility with MSP 3410, it is possible to connect with DVSS as well.

Pin No. PLCC 68-pin	Pin No. PSDIP 64-pin	Pin No. PSDIP 52-pin	Pin No. PQFP 80-pin	Pin Name 3410D in ( )	Type	Connection (if not used)	Short Description
13	5	4	78	D_CTR_OUT0	OUT	LV	Digital control output 0
14	4	3	77	D_CTR_OUT1	OUT	LV	Digital control output 1
15	3	–	76	NC		LV	Not connected
16	2	–	–	NC		LV	Not connected
17	–	–	75	NC		LV	Not connected
18	1	2	74	AUD_CL_OUT	OUT	LV	Audio clock output
19	64	1	73	DMA_SYNC	IN	LV	DMA-Sync. Input
20	63	52	72	XTAL_OUT	OUT	X	Crystal oscillator
21	62	51	71	XTAL_IN	IN	X	Crystal oscillator
22	61	50	70	TESTEN	IN	X	Test pin
23	60	49	69	ANA_IN2+	IN	LV	IF input 2 (if ANA_IN1+ is used only, connect to AVSS with 50 pF capacitor)
24	59	48	68	ANA_IN–	IN	LV	IF common
25	58	47	67	ANA_IN1+	IN	LV	IF input 1
26	57	46	66	AVSUP		X	Analog power supply +5 V
–	–	–	65	AVSUP		X	Analog power supply +5 V
–	–	–	64	NC		LV	Not connected
–	–	–	63	NC		LV	Not connected
27	56	45	62	AVSS		X	Analog ground
–	–	–	61	AVSS		X	Analog ground
28	55	44	60	MONO_IN	IN	LV	Mono input
–	–	–	59	NC		LV	Not connected
29	54	43	58	VREFTOP		X	Reference voltage IF A/D converter
30	53	42	57	SC1_IN_R	IN	LV	Scart input 1 in, right
31	52	41	56	SC1_IN_L	IN	LV	Scart input 1 in, left
32	51	–	55	ASG1		AHVSS	Analog Shield Ground 1
33	50	40	54	SC2_IN_R	IN	LV	Scart input 2 in, right
34	49	39	53	SC2_IN_L	IN	LV	Scart input 2 in, left

1) Depending on MODE_REG[14], the SBUS Interface can be switched into ADR_MODE with S_CL becoming ADR_CL, S_ID becoming ADR_WS and S_DA_IN becoming ADR_DA (see also section 4.5.).
2) Due to compatibility with MSP 3410, it is possible to connect with DVSS as well.

Pin No. PLCC 68-pin	Pin No. PSDIP 64-pin	Pin No. PSDIP 52-pin	Pin No. PQFP 80-pin	Pin Name 3410D in ( )	Type	Connection (if not used)	Short Description
35	48	–	52	ASG2		AHVSS	Analog Shield Ground 2
36	47	38	51	SC3_IN_R	IN	LV	Scart input 3 in, right
37	46	37	50	SC3_IN_L	IN	LV	Scart input 3 in, left
38	45	–	49	NC (ASG4)		LV	Not connected
39	44	–	48	NC (SC4_IN_R)		LV	Not connected
40	43	–	47	NC (SC4_IN_L)		LV	Not connected
41	–	–	46	NC		LV or AHVSS	Not connected
42	42	36	45	AGNDC		X	Analog reference voltage high voltage part
43	41	35	44	AHVSS		X	Analog ground
–	–	–	43	AHVSS		X	Analog ground
–	–	–	42	NC		LV	Not connected
–	–	–	41	NC		LV	Not connected
44	40	34	40	CAPL_M		X	Volume capacitor MAIN
45	39	33	39	AHVSUP		X	Analog power supply 8.0 V
46	38	32	38	CAPL_A		X	Volume capacitor AUX
47	37	31	37	SC1_OUT_L	OUT	LV	Scart output 1, left
48	36	30	36	SC1_OUT_R	OUT	LV	Scart output 1, right
49	35	29	35	VREF1		X	Reference ground 1 high voltage part
50	34	28	34	SC2_OUT_L	OUT	LV	Scart output 2, left
51	33	27	33	SC2_OUT_R	OUT	LV	Scart output 2, right
52	–	–	32	ASG3		AHVSS[2)]	Analog Shield Ground 3
53	32	–	31	NC		LV	Not connected
54	31	26	30	NC (DACM_SUB)		LV	Not connected
55	30	–	29	NC		LV	Not connected
56	29	25	28	DACM_L	OUT	LV	Analog output MAIN, left

1) Depending on MODE_REG[14], the SBUS Interface can be switched into ADR_MODE with S_CL becoming ADR_CL, S_ID becoming ADR_WS and S_DA_IN becoming ADR_DA (see also section 4.5.).

2) Due to compatibility with MSP 3410, it is possible to connect with DVSS as well.

Pin No. PLCC 68-pin	Pin No. PSDIP 64-pin	Pin No. PSDIP 52-pin	Pin No. PQFP 80-pin	Pin Name 3410D in ( )	Type	Connection (if not used)	Short Description
57	28	24	27	DACM_R	OUT	LV	Analog output MAIN, right
58	27	23	26	VREF2		X	Reference ground 2 high voltage part
59	26	22	25	DACA_L	OUT	LV	Analog output AUX, left
60	25	21	24	DACA_R	OUT	LV	Analog output AUX, right
–	–	–	23	NC		LV	Not connected
–	–	–	22	NC		LV	Not connected
61	24	20	21	RESETQ	IN	X	Power-on-reset
62	23	–	20	NC		LV	Not connected
63	22	–	19	NC		LV	Not connected
64	21	19	18	NC		LV	Not connected
65	20	18	17	I^2S_DA_IN2	IN	LV	I^2S2-data input
66	19	17	16	DVSS		X	Digital ground
–	–	–	15	DVSS		X	Digital ground
–	–	–	14	DVSS		X	Digital ground
67	18	16	13	DVSUP		X	Digital power supply +5 V
–	–	–	12	DVSUP		X	Digital power supply +5 V
–	–	–	11	DVSUP		X	Digital power supply +5 V
68	17	15	10	S_CL (ADR_CL)	OUT	LV	SBUS clock or ADR clock[1)]

1) Depending on MODE_REG[14], the SBUS Interface can be switched into ADR_MODE with S_CL becoming ADR_CL, S_ID becoming ADR_WS and S_DA_IN becoming ADR_DA (see also section 4.5.).
2) Due to compatibility with MSP 3410, it is possible to connect with DVSS as well.

8.3. Pin Configurations

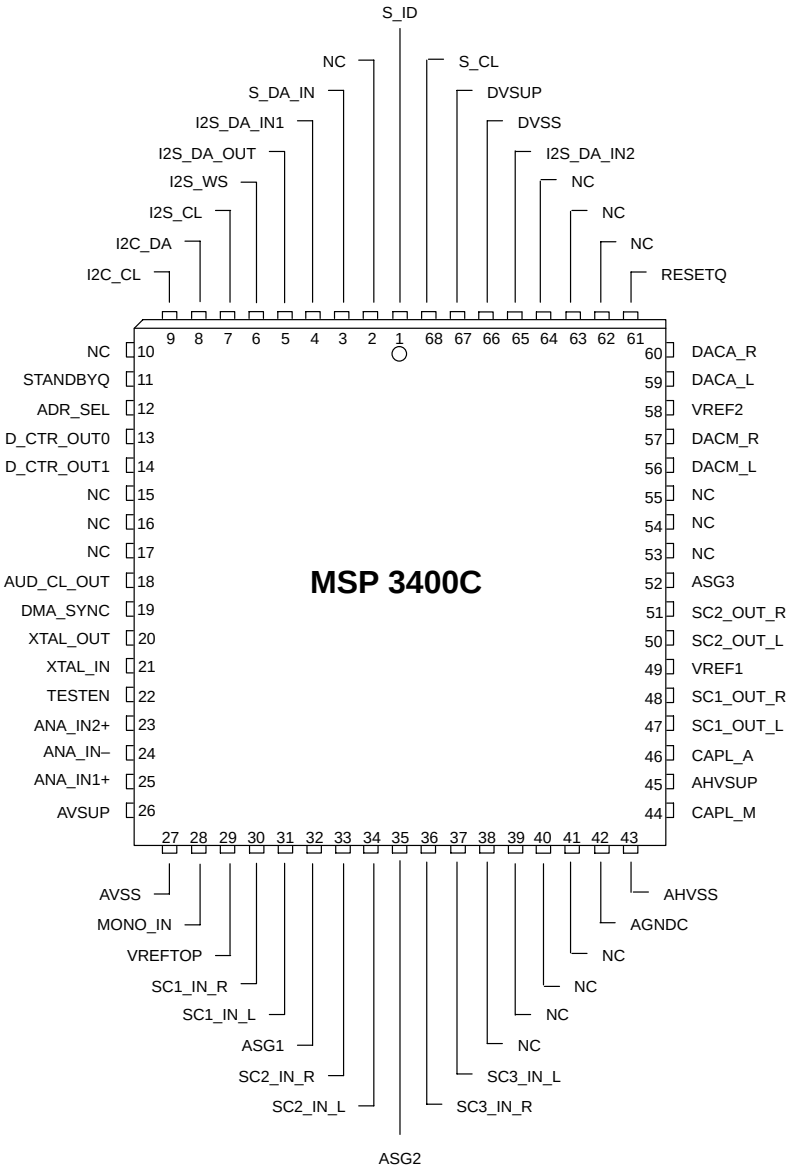


Fig. 8–5: 68-pin PLCC package

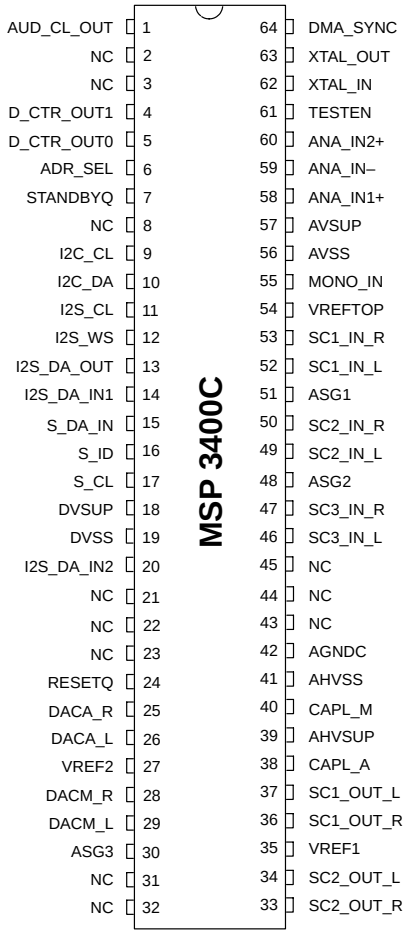


Fig. 8–6: 64-pin shrink PSDIP package

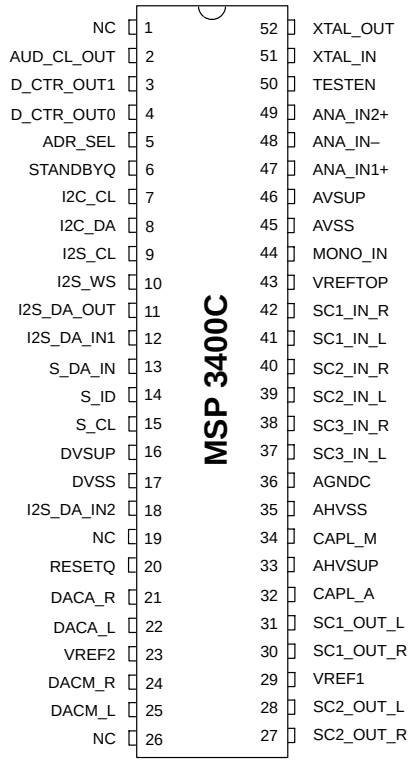


Fig. 8–7: 52-pin shrink PSDIP package

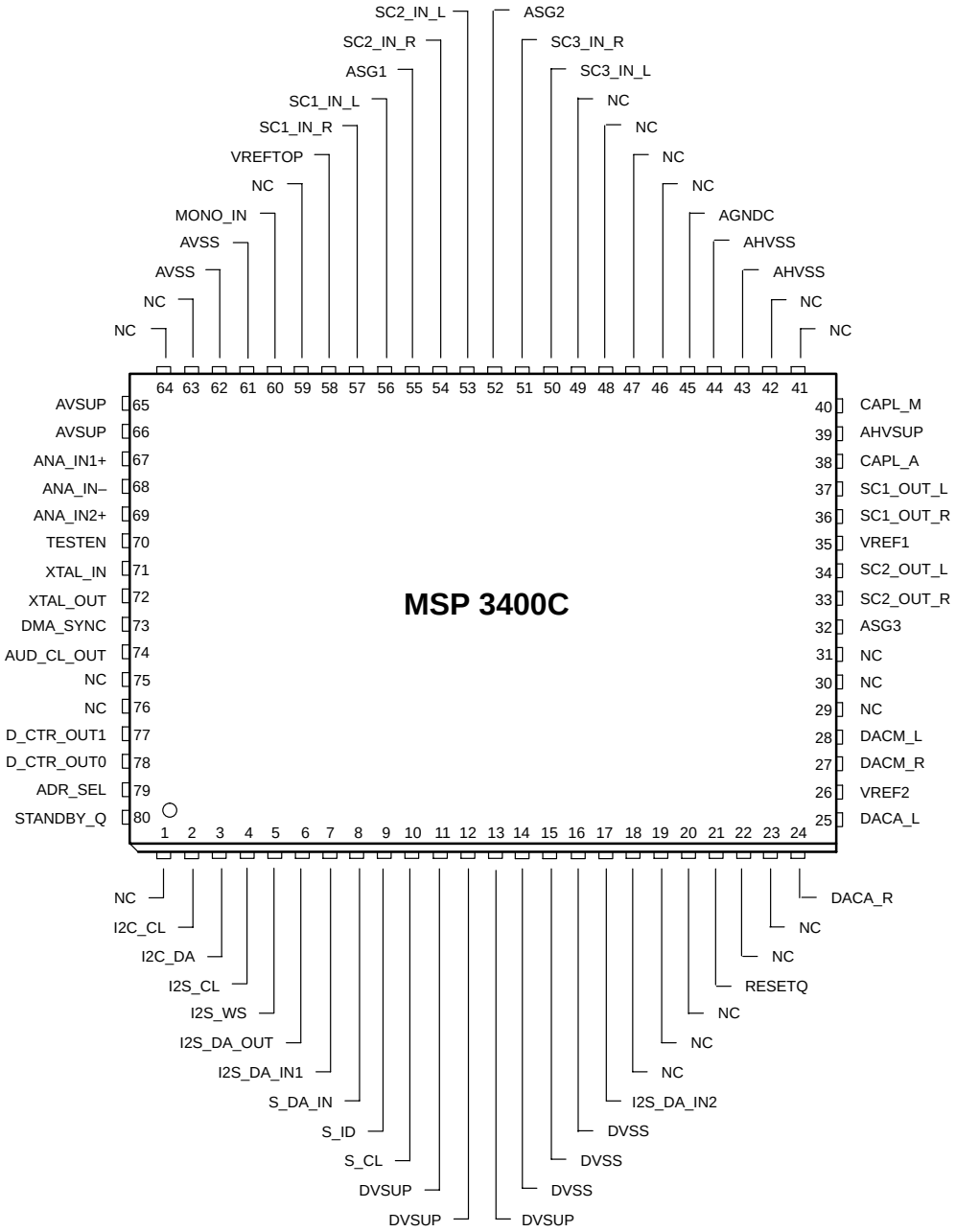


Fig. 8–8: 80-pin PQFP package

8.4. Pin Circuits

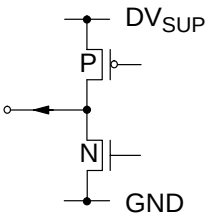


Fig. 8–9: Output Pins 1, 5, 13, 14, and 68
(S_ID, I²S_DA_OUT, D_CTR_OUT0/1, S_CL)

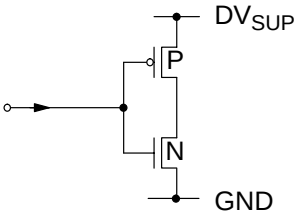


Fig. 8–10: Input Pins 4 and 65
(I²S_DA_IN1/2)

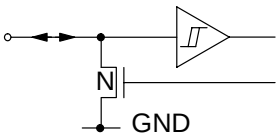


Fig. 8–11: Input/Output Pins 8 and 9
(I²C_DA, I²C_CL)

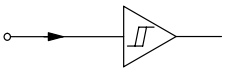


Fig. 8–12: Input Pins 11, 12, 61, and 62
(STANDBYQ, ADR_SEL, RESETQ, TESTEN)

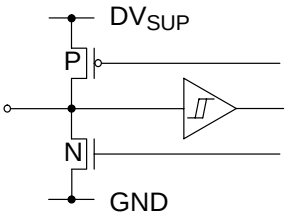


Fig. 8–13: Input/Output Pins 6 and 7
(I²S_WS, I²S_CL)

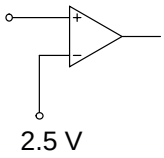


Fig. 8–14: Input Pin 19 (DMA_SYNC)

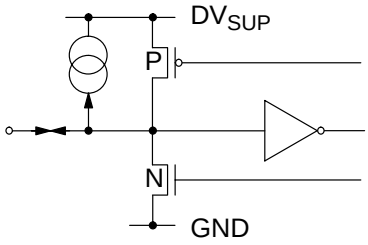


Fig. 8–15: Input Pin 3
(S_DA_IN)

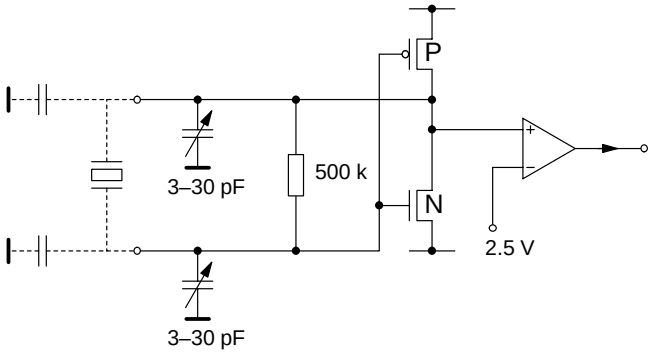


Fig. 8–16: Output/Input Pins 18, 20, and 21
(AUD_CL_OUT, XTALIN/OUT)

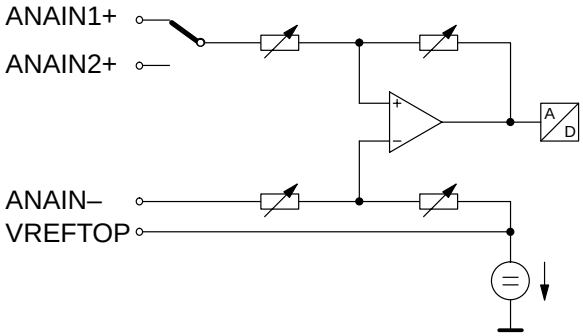


Fig. 8–17: Input Pins 23–25 and 29
(ANA_IN2+, ANA_IN–, ANA_IN1+, VREFTOP)

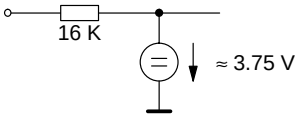


Fig. 8–18: Input Pin 28 (MONO_IN)

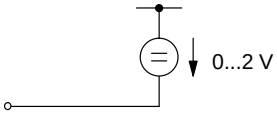


Fig. 8–19: Capacitor Pins 44 and 46 (CAPL_M, CAPL_A)

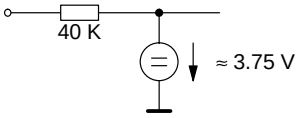


Fig. 8–20: Input Pins 30, 31, 33, 34, 36, and 37 (SC1–3_IN_L/R)

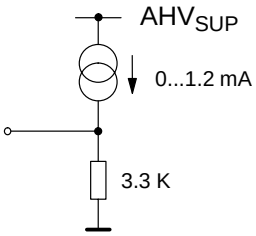


Fig. 8–21: Output Pins 56, 57, 59, and 60 (DACA_L/R, DACM_L/R)

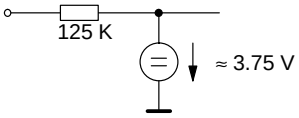


Fig. 8–22: Pin 42 (AGNDC)

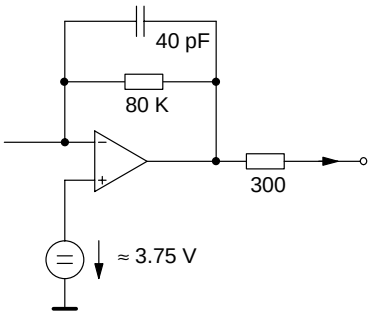


Fig. 8–23: Output Pins 47, 48, 50 and 51 (SC_1/2_OUT_L/R)

8.5. Electrical Characteristics

8.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	70	°C
T_S	Storage Temperature	–	–40	125	°C
V_{SUP1}	First Supply Voltage	AHVSUP	–0.3	9.0	V
V_{SUP2}	Second Supply Voltage	DVSUP	–0.3	6.0	V
V_{SUP3}	Third Supply Voltage	AVSUP	–0.3	6.0	V
dV_{SUP23}	Voltage between AVSUP and DVSUP	AVSUP, DVSUP	–0.5	0.5	V
P_{TOT}	Chip Power Dissipation PLCC68 without Heat Spreader	AHVSUP, DVSUP, AVSUP		1100	mW
V_{Idig}	Input Voltage, all Digital Inputs		–0.3	V_{SUP2}+0.3	V
I_{Idig}	Input Current, all Digital Pins	–	–20	+20	mA[1)]
V_{Iana}	Input Voltage, all Analog Inputs	SCn_IN_s,[2)] MONO_IN	–0.3	V_{SUP1}+0.3	V
I_{Iana}	Input Current, all Analog Inputs	SCn_IN_s,[2)] MONO_IN	–5	+5	mA[1)]
I_{Oana}	Output Current, all SCART Outputs	SCn_OUT_s[2)]	[3)], [4)]	[3)], [4)]	
I_{Oana}	Output Current, all Analog Outputs except SCART Outputs	DACp_s[2)]	[3)]	[3)]	
I_{Cana}	Output Current, other pins connected to capacitors	CAPL_p,[2)] AGNDC	[3)]	[3)]	

1) positive value means current flowing into the circuit
2) “n” means “1”, “2” or “3”, “s” means “L” or “R”, “p” means “M” or “A”
3) The Analog Outputs are short circuit proof with respect to First Supply Voltage and Ground.
4) Total chip power dissipation must not exceed absolute maximum rating.

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

8.5.2. Recommended Operating Conditions

(at T_A = 0 to 70 °C)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{SUP1}	First Supply Voltage	AHVSUP	7.6	8.0	8.4	V
V_{SUP2}	Second Supply Voltage	DVSUP	4.75	5.0	5.25	V
V_{SUP3}	Third Supply Voltage	AVSUP	4.75	5.0	5.25	V
V_{REIL}	RESET Input Low Voltage	RESETQ			0.45	V_{SUP2}
V_{REIH}	RESET Input High Voltage		0.8			V_{SUP2}
t_{REIL}	RESET Low Time after DVSUP Stable and Oscillator Startup		5			µs
V_{DMAIL}	Sync Input Low Voltage	DMA_SYNC			0.44	V_{SUP1}
V_{DMAIH}	Sync Input High Voltage		0.56			V_{SUP1}
t_{DMA}	Sync Input Frequency			18.0		kHz
R_{DMA}	Sync Input Clock High-Level Time		500			ns
V_{DIGIL}	Digital Input Low Voltage	STANDBYQ, ADR_SEL, TESTEN			0.25	V_{SUP2}
V_{DIGIH}	Digital Input High Voltage		0.75			V_{SUP2}
t_{STBYQ1}	STANDBYQ Setup Time before Turn-off of Second Supply Voltage	STANDBYQ, DVSUP	1			µs
I^2C-Bus Recommendations						
V_{IMIL}	I^2C-BUS Input Low Voltage	I^2C_CL, I^2C_DA			0.3	V_{SUP2}
V_{IMIH}	I^2C-BUS Input High Voltage		0.6			V_{SUP2}
f_{IM}	I^2C-BUS Frequency	I^2C_CL			1.0	MHz
t_{I2C1}	I^2C START Condition Setup Time	I^2C_CL, I^2C_DA	120			ns
t_{I2C2}	I^2C STOP Condition Setup Time		120			ns
t_{I2C3}	I^2C-Clock Low Pulse Time	I^2C_CL	500			ns
t_{I2C4}	I^2C-Clock High Pulse Time		500			ns
t_{I2C5}	I^2C-Data Setup Time Before Rising Edge of Clock	I^2C_CL, I^2C_DA	55			ns
t_{I2C6}	I^2C-Data Hold Time after Falling Edge of Clock		55			ns
V_{I2SIL}	I^2S-Data Input Low Voltage	I2S_DA_IN1/2			0.25	V_{SUP2}
V_{I2SIH}	I^2S-Data Input High Voltage		0.75			V_{SUP2}

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
t_{I2S1}	I^2S-Data Input Setup Time before Rising Edge of Clock	I2S_DA_IN1/2, I2S_CL	20			ns
t_{I2S2}	I^2S-Data Input Hold Time after Falling Edge of Clock		0			ns
V_{I2SIDL}	I^2S-Input Low Voltage when MSP 3400C in I2S-Slave-Mode	I2S_CL, I2S_WS			0.25	V_{SUP2}
V_{I2SIDH}	I^2S-Input High Voltage when MSP 3400C in I2S-Slave-Mode		0.75			V_{SUP2}
f_{I2SCL}	I^2S-Clock Input Frequency when MSP 3400C in I2S-Slave-Mode	I2S_CL		1.024		MHz
R_{I2SCL}	I^2S-Clock Input Ratio when MSP 3400C in I2S-Slave-Mode		0.9		1.1	
f_{I2SWS}	I^2S-Wordstrobe Input Frequency when MSP 3400C in I2S-Slave-Mode	I2S_WS		32.0		kHz
t_{I2SWS1}	I^2S-Wordstrobe Input Setup Time before Rising Edge of Clock when MSP 3400C in I2S-Slave-Mode	I2S_WS, I2S_CL	60			ns
t_{I2SWS2}	I^2S-Wordstrobe Input Hold Time after Falling Edge of Clock when MSP 3400C in I2S-Slave-Mode		0			ns
V_{SBUSIL}	SBUS-Data Input Low Voltage	S_DA_IN			0.6	V
I_{SBUSIL}	SBUS-Data Input Low Current		0.9	1.7	3.2	mA
$V_{SBUSTRIG}$	SBUS-Data Input Trigger Voltage		0.8		1.2	V
t_{SBUS1}	SBUS-Data Input Setup Time before Rising Edge of Clock	S_DA_IN, S_CL	10			ns
t_{SBUS2}	SBUS-Data Input Hold Time after Falling Edge of Clock		0			ns
Crystal Recommendations for Master-Slave Application						
f_P	Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
f_{TOL}	Accuracy of Adjustment		–20		+20	ppm
D_{TEM}	Frequency Variation versus Temperature		–20		+20	ppm
R_R	Series Resistance			8	25	Ω
C_0	Shunt (Parallel) Capacitance			6.2	7.0	pF
C_1	Motional (Dynamic) Capacitance		19	24		fF

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Load Capacitance Recommendations for Master-Slave Applications						
C_L	External Load Capacitance[2)]	XTAL_IN, XTAL_OUT	PSDIP PLCC	1.5 3.3		pF pF
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25°C)		18.431		18.433	MHz
Crystal Recommendations for FM Application (No Master-Slave Mode possible)						
f_P	Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
f_{TOL}	Accuracy of Adjustment		–100		+100	ppm
D_{TEM}	Frequency Variation versus Temperature		–50		+50	ppm
R_R	Series Resistance			8	25	Ω
C_0	Shunt (Parallel) Capacitance			6.2	7.0	pF
Load Capacitance Recommendations for FM Application (No Master-Slave Mode possible)						
C_L	External Load Capacitance[2)]	XTAL_IN, XTAL_OUT	PSDIP PLCC	1.5 3.3		pF pF
Amplitude Recommendation for Operation with External Clock Input (C_{load} after reset = 22 pF)						
V_{XCA}	External Clock Amplitude	XTAL_IN	0.7			V_{pp}
Analog Input and Output Recommendations						
C_{AGNDC}	AGNDC-Filter-Capacitor	AGNDC	–20%	3.3		µF
	Ceramic Capacitor in Parallel		–20%	100		nF
C_{inSC}	DC-Decoupling Capacitor in front of SCART Inputs	SCn_IN_s[1)]	–20%	330	+20%	nF
V_{inSC}	SCART Input Level				2.0	V_{RMS}
V_{inMONO}	Input Level, Mono Input	MONO_IN			2.0	V_{RMS}
R_{LSC}	SCART Load Resistance	SCn_OUT_s[1)]	10			kΩ
C_{LSC}	SCART Load Capacitance				6.0	nF
C_{VMA}	Main/AUX Volume Capacitor	CAPL_M, CAPL_A		10		µF
C_{FMA}	Main/AUX Filter Capacitor	DACM_s, DACA_s[1)]	–10%	1	+10%	nF

1) "n" means "1", "2" or "3", "s" means "L" or "R", "p" means "M" or "A"

2) External capacitors at each crystal pin to ground are required. They are necessary to tune the open-loop frequency of the internal PLL and to stabilize the frequency in closed-loop operation. The higher the capacitors, the lower the clock frequency results. The nominal free running frequency should match 18.432 MHz as closely as possible. Due to different layouts of customer PCBs, the matching capacitor size should be defined in the application. The suggested values (1.5 pF/3.3 pF) are figures based on experience with various PCB layouts.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Recommendations for Analog Sound IF Input Signal						
$C_{VREFTOP}$	VREFTOP-Filter-Capacitor	VREFTOP	–20%	10		µF
	Ceramic Capacitor in Parallel		–20%	100		nF
V_{IF}	Analog Input Range (Complete Sound IF, 0 – 9 MHz)	ANA_IN1+, ANA_IN2+, ANA_IN–	0.14	0.8	3	Vpp
R_{FM}	Ratio: FM-Main/FM-Sub Satellite			7		dB
$R_{FM1/FM2}$	Ratio: FM1/FM2 German FM-System			7		dB
R_{FC}	Ratio: Main FM Carrier/Color Carrier		15	–	–	dB
R_{FV}	Ratio: Main FM Carrier/Luma Components		15	–	–	dB
PR_{IF}	Passband Ripple		–	–	±2 dB	dB
SUP_{HF}	Suppression of Spectrum Above 9.0 MHz		15		–	dB
FM_{MAX}	Maximum FM-Deviation (apprx.) normal mode high deviation mode				 ±192 ±360	kHz

8.5.3. Characteristics at T_A = 0 to 70 °C, f_{CLOCK} = 18.432 MHz

(Typical values are measured at T_A = 25 °C, AHVSUP = 8 V, DVSUP = 5 V, AVSUP = 5 V.)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
DCO							
f_{CLOCK}	Clock Input Frequency	XTAL_IN		18.432		MHz	
D_{CLOCK}	Clock High to Low Ratio		45		55	%	
t_{JITTER}	Clock Jitter (verification not provided in production test)				50	ps	
V_{xtalDC}	DC-Voltage Oscillator			2.5		V	
$t_{Startup}$	Oscillator Startup Time at VDD Slew-rate of 1 V / 1 µs	XTAL_IN, XTAL_OUT		0.4	2.0	ms	
Power Supply							
I_{SUP1A}	First Supply Current (active) Analog Volume for Main and Aux at 0dB Analog Volume for Main and Aux at –30dB at T_j = 27 °C	AHVSUP	 8.2 5.6	 14.8 10.0	 22.0 15.0	 mA mA	f = 18.432 MHz AHVSUP = 8 V DVSUP = 5 V AVSUP = 5 V
I_{SUP2A}	Second Supply Current (active)	DVSUP	60	65	70	mA	f = 18.432 MHz DVSUP = 5 V
I_{SUP3A}	Third Supply Current (active)	AVSUP		25		mA	f = 18.432 MHz AVSUP = 5 V
I_{SUP1S}	First Supply Current (standby mode) at T_j = 27 °C	AHVSUP	2.8	5.0	7.2	mA	STANDBYQ = low VSUP = 8 V
Audio Clock Output							
V_{APUAC}	Audio Clock Output AC Voltage	AUD_CL_OUT	1.2			V_{pp}	40 pF load
V_{APUDC}	Audio Clock Output DC Voltage		0.4		0.6	V_{SUP1}	
Digital Output							
V_{DCTROL}	Digital Output Low Voltage	D_CTR_OUT0 D_CTR_OUT1			0.4	V	I_{DDCTR} = 1 mA
V_{DCTROH}	Digital Output High Voltage		4.0			V	I_{DDCTR} = –1 mA
I^2C Bus							
V_{IMOL}	I^2C-Data Output Low Voltage	I^2C_DA	0.4			V	I_{iMOL} = 3 mA
I_{IMOH}	I^2C-Data Output High Current				1	µA	V_{IMOH} = 5 V
t_{IMOL1}	I^2C-Data Output Hold Time after Falling Edge of Clock	I^2C_DA, I^2C_CL	15			ns	
t_{IMOL2}	I^2C-Data Output Setup Time before Rising Edge of Clock		100			ns	f_{IM} = 1 MHz DVSUP = 5 V
SBus							
f_{SB}	SBUS-Clock Frequency	S_CL		4608		kHz	DVSUP = 5 V
$t_{S1/S2}$	SBUS-Clock High/Low-Ratio		0.9	1.0	1.1	ns	
t_{S3}	SBUS Setup Time before Ident End Pulse	S_CL, S_ID	210			ns	DVSUP = 5.25 V
f_{SIO}	SBUS Ident frequency	S_ID		32		kHz	
t_{S6}	SBUS-Ident End Pulse Time		210			ns	DVSUP = 5.25 V

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
I^2S Bus							
V_{I2SOL}	I^2S Output Low Voltage	I2S_WS, I2S_CL, I2S_DA_OUT			0.4	V	I_{I2SOL} = 1 mA
V_{I2SOH}	I^2S Output High Voltage		4.0			V	I_{I2SOH} = –1 mA
f_{I2SCL}	I^2S-Clock Output Frequency	I2S_CL		1204		kHz	DVSUP = 5 V
f_{I2SWS}	I^2S-Wordstrobe Output Frequency	I2S_WS		32.0		kHz	DVSUP = 5 V
$t_{I2S1/I2S2}$	I^2S-Clock High/Low-Ratio	I2S_CL	0.9	1.0	1.1		
t_{I2S3}	I^2S-Data Setup Time before Rising Edge of Clock	I2S_CL, I2S_DA_OUT	200			ns	DVSUP = 4.75 V
t_{I2S4}	I^2S-Data Hold Time after Falling Edge of Clock		12			ns	DVSUP = 5.25 V
t_{I2S5}	I^2S-Wordstrobe Setup Time before Rising Edge of Clock	I2S_CL, I2S_WS	100			ns	DVSUP = 4.75 V
t_{I2S6}	I^2S-Wordstrobe Hold Time after Falling Edge of Clock		50			ns	DVSUP = 5.25 V
Analog Ground							
V_{AGNDC0}	AGNDC Open Circuit Voltage	AGNDC	3.64	3.73	3.84	V	$R_{load} \geq 10\ M\Omega$
R_{outAGN}	AGNDC Output Resistance at T_j = 27 °C from T_A = 0 to 70 °C		70 70	125	180 180	kΩ kΩ	3 V ≤ V_{AGNDC} ≤ 4 V
Analog Input Resistance							
R_{inSC}	SCART Input Resistance at T_j = 27 °C from T_A = 0 to 70 °C	SCn_IN_s[1)]	25 25	40	58 58	kΩ kΩ	f_{signal} = 1 kHz, I ≤ 0.05 mA
R_{inMONO}	MONO Input Resistance at T_j = 27 °C from T_A = 0 to 70 °C	MONO_IN	10 10	16	23 23	kΩ kΩ	f_{signal} = 1 kHz, I ≤ 0.1 mA
Audio Analog-to-Digital-Converter							
V_{AICL}	Analog Input Clipping Level for Analog-to-Digital-Conversion	SCn_IN_s,[1)] MONO_IN	2.02	2.12	2.22	V_{RMS}	f_{signal} = 1 kHz
SCART Outputs							
R_{outSC}	SCART Output Resistance at T_j = 27 °C from T_A = 0 to 70 °C	SCn_OUT_s[1)]	0.20 0.20	0.33	0.46 0.5	kΩ kΩ	f_{signal} = 1 kHz, I = 0.1 mA
dV_{OUTSC}	Deviation of DC-Level at SCART Output from AGNDC Voltage		–70		+70	mV	
A_{SCtoSC}	Gain from Analog Input to SCART Output	SCn_IN_s[1)] MONO_IN → SCn_OUT_s[1)]	–1.0	0	+0.5	dB	f_{signal} = 1kHz
$f_{rSCtoSC}$	Frequency Response from Analog Input to SCART Output bandwidth: 0 to 20000 Hz		–0.5	0	+0.5	dB	with respect to 1 kHz
V_{outSC}	Signal Level at SCART-Output during full-scale digital input signal from DSP	SCn_OUT_s[1)]	1.8	1.9	2.0	V_{RMS}	f_{signal} = 1 kHz

1) “n” means “1”, “2” or “3”, “s” means “L” or “R”, “p” means “M” or “A”

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Main and AUX Outputs							
R_{outMA}	Main/AUX Output Resistance at T_j = 27 °C from T_A = 0 to 70 °C	DACp_s[1]	2.1 2.1	3.3	4.6 5.0	kΩ kΩ	f_{signal} = 1 kHz, I = 0.1 mA
$V_{outDCMA}$	DC-Level at Main/AUX-Output for Analog Volume at 0 dB for Analog Volume at –30 dB		1.74 –	1.94 61	2.14 –	V mV	
V_{outMA}	Signal Level at Main/AUX-Output during full-scale digital input signal from DSP for Analog Volume at 0 dB		1.23	1.37	1.51	V_{RMS}	f_{signal} = 1 kHz
Analog Performance							
SNR	Signal-to-Noise Ratio						
	from Analog Input to DSP	MONO_IN, SCn_IN_s[1]	85	88		dB	Input Level = –20 dB with resp. to V_{AICL}, f_{sig} = 1 kHz, equally weighted 20 Hz ... 16 kHz[2]
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s[1] → SCn_OUT_s[1]	93	96		dB	Input Level = –20 dB, f_{sig} = 1 kHz, equally weighted 20 Hz ... 20 kHz
	from DSP to SCART Output	SCn_OUT_s[1]	85	88		dB	Input Level = –20 dB, f_{sig} = 1 kHz, equally weighted 20 Hz ... 15 kHz[3]
	from DSP to Main/AUX-Output for Analog Volume at 0 dB for Analog Volume at –30 dB	DACp_s[1]	85 78	88 83		dB dB	Input Level = –20 dB, f_{sig} = 1 kHz, equally weighted 20 Hz ... 15 kHz[3]
THD	Total Harmonic Distortion						
	from Analog Input to DSP	MONO_IN, SCn_IN_s[1]			0.05	%	Input Level = –3 dBr with resp. to V_{AICL}, f_{sig} =1kHz, equally weighted 20 Hz ...16 kHz, R_{Load} = 30 kΩ[2]
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s → SCn_OUT_s[1]		0.01	0.03	%	Input Level = –3 dBr, f_{sig} = 1 kHz, equally weighted 20 Hz ... 20 kHz, R_{Load} = 30 kΩ
	from DSP to SCART Output	SCn_OUT_s[1]		0.01	0.03	%	Input Level = –3 dBr, f_{sig} = 1 kHz, equally weighted 20 Hz ... 16 kHz, R_{Load} = 30 kΩ[3]
	from DSP to Main or AUX Output	DACA_s, DACM_s[1]		0.01	0.03	%	Input Level = –3 dBr, f_{sig} = 1 kHz, equally weighted 20 Hz ... 16 kHz, R_{Load} = 30 kΩ[3]

1) "n" means "1", "2" or "3", "s" means "L" or "R", "p" means "M" or "A"
2) DSP measured at I^2S-Output
3) DSP Input at I^2S-Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
XTALK	Crosstalk attenuation – PLCC68 – PSDIP64						Input Level = –3 dB, f_{sig} = 1 kHz, unused analog inputs connected to ground by Z<1 kΩ
	between left and right channel within SCART Input/Output pair (L→R, R→L)						equally weighted 20 Hz ... 20 kHz
	SCn_IN → SCn_OUT[1]	PLCC68 PSDIP64	80 80			dB dB	[2]
	SCn_IN → DSP[1]	PLCC68 PSDIP64	80 80			dB dB	
	DSP → SCn_OUT[1]	PLCC68 PSDIP64	80 80			dB dB	[3]
	between left and right channel within Main or AUX Output pair						equally weighted 20 Hz ... 16 kHz
	DSP → DACp[1]	PLCC68 PSDIP64	80 75			dB dB	[3]
	between SCART Input/Output pairs[1] D = disturbing program O = observed program						(equally weighted 20 Hz ... 20 kHz) same signal source on left and right disturbing channel, effect on each observed output channel
	D: MONO/SCn_IN → SCn_OUT O: MONO/SCn_IN → SCn_OUT[1]	PLCC68 PSDIP64	100 100			dB dB	
	D: MONO/SCn_IN → SCn_OUT O: or unsel. MONO/SCn_IN → DSP[1]	PLCC68 PSDIP64	95 95			dB dB	[2]
	D: MONO/SCn_IN → SC1_OUT O: DSP → SCn_OUT[1]	PLCC68 PSDIP64	100 100			dB dB	[3]
	D: MONO/SCn_IN → unselected O: DSP → SC1_OUT[1]	PLCC68 PSDIP64	100 100			dB dB	[3]
	Crosstalk between Main and AUX Output pairs DSP → DACp[1]	PLCC68 PSDIP64	95 90			dB dB	(equally weighted 20 Hz ... 16 kHz)[3] same signal source on left and right disturbing channel, effect on each observed output channel
	Crosstalk from Main or AUX Output to SCART Output and vice versa D = disturbing program O = observed program						(equally weighted 20 Hz ... 20 kHz) same signal source on left and right disturbing channel, effect on each observed output channel
	D: MONO/SCn_IN/DSP → SCn_OUT O: DSP → DACp[1]	PLCC68 PSDIP64	90 85			dB dB	SCART output load resistance 10 kΩ
	D: MONO/SCn_IN/DSP → SCn_OUT O: DSP → DACp[1]	PLCC68 PSDIP64	95 85			dB dB	SCART output load resistance 30 kΩ
	D: DSP → DACp O: MONO/SCn_IN → SCn_OUT[1]	PLCC68 PSDIP64	100 95			dB dB	[3]
	D: DSP → DACp O: DSP → SCn_OUT[1]	PLCC68 PSDIP64	100 95			dB dB	

1) "n" means "1", "2" or "3", "s" means "L" or "R", "p" means "M" or "A"
2) DSP measured at I^2S-Output
3) DSP Input at I^2S-Input

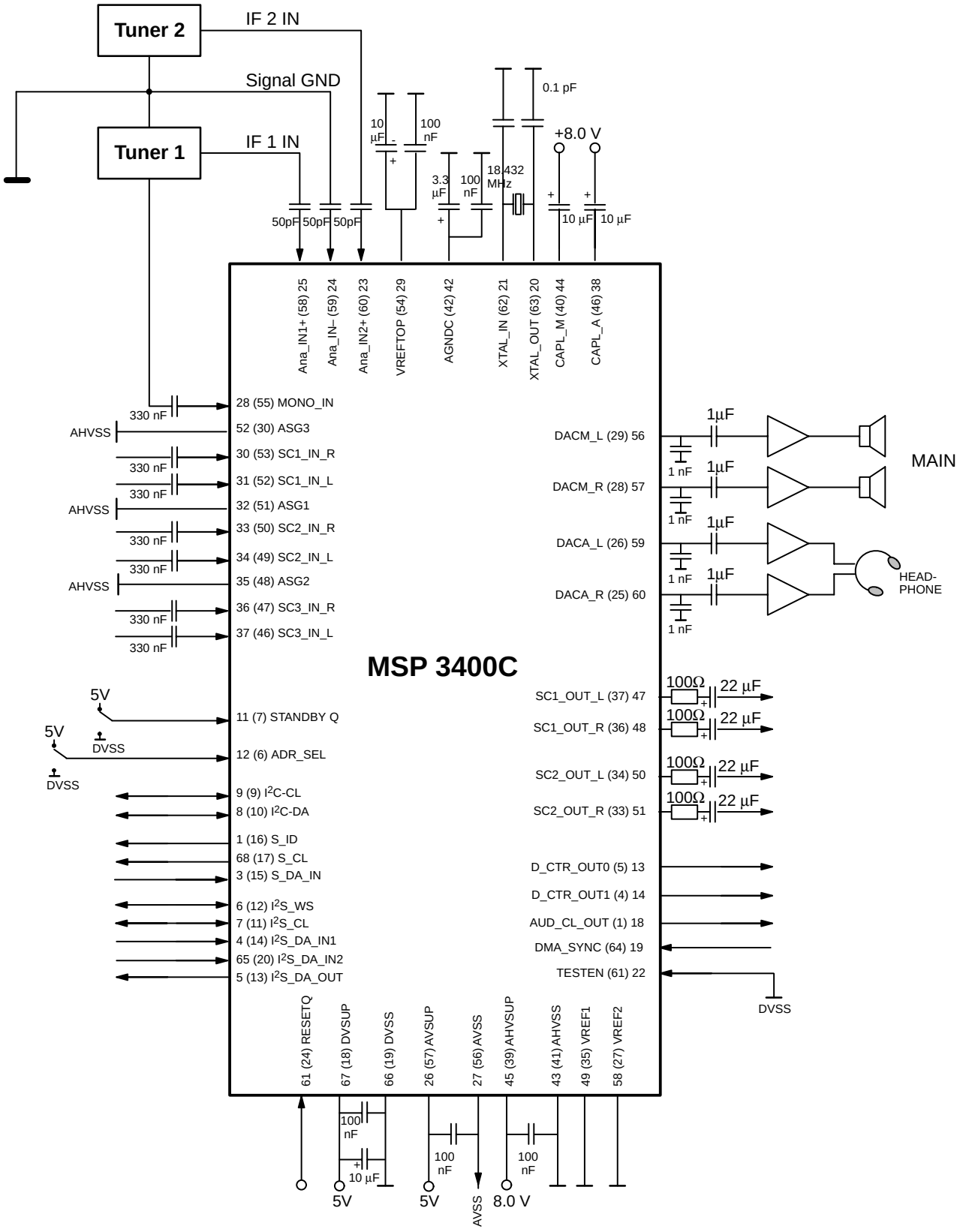
Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
PSRR: rejection of noise on AHVSUP at 1 kHz							
PSRR	AGNDC	AGNDC		80		dB	
	From analog Input to DSP	MONO_IN SCn_IN_s[1)]		69		dB	
	From analog Input to SCART Output	MONO_IN SCn_IN_s,[1)] SCn_OUT_s[1)]		74		dB	
	From DSP to SCART Output	SCn_OUT_s[1)]		70		dB	
	From DSP to MAIN/AUX Output	DACp_s[1)]		80		dB	
Sound IF Input Section							
$DC_{VREFTOP}$	DC voltage at VREFTOP	VREFTOP	2.4	2.6	2.7	V	$V_{SUPANALOG}$ = 5 V $R_{Load} \geq 10$ MΩ
R_{IFIN}	Input Impedance	ANA_IN1+, ANA_IN2+, ANA_IN–	1.5 10.5	2 14.1	2.5 17.6	kOhm	AGC = +20 dB AGC = +3 dB $R_{Load} \geq 10$ MΩ
DC_{ANA_IN}	DC voltage on IF inputs		1.3	1.5	1.7	V	AVSUP = 5 V $R_{Load} \geq 10$ MΩ
$XTALK_{IF}$	Crosstalk attenuation		40	t.b.d.	–	dB	f_{sig} = 1 MHz, Input Level = –2 dBr
BW_{IF}	3 dB Bandwidth		10	–	–	MHz	Input Level = –2 dBr
AGC	AGC step width		t.b.d.	0.85	t.b.d.	dB	f_{sig} = 1 MHz, Input Level = –2 dBr

1) “n” means “1”, “2” or “3”, “s” means “L” or “R”, “p” means “M” or “A”

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Overall Performance							
S/N_{FM}	FM input to Main/AUX/SCART Output	DACp_s, SCn_OUT_s[1)]	70		–	dB	1 FM-carrier 5.5 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS, unweighted 0 to 15 kHz; full input range
S/N_{D2MAC}	Signal to Noise ratio of D2MAC baseband signal on Main/AUX/ SCART outputs		TBD		–	dB	
THD_{FM}	Total Harmonic Distortion + Noise of FM demodulated signal on Main/AUX/SCART output		–		0.3	%	1 FM-carrier 5.5 MHz, 1kHz, 50 µs; 40 kHz deviation; full input range
THD_{D2MAC}	Total Harmonic Distortion + Noise of D2MAC baseband signal for Main/AUX/SCART output		–	0.01	0.1	%	2.12 kHz, Modulator input level = 0 dBref
dV_{FMOUT}	Tolerance of output voltage of FM demodulated signal		–1.5		+1.5	dB	1 FM-carrier, 50 µs, 1 kHz 40 kHz deviation; RMS
$dV_{D2MACOUT}$	Tolerance of output voltage of D2MAC baseband signal		–1.5		+1.5	dB	2.12 kHz, Modulator input level = 0 dBref
fR_{FM}	FM frequency response on Main/ AUX/SCART outputs, bandwidth 20 to 15000 Hz		–1.0		+1.0	dB	1 FM-carrier 5.5 MHz, 50 µs, Modulator input level = –14.6 dBref; RMS
fR_{D2MAC}	D2MAC frequency response on Main/AUX/SCART outputs, bandwidth 20 to 15000 Hz		–1.0		+1.0	dB	Modulator input level = –12 dB dBref; RMS
SEP_{FM}	FM channel separation (Stereo)		50			dB	2 FM-carriers 5.5/5.74 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS
SEP_{D2MAC}	D2MAC channel separation (Stereo)		80			dB	
$XTALK_{FM}$	FM crosstalk attenuation (Dual)		80			dB	2 FM-carriers 5.5/5.74 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS
$XTALK_{D2MAC}$	D2MAC crosstalk attenuation (Dual)		80			dB	

1) “n” means “1”, “2” or “3”, “s” means “L” or “R”, “p” means “M” or “A”

9. Application of the MSP 3400C



Note: Pin numbers refer to PLCC packages, pin numbers for PSDIP packages in brackets.
not connected pins are 2,10,15,16,17,38,39,40,41,53,54,55,62,63,64 (2,3,8,21,22,23,31,32,43,44,45)

10. DMA Application

Fig. 10–1 shows an example for the D2MAC application with the MSP 3400 or MSP 3400C. To obtain the optimal amplitude and phase conditions for the clock input of AMU, DMA 2386, and DMA 2381, it is recommended to use a clock inverter circuit, as shown below right, a minimum gain of 1.0 at 18.432 MHz and an output phase as specified in Fig. 10–2.

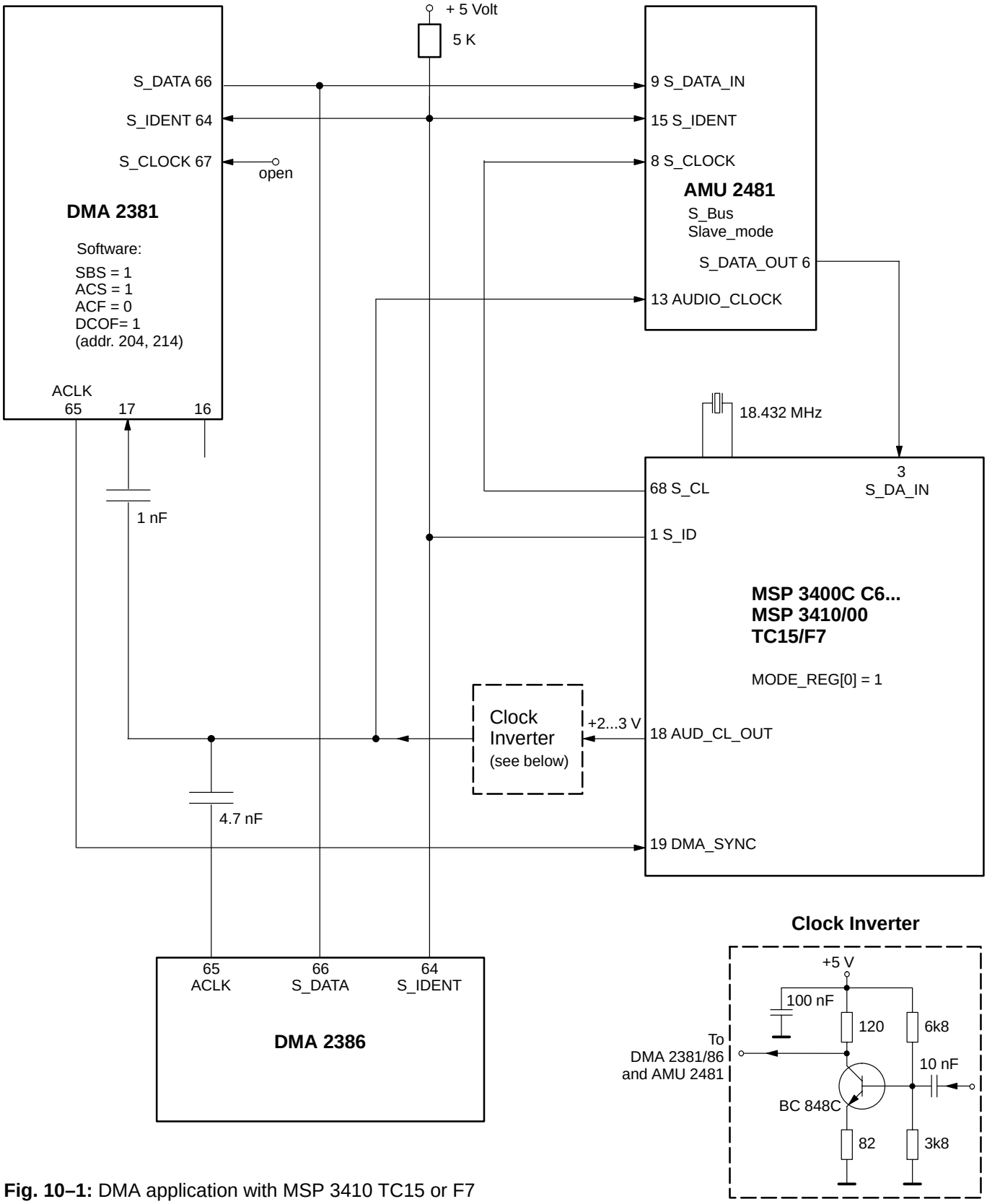


Fig. 10–1: DMA application with MSP 3410 TC15 or F7

Note: Pin numbers refer to PLCC packages for DMA 2381 and MSP 3400C and to PSDIP package for AMU 2481

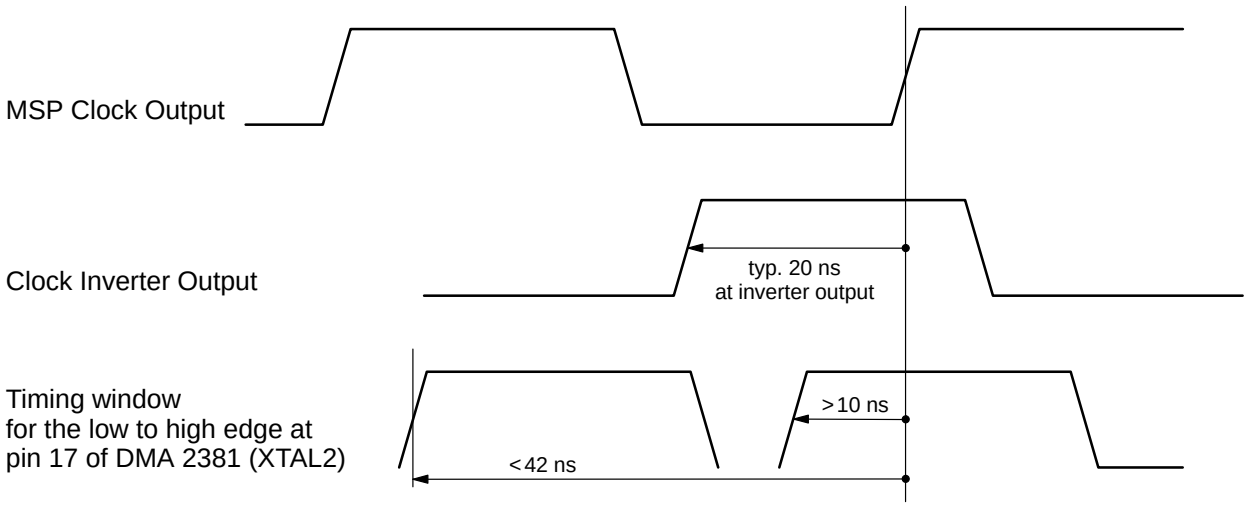


Fig. 10–2: Timing requirements for the clock signal at the DMA 2381 clock input

In the following table, the input/output clock-specification of the D2MAC circuit is shown.

Table 10–1: Clock input and output specification for MSPs

	MSP 3400C >C6 new Version	**MSP 3410/00 TC27** new Version	**MSP 3410/00 TC15** actual Version
XTAL_IN min (minimum amplitude)	>0.7 Vpp	>0.7 Vpp	>0.7 Vpp
C input (after Reset)	22 pF	22 pF	31 pF
AUD_CL_OUT min with C load	>1.2 Vpp 40 pF	>1.2 Vpp 40 pF	>1.0 Vpp 43 pF
Rout (HF) typ.	150 Ω	120 Ω	120 Ω

Table 10–2: Clock input and output specification for ICs connected to MSP

	DMA 2381	**DMA 2386**	**AMU2481**
XTAL_IN min Clock-in min (minimal amplitude)	>0.7 Vpp	>0.7 Vpp	>0.7 Vpp
C input	24 pF 10 pF with: Adr. 204,14=1	7pF	7pF

For the DMA_SYNC input specification of the MSP, please refer to page 54 “V_{DMAIL}, V_{DMAIH}.”

11. MSP Application with External Clock

If for some reason, e.g. to spare the cost of an additional crystal, the MSP receives the 18.432 MHz clock from an external source, for example from an other MSP, the following circuit can be used. For input/output specification see also Table 10–1.

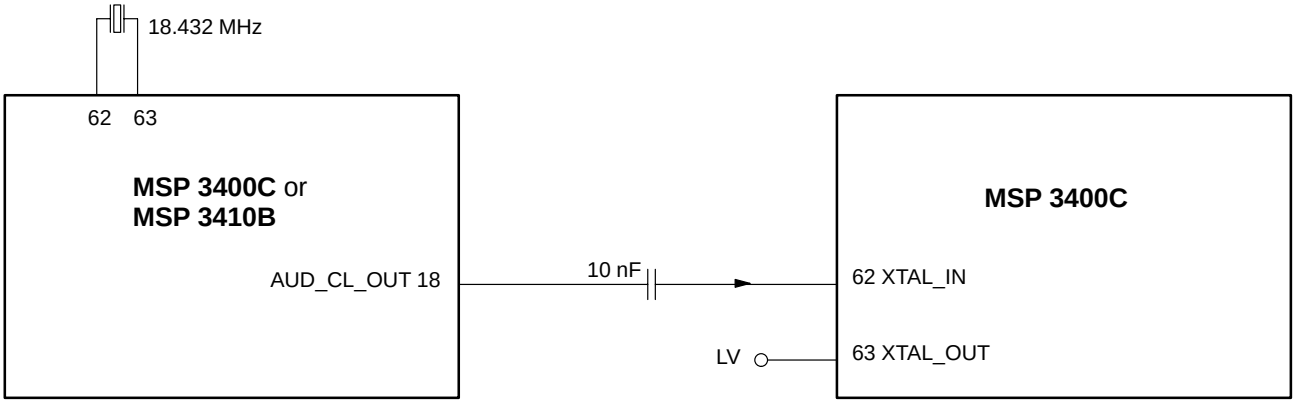
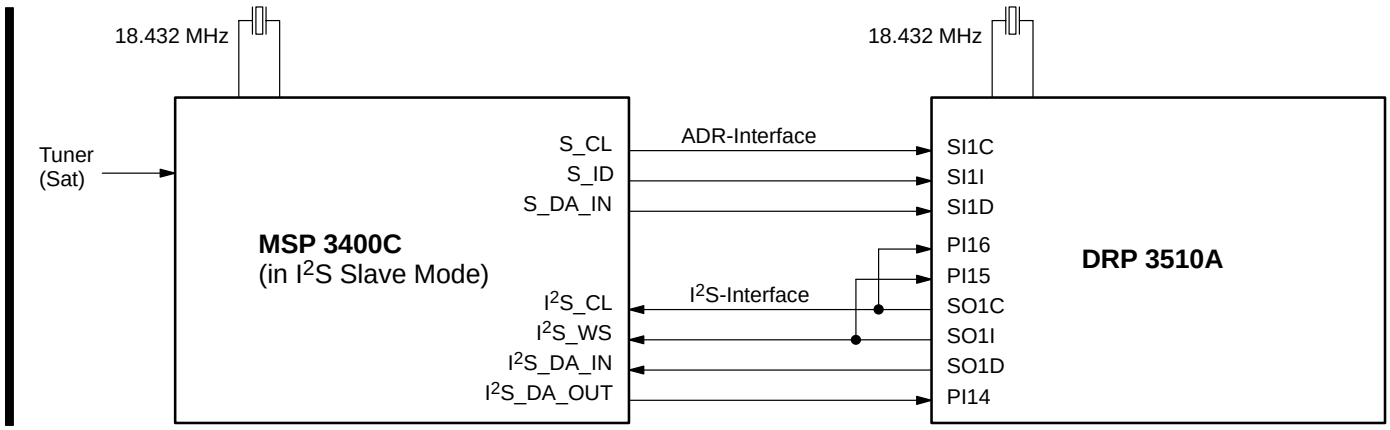


Fig. 11–1: MSP 3400C with external clock

12. ADR Application



13. I²S Bus in Master/Slave Configuration with Standby Mode

In a master/slave application, both MSP, after power up and reset, will start as master by default. This means that before the slave MSP is set to slave-mode, relatively large current-pulses (~20 mA) in the I2S_CL and I2S_WS lines can cause some crackling noise during startup time, if the the MSP is demuted before the slave MSP is set to slave mode.

These high current pulses are also possible, if the active I2S_CL and I2S_WS outputs of the master MSP are clipped by the correspondent inputs of the slave MSP, which is switched to standby mode.

To avoid this, it is recommended, that the I2S-bus lines I2S_CL and I2S_WS are current-limited to about 5 mA with series resistors of about 390 Ω (330...470 Ω).

Fig. 13–1 depicts the recommended application circuit for two MSP 3410/00 or MSP 3400C, which are connected via I2S Bus in a master/slave configuration, and where the slave MSP can be switched in standby mode (+5 Volt power is switched off).

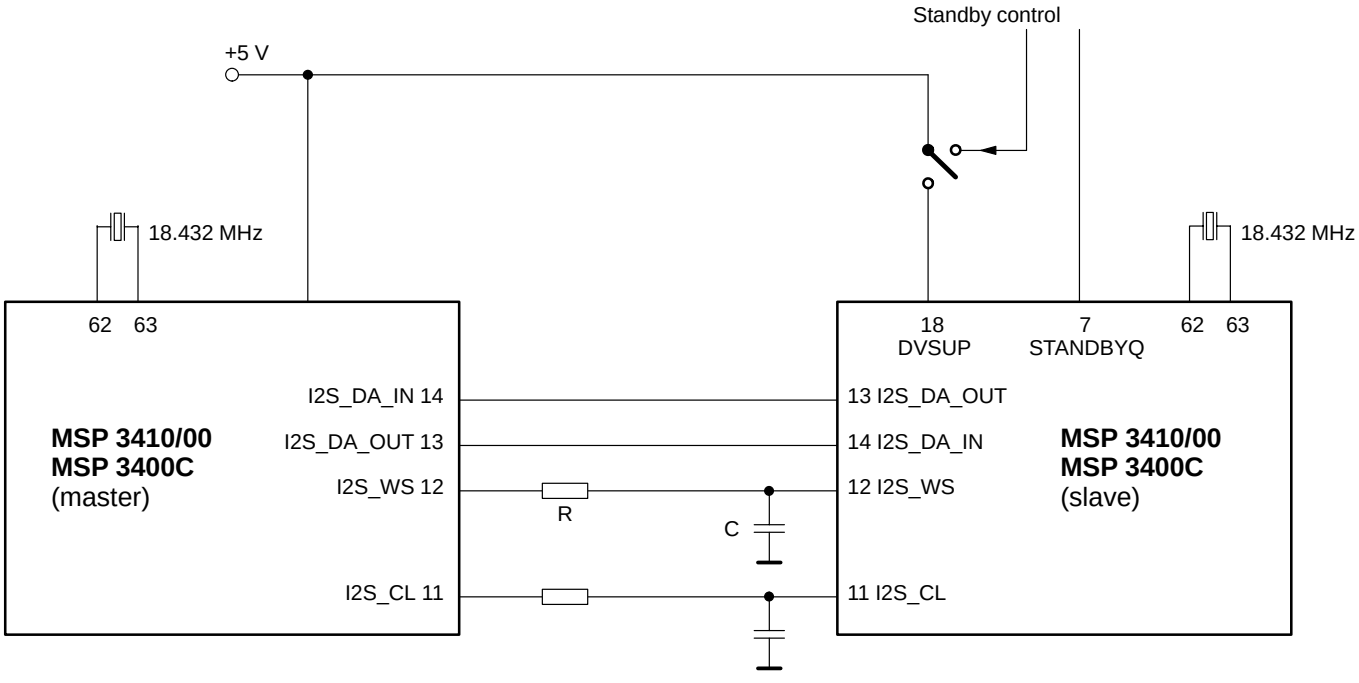


Fig. 13–1: I²S master/slave application

14. APPENDIX A: Technical Code History

TC01

First Release, compatible with MSP3410 and MSP 3400. Date: June 1994.

TC04

Emulator version for software development.

Version B5

New Features:
1. Equalizer
2. Improved identification
3. Improved adaptive deemphasis

Version C6

New Features:
1. Adjustable Stereo Basewidth Enlargement (SBE) and switchable Pseudo Stereo Effect (SBE)
2. New Channel Matrix Modes (Mono, Sum/Dif, etc)
3. New Audio Clock Output Driver
4. Fast mute (Volume)
5. Clipping mode (Volume)
6. Sub dB steps for Volume, Bass, Treble, Equalizer

Version C7

New Features:
1. Balance, Bass, Treble and Loudness for Headphone output
2. Prescale for I2S1 and I2S2 inputs
3. Balance in dB units and linear mode
4. SCART volume in dB units and linear mode
5. Increased range for Bass/Treble

Version C8

New Features:
1. Automatic Volume Control A.V.C.
2. Subwoofer Output alternatively with Headphone Output.

15. APPENDIX B: Documentation History

1. Advance Information: “MSP 3400C Multistandard Sound Processor”, Apr. 14, 1994, 6251-377-1AI.
First release of the advance information.

2. MSP 3400C Data Sheet: “MSP 3400C Multistandard Sound Processor”, Dec. 14, 1994, 6251-377-1PD.
First release of the preliminary data sheet.

3. MSP 3400C Data Sheet: “MSP 3400C Multistandard Sound Processor”, Oct. 6, 1996, 6251-377-2PD.
Second release of the preliminary data sheet.
Major changes: see Appendix A: Version C6

4. MSP 3400C Data Sheet: “MSP 3400C Multistandard Sound Processor”, Dec. 8, 1997, 6251-377-3PD.
Third release of the preliminary data sheet.
Major changes: see Appendix A: Version C7 and C8

– new PQFP80 package

MICRONAS INTERMETALL GmbH
Hans-Bunte-Strasse 19
D-79108 Freiburg (Germany)
P.O. Box 840
D-79008 Freiburg (Germany)
Tel. +49-761-517-0
Fax +49-761-517-2174
E-mail: docservice@intermetall.de
Internet: http://www.intermetall.de

Printed in Germany
Order No. 6251-377-3PD