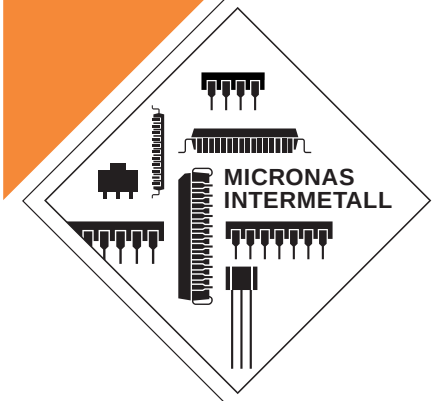

PRELIMINARY DATA SHEET

MSE 3010 Multistandard Encoder

Edition April 7, 1994
6251-351-1PD

MICRONAS
INTERMETALL

Contents

Page	Section	Title
4	**1.**	**Introduction**
4	**2.**	**Functional Description**
5	2.1.	RGB/YUV Inputs
5	2.2.	RGB/YUV D/A Converters
5	2.3.	RGB Matrix
5	2.4.	U and V Lowpass Filter
6	2.5.	PAL/NTSC Burst Insertion
6	2.6.	PAL/NTSC Modulator
6	2.7.	SECAM Preemphasis
7	2.8.	SECAM Modulator
8	2.9.	SECAM Antibell Filter
8	2.10.	SECAM Two’s Complement
8	2.11.	Chroma Bandpass Filter
9	2.12.	Luminance Lowpass Filter
9	2.13.	Chroma Carrier Trap
10	2.14.	Sync Generation and Insertion
10	2.15.	Y, C, and CVBS D/A Converters
10	2.16.	CCU Interface/IM Bus
11	2.17.	Initialization
13	**3.**	**Specifications**
13	3.1.	Outline Dimensions
13	3.2.	Pin Connections
14	3.3.	Pin Descriptions
15	3.4.	Pin Circuits
16	3.5.	Electrical Characteristics
16	3.5.1.	Absolute Maximum Ratings
16	3.5.2.	Recommended Operating Conditions
18	3.5.3.	Characteristics
21	**4.**	**Programming**
21	4.1.	Adjustment of the MSE 3010
21	4.1.1.	Color Mode
21	4.1.2.	Initialization (all modes)
21	4.1.3.	Input Switch (all modes)
21	4.1.4.	Sync Input (all modes)
21	4.1.5.	Blanking Signal (all modes)
21	4.1.6.	Encoder Blanking (all modes)
21	4.1.7.	RGB Pedestal (all modes)
21	4.1.8.	Color Lowpass (all modes)
21	4.1.9.	Color Component Gain (all modes)
21	4.1.10.	Chroma Preemphasis (SECAM only)
22	4.1.11.	Chroma Antibell (SECAM only)
22	4.1.12.	Color Carrier Frequency (all modes)
22	4.1.13.	Limiter for Frequency Modulator
22	4.1.14.	Color Burst Amplitude (NTSC/PAL only)
22	4.1.15.	C Gain (all modes)

Contents

Page	Section	Title
22	4.1.16.	Chroma Bandpass (all modes)
23	4.1.17.	Luminance Lowpass Filter (all modes)
23	4.1.18.	Chroma Trap (all modes)
24	4.1.19.	Luminance Gain SVHS (all modes)
24	4.1.20.	Luminance Gain CVBS (all modes)
24	4.1.21.	Luminance Delay (all modes)
24	4.1.22.	Matching Delay SVHS Luma (all modes)
24	4.1.23.	Horizontal Pulses (all modes)
24	4.1.24.	Vertical Pulses (all modes)

Multistandard Encoder

1. Introduction

The MSE 3010 is a multistandard encoder implemented in CMOS technology for multimedia and computer applications. It supplies an analog composite video signal and an S–VHS signal (chroma and luma separated) which can be fed directly into a 75 Ω video input (e.g. SCART) of a connected device. In addition, it includes 3 D/A converters for the digital input signals which can also drive 75 Ω loads directly. The composite signal can be coded as PAL, NTSC or SECAM or, in a fourth mode, for example as PAL–M. The MSE 3010 requires a digital component input signal that is in 3 x 8 bit RGB or YUV format. The main features of the MSE 3010 are:

– encoding of RGB or component signals (YUV) to composite video and S–VHS signals in PAL/NTSC/SECAM standard

– analog output of composite video and SVHS signals

– analog output of digital RGB or YUV input signals

– analog output signals drives directly 75 Ω load

– automatic hardware programmable initialisation after reset in one of four modes

– very flexible due to adjustments via IM bus.

– color carrier frequency freely programmable

– all filter characteristics freely programmable

2. Functional Description

In the following, the functions of the MSE 3010 will be described. The descriptions refer to the block diagram shown in figure 2–1.

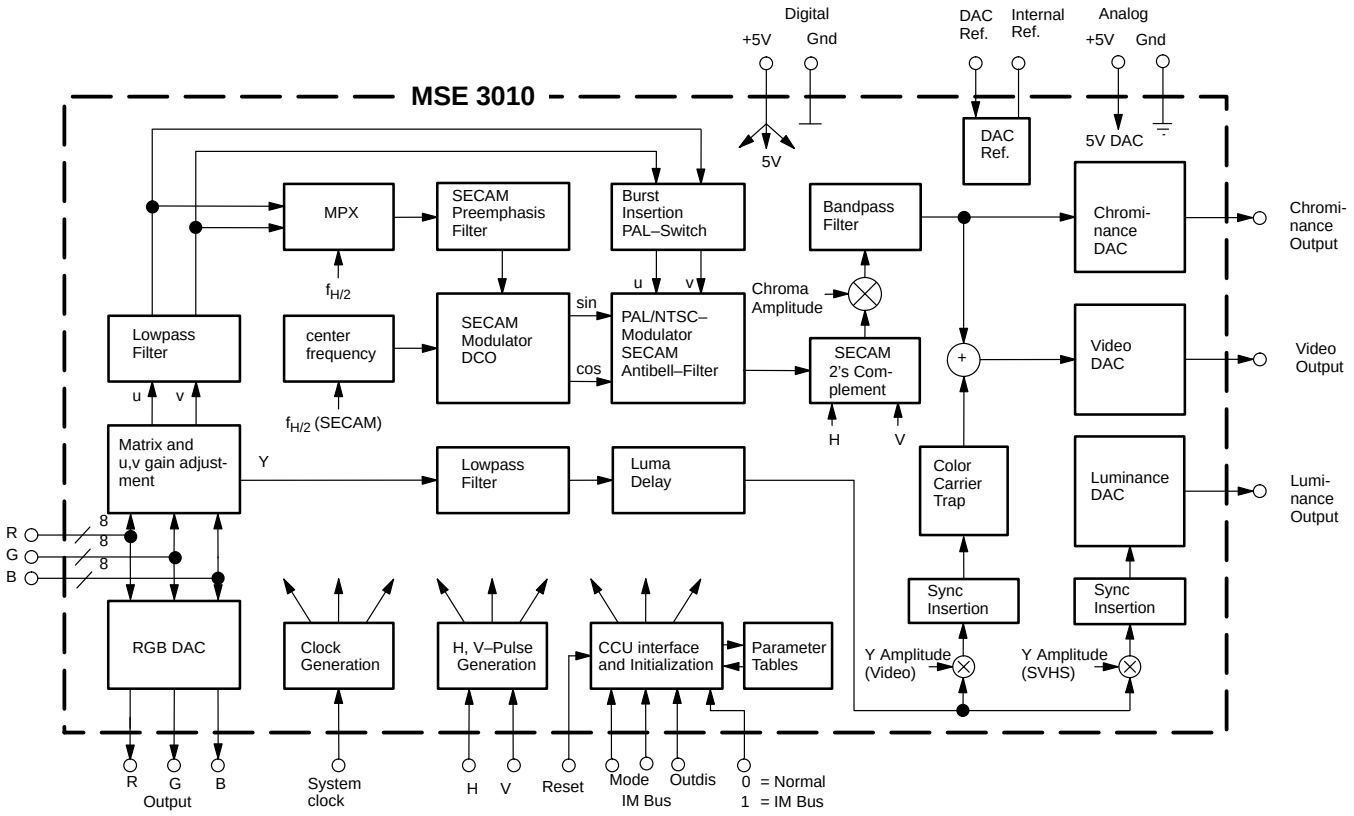

Fig. 2–1: Block diagram MSE 3010

2.1. RGB/YUV Inputs

There are 24 (3x8) digital inputs that can be switched over for either RGB signals or YUV signals. The input clock frequency is equal to the main clock frequency of the MSE 3010. For RGB input signals pure binary coding is used. The value 0 at all three inputs means black level and the value 255 at all three inputs means white. With YUV input signals the Y signal uses pure binary coding and the U and V component signals use two's complement coding (see also Fig. 2–2).

2.2. RGB/YUV D/A Converters

The inputs for the RGB/YUV signals are directly connected to three 8 bit D/A converters. The D/A converters are current source types, where the current flows from the positive supply through the load resistor to ground. If the inputs are switched to RGB mode, a zero at the inputs yields zero output currents. For input values of 255 the output currents are at maximum. If the inputs are switched to YUV the Y signal behaves like the RGB signals. A zero at the two's complement inputs for U and V produces output currents of half the maximum. A value of –128 at these inputs results in zero output currents, a value of 127 results in maximal output currents (see also Fig. 2–2). The output currents are proportional to a reference current. This current which is generated by a stabilized reference voltage is adjustable with an external resistor in the range of 25% to 100%. Therefore the recommended load resistance can vary between 75 Ω and 300 Ω for nominal output voltages. Unused D/A converter outputs must be connected to ground. A lowpass filter is recommended for the D/A outputs, a circuit is shown in the application, see Fig. 2–11. The converters run with the main clock frequency.

2.3. RGB Matrix

The RGB matrix uses a standard matrix for conversion from RGB to Y, R–Y and B–Y. The matrix is shown in the block diagram in Fig. 2–2. The coefficients are fixed and give the following relations for R,G,B signals and the luminance and color difference signals:

```
Y   =  0.30·R  +  0.59·G  +  0.11·B
R–Y =  0.70·R  –  0.59·G  –  0.11·B
B–Y = –0.30·R  –  0.59·G  +  0.89·B
```

The U and V signals are generated after the chroma lowpass filter by the multiplication of the R–Y and B–Y signals with two independent coefficients to adjust for the different composite color standards (PAL, NTSC, SECAM). The RBG matrix can be switched off, if the input signals are YUV rather than RGB. The switching is done by software. The matrix runs with the main clock frequency.

2.4. U and V Lowpass Filter

For modulation with the color subcarrier, the U and V signals have to be bandlimited to approximately 1 MHz. The lowpass filter for the U and V components provides adjustable bandwidth and peaking settings. Frequency responses and step responses of the filters are shown in Fig. 2–3. The description of the complete transfer function can be found in the item 4.1.4 'Programming'. The first part of the filter runs at the main clock frequency. After downsampling by a factor of two, both channels are multiplexed and share the same filter. After demultiplexing (after filter and gain adjustment) the sampling frequency of the U and V signals is half the main clock frequency.

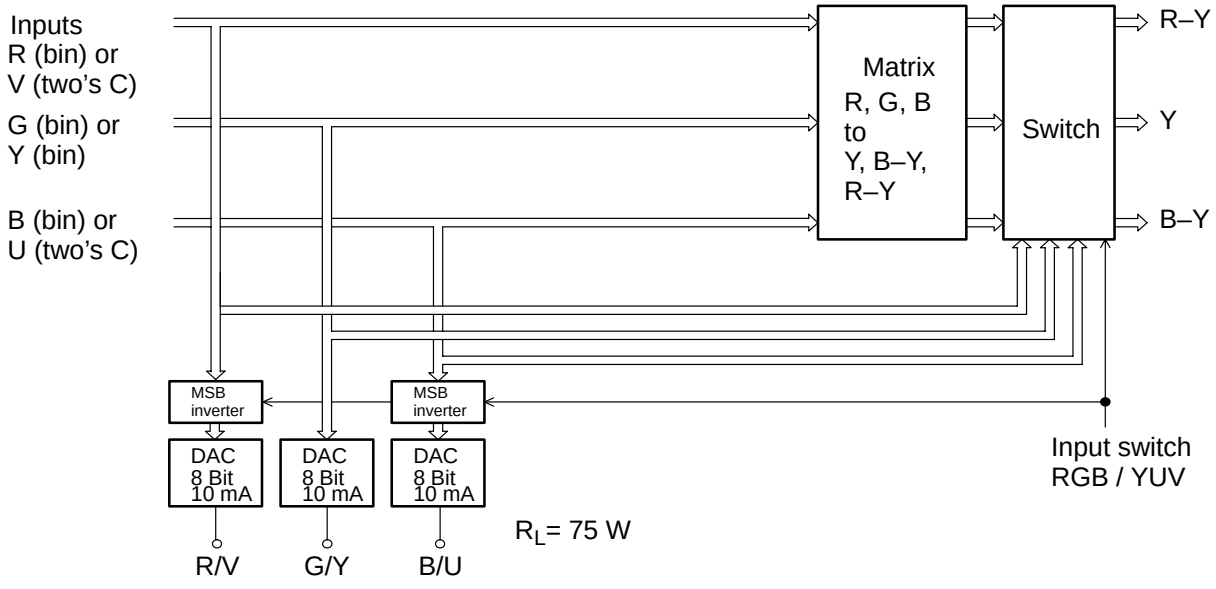

Fig. 2–2: Matrix and YUV/RGB D/A Converters

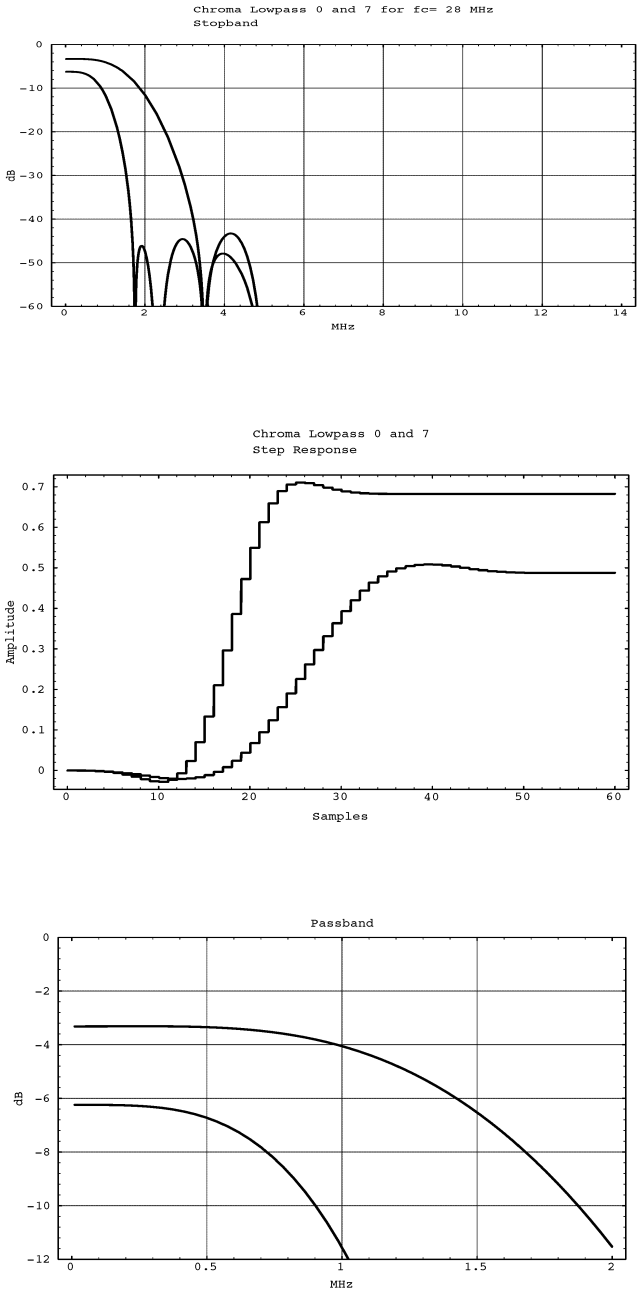

Fig. 2–3: Frequency Response and Step Response of Color component Lowpass Filters

2.5. PAL/NTSC Burst Insertion

During an internally generated color key pulse the color component signals U and V are replaced by a programmable value for the burst amplitude. This value is inserted into the U channel and the inverted value is inserted into the V channel (PAL only). To generate a standard PAL color burst the value for the burst amplitude has to be negative. A positive value can be used for test purposes. The start and stop times of the color burst are adjustable by software.

2.6. PAL/NTSC Modulator

The color carrier frequency is generated by direct digital synthesis: a 24-bit wide accumulator produces a sawtooth signal with the color carrier frequency. The accumulator runs at one half the main clock frequency, thus an accuracy of ±0.4 Hz is achieved. The sawtooth signal drives two ROM tables which contain sine and cosine functions. The modulator for PAL and NTSC has inputs for U, V, sine and cosine of the color carrier. The U signal is multiplied with the cosine and the V signal is multiplied with the sine of the color carrier. The total gain of the modulator is unity and can be adjusted to lower values. The maximum amplitude resolution of the color carrier is eight bit. The modulator runs with half the main clock frequency.

2.7. SECAM Preemphasis

The SECAM preemphasis filter is recursive with two coefficients. The description of the transfer function can be found in the item 4.1.5 'Programming'. The gain of the color component signals has to be adjusted in the chroma lowpass filter (U and V gain). In front of the preemphasis filter a multiplexer switches between the U and V signals at one half the horizontal frequency. Typical amplitude and group delay transfer characteristics are shown in Fig. 2–4. The filter runs with half the main clock frequency.

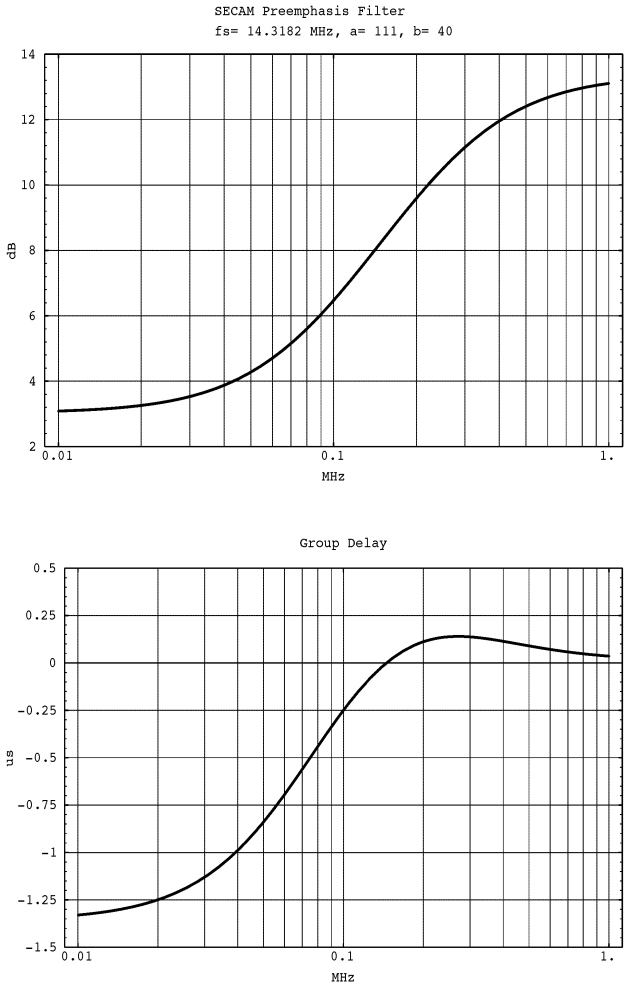

Fig. 2–4: Frequency Response and Group Delay of Secam Preemphasis Filter

2.8. SECAM Modulator

The SECAM modulator uses the same hardware as the color carrier generator used in PAL/NTSC mode. The frequency modulation input of the generator is driven by a value for the center frequency plus the color difference signal in line multiplex. The value for the center frequency changes from line to line. The input values of the generator are limited to two programmable values (upper and lower limit). The center frequencies and the limits can be adjusted by software. In SECAM mode the color carrier signal starts at the begin of each horizontal line with the same phase. The modulator runs with half the main clock frequency.

2.9. SECAM Antibell Filter

The SECAM antibell filter is a transversal filter with two coefficients. The description of the transfer function can be found in the item 4.1.6 ‘Programming’. The correct center frequency can be adjusted with a main clock frequency above 26 MHz. The typical amplitude and group delay transfer characteristics are shown in figure 2–5. The filter runs with half the main clock frequency.

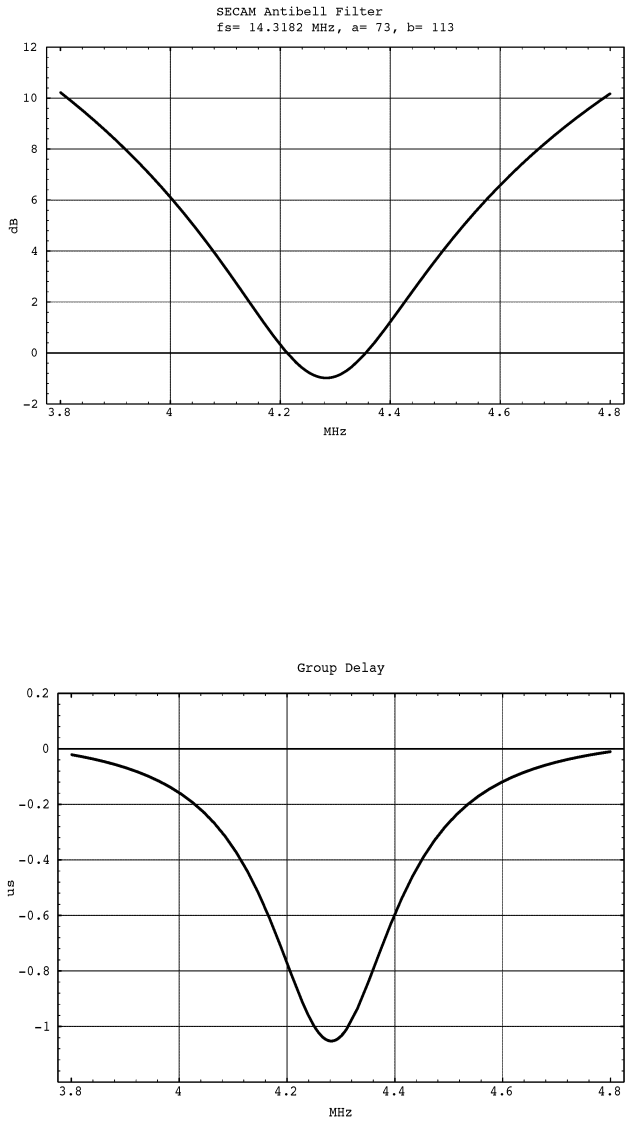

Fig. 2–5: Frequency Response and Group Delay of Secam Antibell Filter

2.10. SECAM Two’s Complement

This stage changes the phase of the color subcarrier in the SECAM mode in the following sequence: 1 line non-inverted, 2 lines inverted. At each second field an additional inversion occurs. The phase of the color subcarrier at the output of the frequency modulator starts at the beginning of each horizontal line with the same value.

2.11. Chroma Bandpass Filter

The chroma bandpass is a transversal filter structure. It consists of five parts. The first part can be switched to one or two frequency variable zeroes or to neutral. The other four parts are zeros that can be switched to zero or a quarter of the main clock frequency or to neutral. This filter should be used mainly for suppression of the sidebands generated by the frequency modulation in SECAM mode. The description of the transfer function can be found in the item 4.1.7 ‘Programming’. Typical transfer characteristics are shown in figure 2–6. The filter runs with half the main clock frequency.

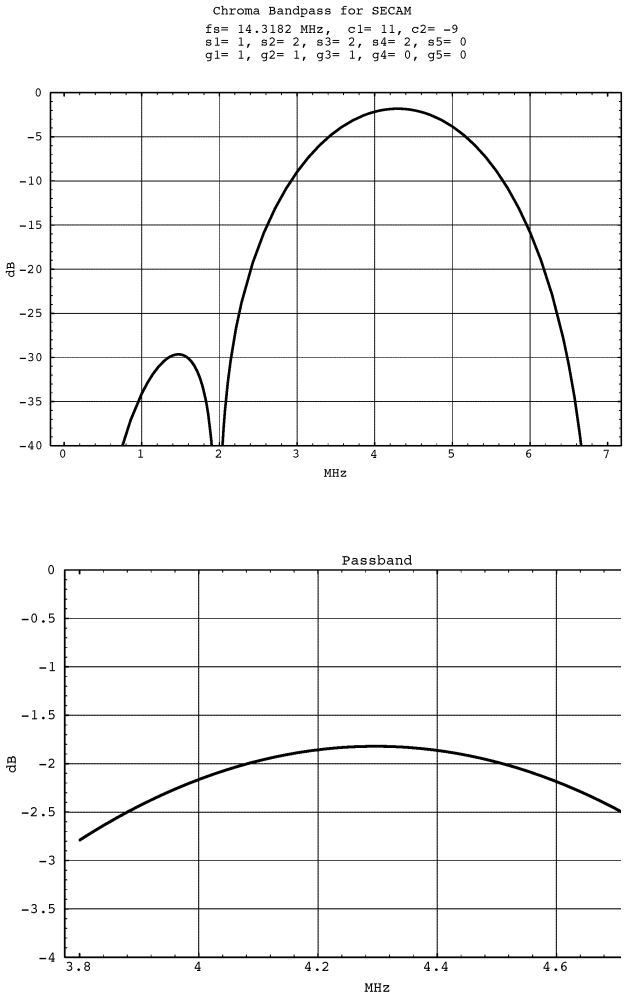

Fig. 2–6: Chroma Bandpass Filter

2.12. Luminance Lowpass Filter

The bandwidth of the luminance path can be reduced by a switchable lowpass filter. The description of the transfer function can be found in the item 4.1.14 ‘Programming’. The frequency response is shown in figure 2–7. The position of this filter in the luminance path is shown in figure 2–9. The filter runs with the main clock frequency.

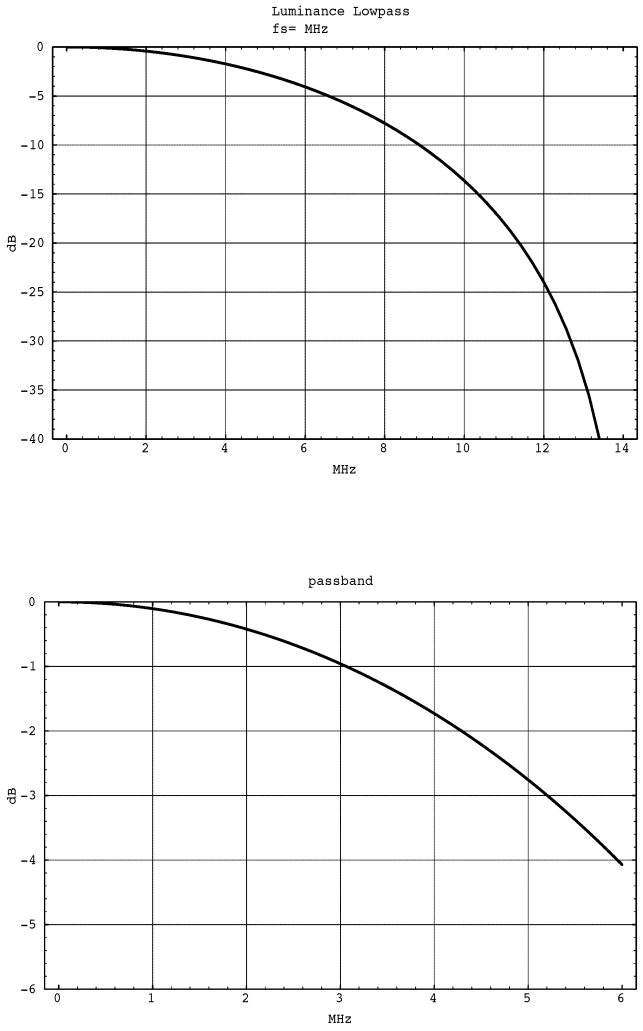

Fig. 2–7: Frequency Response of Luminance Lowpass Filter

2.13. Chroma Carrier Trap

The chroma carrier trap is a band stop filter in the luminance part of the composite video channel. It consists of 4 parts. Two zeroes at $f_{MCLK}/2$ can be switched on or off separately. A single variable zero can be moved between 0 and $f_{MCLK}/2$. The fourth part of the filter is a peaking term to improve the frequency characteristics in the higher luma frequency range. Typical transfer characteristics are shown in Fig. 2–8. Two zeros are shown at $f_{MCLK}/2$, one zero at 4.43 MHz and peaking switched off and on.

The luminance band stop filter influences only the luminance signal in the composite video path, not the luminance signal for SVHS. The description of the complete transfer function can be found in the item 4.1.12 ‘Programming’. The filter runs with the main clock frequency.

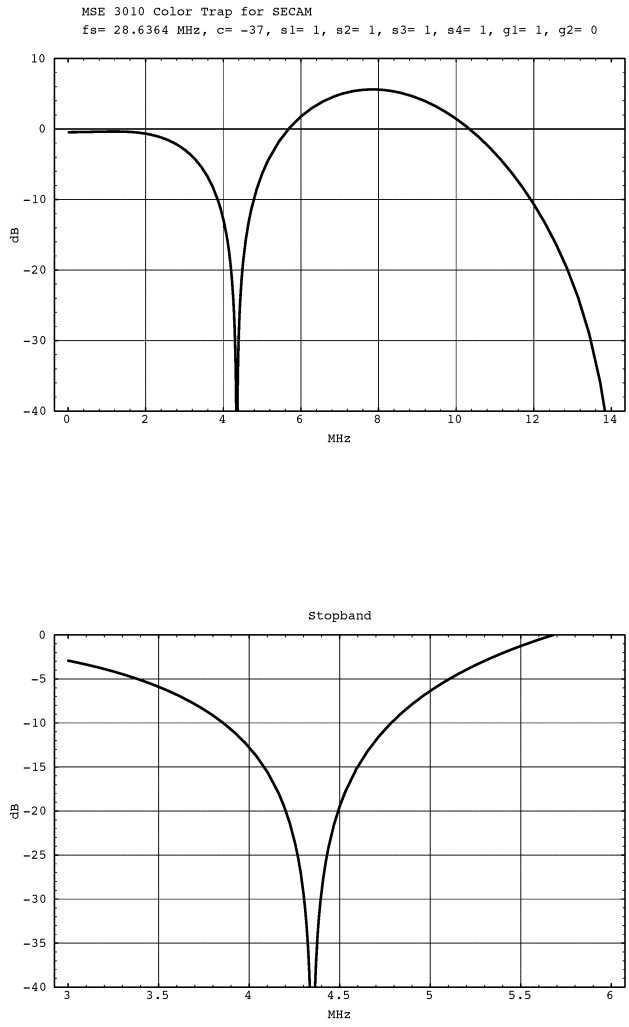

Fig. 2–8: Chroma Carrier Trap
(= Luminance Band Stop Filter)

2.14. Sync Generation and Insertion

The generation of the horizontal sync pulses and all other internally used pulses with horizontal frequency starts with the low transition of the signal at pin 8. This pulse can have two different forms:

a) horizontal sync pulse (low active)
b) composite sync (e.g. from a computer, low active)

In both cases a trigger pulse is generated and starts a programmable down-counter for the generation of the horizontal sync pulse.

In case a) the output pulse of the counter is filtered to get a sync pulse with rise and fall times of approximately 70 ns at 28 MHz main clock frequency. The delayed pulse from the counter triggers a 2H generator. This generator doubles the horizontal frequency. With this signal the vertical sync input (pin 9) is synchronized. The synchronized vertical pulse will be delayed by a programmable delay and triggers a pulse generator which produces a pulse with a duration of three horizontal lines. This is the (nonstandard) vertical sync pulse.

In case b), if a composite sync pulse is fed to pin 8 and the MSE3010 is switched to composite sync, this signal will be lowpass-filtered and added to the luminance signal like the internally generated sync signal in case a). To prevent the internal pulse generator from triggering through by the half line equalisation pulses, the end of the generator has to be programmed by a value of more than half and less than one horizontal period. During this time the trigger input is disabled. The insertion of the sync pulses is made after the luminance gain adjustment, directly in front of the luminance and composite video D/A-converters. Because the ranges of the converters are 9 bit, a value of 124 is added to the luma signal during the active line. During the sync pulse time, a value of zero is added. This produces low sync pulses with the amplitude of approx. 25 % of the D/A converter range.

2.15. Y, C and CVBS D/A Converters

There are three D/A-converters, two of them with 9 bit resolution, one with 8-bit resolution as shown in Fig. 2–9. The 8-bit D/A converter produces the chrominance signal. One 9-bit A/D converter delivers the analog luminance signal, sync included, the other one delivers the composite video signal.
The D/A converters are current source types, where the current flows from the positive supply through the load resistor to ground. The outputs need an external 75... 300 Ω load resistor (depending on the reference current) to produce the correct output voltage. The converters have the following data:

Signal	*Resolution*	*max. Current*	*max. Voltage*
CVBS	9 bit	16.5 mA	1.24 V
Luma	9 Bit	16.5 mA	1.24 V (1 V nominal)
Chroma	8 Bit	16.5 mA	1.24 V (0.8 V_{pp} nominal)

The output currents are proportional to a reference current. This current is driven internally by a stabilized reference voltage and can be adjusted by an external resistor in the range of 25% to 100%. Therefore the recommended load resistance can vary between 75 Ω and 300 Ω for nominal output voltage. Unused D/A converter outputs must be connected to ground. A lowpass filter is recommended at the D/A outputs. A circuit diagram is shown in the application circuit, see Fig. 2–11. The converters run with the main clock frequency.

2.16. CCU Interface/IM Bus

The CCU interface uses only the IM Bus address 169. The data word is 16 bit wide and contains a subaddress (bit 0 to 5) and 8 bit data (bit 8 to 15). The IM bus consists of three lines for the signals Ident, Clock and Data. Ident and Clock are unidirectional, Data is bidirectional. The MSE uses only one direction. This means that data can only be written to the MSE, not read.

In the non-operative state the signals of all three lines are at high level. To start a transaction, the CCU (Central Control Unit) sets the Ident to low level, indicating an address transmission. The Clock signal is set to low level as well, to switch the first bit on the Data line. Then eight address bits are transmitted, beginning with the LSB. Data is latched by the MSE at the positive edge of the Clock signal.

At the end of the address byte the Ident signal goes high, initiating the address comparison in the the connected circuits. In the addressed circuit (i.e. the MSE) the IM bus interface switches over to Data read or write, depending on the address. Also depending on the address, the CCU now transmits sixteen clock pulses, and accordingly two bytes of data are written to or read from the addressed circuit, beginning with the LSB. The completion of the bus transaction is signalled by a short low pulse of the Ident signal. This initiates the storing of the transferred data.

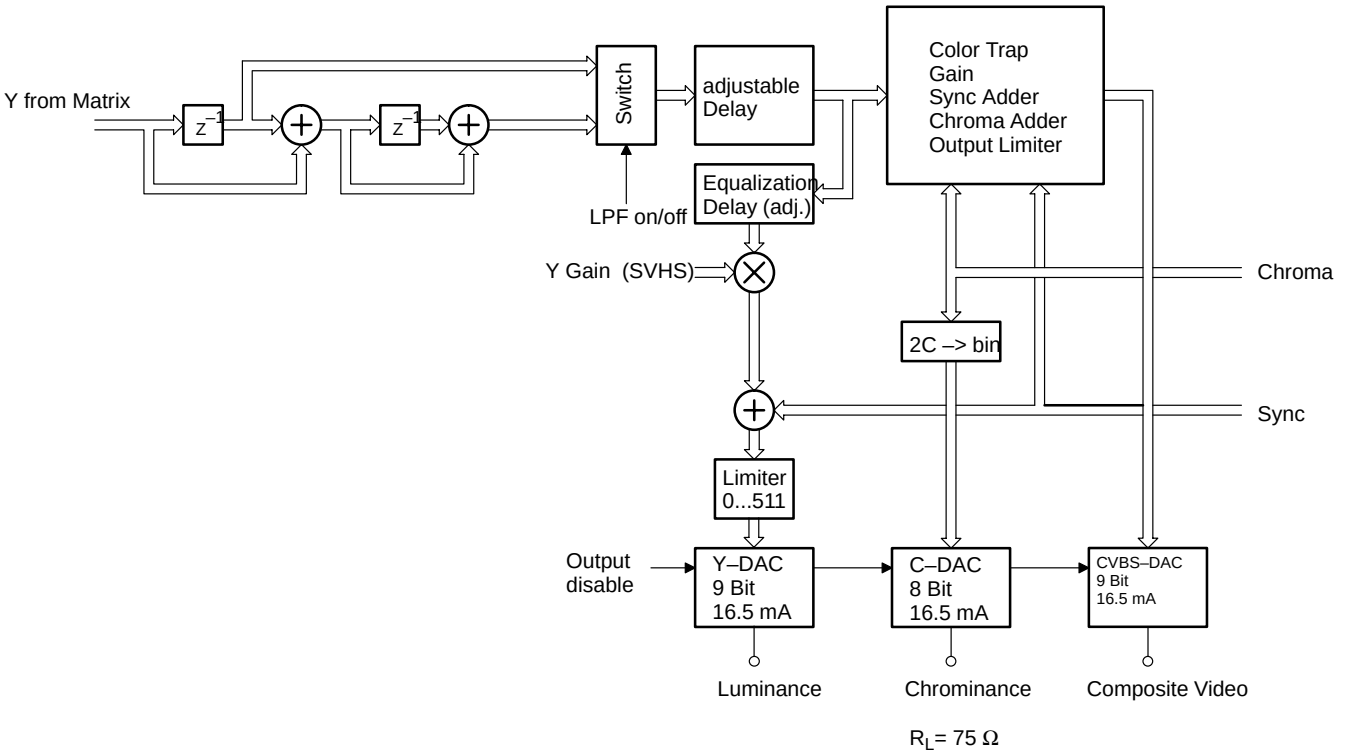

Fig. 2–9: Luminance part and Y, C, CVBS D/A Converters

2.17. Initialization

In the test mode (pin 32 = high) the initialization can be achieved by writing all data from a computer or CCU via the IM bus to the MSE 3010. In this mode all parameters can be changed, e.g. for adjustments of filter characteristics. In this case the customer can adjust each parameter according to his wishes. This is also to set parameters for test purposes. In the normal mode (pin 32 = low) two of the IM bus pins become mode select pins. With these two pins it is possible to select four different parameter sets for automatic initialization of the MSE 3010. The parameter sets are stored in diffusion mask programmable ROMs and can be changed by creating a new diffusion mask in the factory. After a reset pulse all parameters of the selected parameter set will be written to the corresponding registers. Three parameter sets are available for the color modes PAL, NTSC and SECAM. The fourth parameter set can be used for special purposes, for example NTSC with 4.43 MHz color subcarrier frequency.
The initialization is shown in Fig. 2–10, the default initialization data are given in table 4–2 to 4–4.

Application Note:

During the $\overline{\text{Reset}}$ pulse the test mode input pin 32 must be set to low potential! Please wait for approx. 130 clock pulses after the $\overline{\text{Reset}}$ pulse, before the test mode input is set to high and the IM bus is used.

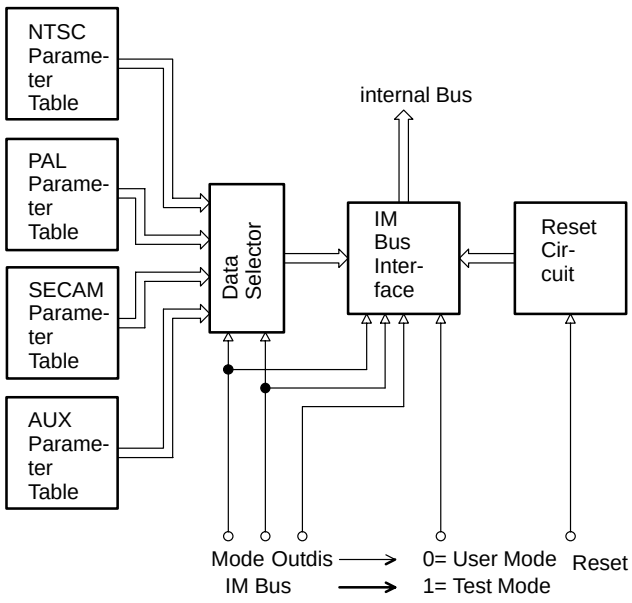

Fig. 2–10: Initialization

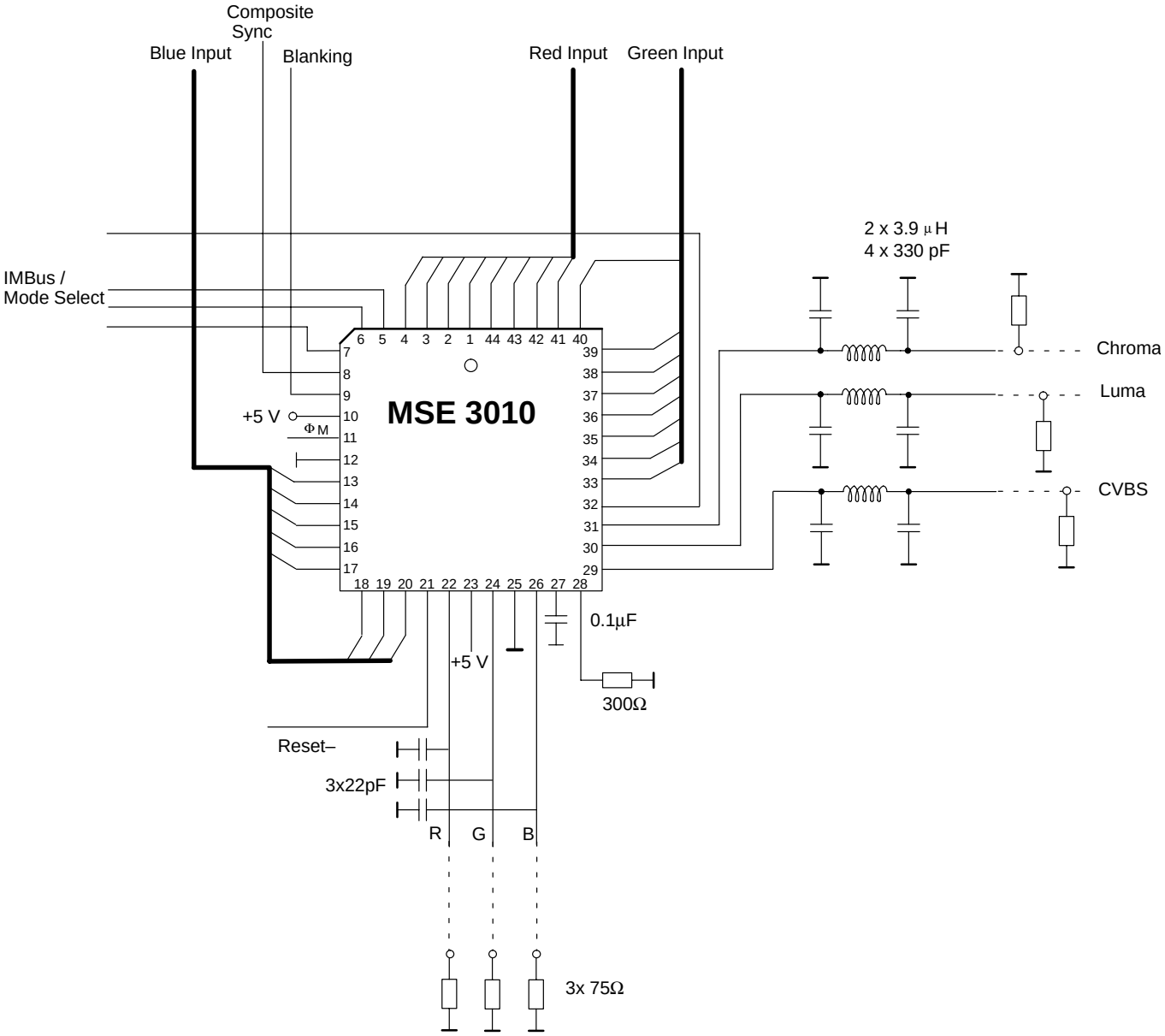

Fig. 2–11: Application circuit

3. Specifications

3.1. Outline Dimensions

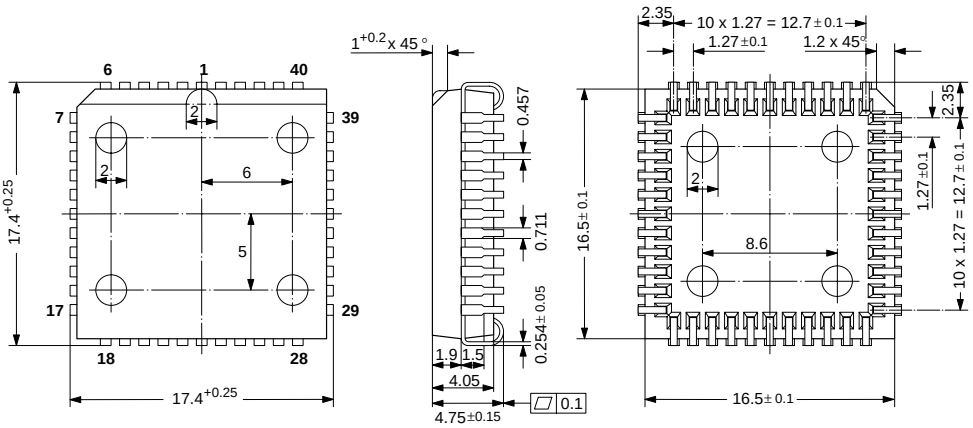

Fig. 3–1: MSE 3010 in 44-pin PLCC Package
Weight approx. 2.5.g Dimensions in mm

3.2. Pin Connections

Pin No.	Signal Name	Symbol
1	Red / V Input 3	RI3
2	Red / V Input 2	RI2
3	Red / V Input 1	RI1
4	Red / V Input 0	RI0
5	Mode Bit 0 / IM Bus Clock	M0
6	Mode Bit 1 / IM Bus Data	M1
7	Output Disable Input / IM Bus Ident	ODI
8	Horiz./ Composite Sync Input	HSYNC
9	Vertical Sync / Blanking Input	VSYNC
10	Digital Supply Voltage	VSUPD
11	Main Clock Input	MCLK
12	Digital Ground	GNDD
13	Blue / U Input 7	BI7
14	Blue / U Input 6	BI6
15	Blue / U Input 5	BI5
16	Blue / U Input 4	BI4
17	Blue / U Input 3	BI3
18	Blue / U Input 2	BI2
19	Blue / U Input 1	BI1
20	Blue / U Input 0	BI0
21	$\overline{\text{Reset}}$ Input	RESQ

Pin No.	Signal Name	Symbol
22	Analog Red / V Output	ARO
23	Analog Supply Voltage	VSUPA
24	Analog Green / Y Output	AGO
25	Analog Ground	GNDA
26	Analog Blue / U Output	ABO
27	Internal Reference DAC	VREFI
28	Reference Current DAC	IREF
29	Analog Luminance Output	ALUO
30	Analog Composite Output	ACVO
31	Analog Chrominance Output	ACO
32	Test Mode Input	TMI
33	Green / Y Input 7	GI7
34	Green / Y Input 6	GI6
35	Green / Y Input 5	GI5
36	Green / Y Input 4	GI4
37	Green / Y Input 3	GI3
38	Green / Y Input 2	GI2
39	Green / Y Input 1	GI1
40	Green / Y Input 0	GI0
41	Red / V Input 7	RI7
42	Red / V Input 6	RI6
43	Red / V Input 5	RI5
44	Red / V Input 4	RI4

3.3. Pin Descriptions

Pins 1 to 4 and 41 to 44 – Digital Red or V Inputs 0...7 (Fig. 3–2)
These are the inputs for the digital red signal in the RGB mode. In YUV mode the digital V component signal has to be connected. In case of the red signal the code has to be pure binary. Bit 0 is the LSB and bit 7 is the MSB. In case of the V signal the code has to be two's complement. Bit 0 is the LSB and bit 7 is the sign bit.

Pins 5 and 6 – Mode Bits 0 and 1 or IM Bus Clock and Data (Fig. 3–2)
In the normal mode (pin 32 at low level) these pins select one of the four parameter tables for initialization. The parameters of a selected table will be written to the corresponding registers after a reset pulse. In the test mode (pin 32 at high level) pin 5 is the clock input and pin 6 is the data input for the IM Bus interface.

Pin 7 – Output Disable Input or IM Bus Ident (Fig. 3–2)
In the normal mode (pin 32 at low level) via this pin the analog outputs for luminance, chrominance and composite video signals can be disabled. The output currents of the D/A converters are switched to zero. The outputs of the RGB/YUV D/A converters are not affected. A high level at this pin means output disabled. In the test mode (pin 32 at high level) this pin is the ID input of the IM Bus interface.

Pin 8 – Horizontal or Composite Sync Input (Fig. 3–2)
Via this pin the horizontal sync or the composite sync pulses have to be supplied. The selection between them can be done by software.
a) On a rectangular sync pulse, the high-low transition is used for starting the internal Hsync generation. All internal pulses with horizontal frequency refer to this transition.
b) At a composite sync signal the generation of internal Hsync pulses starts with the high-low transition of the incoming Hsync pulses. The end of timing generator has to be set to more than 32 µs and less than 64 µs because the Hsync input has to be disabled during h/2-pulses (equalizing pulses). The composite sync signal will be lowpass-filtered and added to the luminance and composite video signal.

Pin 9 – Vertical Sync or Blanking Input (Fig. 3–2)
This input gets the signal for the vertical synchronization or blanking. The input mode of this pin can be selected by software.
a) Vsync: In the non composite sync mode from the high-low transition a vsync pulse of 3 lines duration is generated after an adjustable delay. The length of the input pulse does not matter.
b) Blanking: The blanking pulse blanks the input signals of the RGB D/A converters to zero, meaning ultra black. The normal black level at digital zero input has a higher value. The blanking pulse is also fed to the Y, C and CVBS signals.

Pin 10 – Digital Supply Voltage
This pin supplies all digital stages and has to be connected with the positive supply voltage.

Pin 11 – Main Clock Input (Fig. 3–3)
This is the input for the main clock signal. The frequency can be 26 MHz and above. Over 26 MHz the SECAM filters can be set to the correct center frequencies. PAL/NTSC works with a lower frequency too. For the maximum clock frequency refer to the Recommended Operating Conditions.

Pin 12 – Digital Ground
This is the common ground connection of all digital stages and has to be connected with the ground of the power supply.

Pins 13 to 20 – Digital Blue or U Inputs (Fig. 3–2)
These are the Inputs for the digital blue signal in the RGB mode. In YUV mode the digital color component signal U has to be connected. In case of the blue signal the code has to be pure binary. Bit 0 is the LSB and bit 7 is the MSB. In case of the U signal the code has to be two's complement. Bit 0 is the LSB and bit 7 is the sign bit.

Pin 21 – $\overline{\text{Reset}}$ Input (Fig. 3–4)
A low signal at this pin generates a reset. The low-high transition of this signal should come when the supply voltage is stable (power-on reset). After the reset pulse the initialization of the circuit starts. All software adjustable parameters will be written into the registers.

Pin 22 – Analog Red or V Output (Fig. 3–5)
This output provides the analog red or V signal depending on the digital input signal at pins 1 to 4 and 41 to 44. The amplitude is 0.75 V_{pp} at 75 Ω to 300 Ω (depends on the reference resistor). A 75 Ω to 300 Ω load resistor has to be connected between output and analog ground because the D/A converter is a current source. The load resistor is typically the input resistor of the connected TV set or monitor and has to be DC coupled. Between the output and the load resistor an analog lowpass filter is necessary to suppress the alias signal.

Pin 23 – Analog Supply Voltage
This is the supply voltage for the D/A converters and has to be connected with the positive supply voltage. Note: The layout of the PCB should take into consideration the need for a relatively noise-free supply.

Pin 24 – Analog Green or Y Output (Fig. 3–5)
This output provides the analog green or Y signal depending on the digital input signal at pins 33...40. The amplitude is 0.75 V_{pp} at 75 Ω to 300 Ω (depends on the reference resistor). In the case of U signal the output delivers half the maximum current at two's complement zero input. A 75 Ω to 300 Ω load resistor has to be connected between output and analog ground because the D/A converter is a current source. The load resistor is typically the input resistor of the connected TV set or monitor and has to be DC coupled. Between the output and the load resistor an analog lowpass filter is necessary to suppress the alias signal.

Pin 25 – Analog Ground
This is the ground pin for the D/A converters and has to be connected with the ground of the power supply. Note: The layout of the PCB should take into consideration the need for a relatively noise-free ground.

Pin 26 – Analog Blue or U Output (Fig. 3–5)
This output provides the analog blue or U signal depending on the digital input signal at pins 13...20. The amplitude is 0.75 V_{pp} at 75 Ω to 300 Ω (depends on the reference resistor). In the case of U signal the output delivers half the maximum current at two's complement zero input. A 75 Ω to 300 Ω load resistor has to be connected between output and analog ground because the D/A converter is a current source. The load resistor is typically the input resistor of the connected TV set or monitor and has to be DC-coupled. Between the output and the load resistor an analog lowpass filter is necessary to suppress the alias signal.

Pin 27 – Internal Ref. of the D/A Converters (Fig. 3–6)
This pin has to be connected to ground over a capacitor with a capacity of approx. 100 nF. The capacitor should be a type with low inductance and high insulating resistance.

Pin 28 – Ref. Current of the D/A Converters (Fig. 3–6)
This pin has to be connected to analog ground over a reference resistor. The output currents can be adjusted by varying the resistance in the range between 390 Ω and 1560 Ω.

Pin 29 – Analog Luminance Output (Fig. 3–5)
This output provides the analog luminance signal for an SVHS input of a video recorder or TV set. The amplitude is 1.0 V_{pp} at 75 Ω to 300 Ω (depends on the reference resistor). A 75 Ω to 300 Ω load resistor has to be connected between output and analog ground because the D/A converter is a current source. The load resistor is typically the input resistor of the connected TV set or monitor and has to be DC coupled. Between the output and the load resistor an analog lowpass filter is necessary to suppress the alias signal.

Pin 30 – Analog Composite Video Output (Fig. 3–5)
This output provides the analog composite video signal. The amplitude is 1.24 V_{pp} at 75 Ω to 300 Ω (depends on the reference resistor). A 75 Ω to 300 Ω load resistor has to be connected between output and analog ground because the D/A converter is a current source. The load resistor is typically the input resistor of the connected TV set or monitor and has to be DC coupled. Between the output and the load resistor an analog lowpass filter is necessary to suppress the alias signal.

Pin 31 – Analog Chrominance Output (Fig. 3–5)
This output provides the analog Chrominance signal for an SVHS input of a video recorder or TV set. The amplitude is typically 0.8 V_{pp} at 75 Ω to 300 Ω (depends on the reference resistor) and can be digitally adjusted up to 1.24 V_{pp}. A 75 Ω load resistor has to be connected between output and analog ground because the D/A converter is a current source. The load resistor is typically the input resistor of the connected TV set or monitor and has to be DC coupled. Between the output and the load resistor an analog lowpass filter is necessary to suppress the alias signal.

Pin 32 – Test Mode Input (Fig. 3–2)
With this pin the test mode can be switched on. With low level at this pin the normal mode is selected and the pins 5 and 6 work as initialization mode pins. Pin 7 works as an output disable input.
With high level at this pin, pins 5 to 7 work as IM bus connections.

Pins 33 to 40 – Digital Green or Y Inputs (Fig. 3–2)
These are the inputs for the digital green signal in the RGB mode. In YUV mode the digital Y component signal has to be connected. In both cases the code has to be pure binary. Bit 0 is the LSB and bit 7 is the MSB.

3.4. Pin Circuits

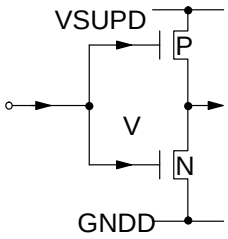

Fig. 3–2: Input Pins 1 to 9, 13 to 20, 32 to 44

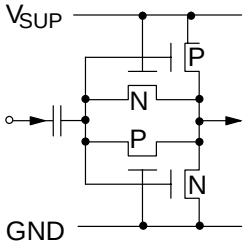

Fig. 3–3: Input Pin 11

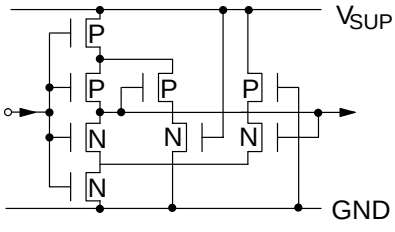

Fig. 3–4: Input Pin 21

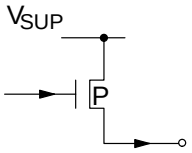

Fig. 3–5: Output Pins 22, 24, 26, 29, 30, 31

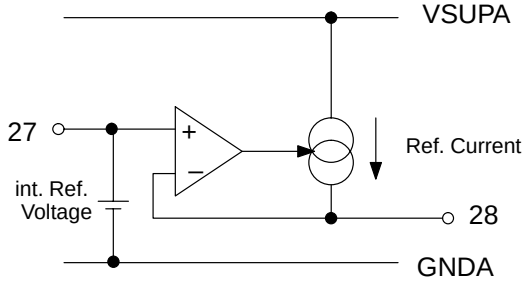

Fig. 3–6: Input Pin 27 and Output Pin 28

3.5. Electrical Characteristics

3.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temp.	–	0	70	°C
T_S	Storage Temperature	–	–40	125	°C
V_{SUP}	Supply Voltage	10, 23	–	6	V
V_I	Input Voltage, all Pins	1 to 44	–0.3	V_{SUP} + 0.3	V
I_I	Input Current all Pins		–20	+20	mA

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

3.5.2. Recommended Operating Conditions at T_A = 0 to 65 °C, f_{MCLK} = 26 to 30 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUPD}	Digital Supply Voltage	10	4.75	5.0	5.25	V
V_{SUPA}	Analog Supply Voltage	23	4.75	5.0	5.25	V
V_{MCLKDC}	Main Clock Input D.C. Voltage	11	1.5	–	3.5	V
V_{MCLKAC}	Main Clock Input A.C. Voltage		0.8	–	2.5	V_{pp}
f_{MCLK}	Main Clock Frequency		26	–	30	MHz
$\frac{t_{MCLKH}}{t_{MCLKL}}$	Main Clock Input High/Low Ratio		0.9	1.0	1.1	–
t_{MCLKHL}	Main Clock Input High to Low Transition Time		–	–	$\frac{0.15}{f_{MCLK}}$	s
V_{RGBH}	RGB/YUV Input High Voltage	1 to 4 13 to 20 33 to 44	2.4	–	–	V
V_{RGBL}	RGB/YUV Input Low Voltage	1 to 4 13 to 20 33 to 44	–	–	0.8	V

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
t_{RGBIH}	RGB/YUV Input Hold Time after Falling Edge of Main Clock	1 to 4 13 to 20 33 to 44	8	–	–	ns
t_{RGBIS}	RGB/YUV Input Setup Time before Falling Edge of Main Clock		2	–	–	ns
V_{SIL}	Sync Input Low Voltage	8, 9	–	–	0.8	V
V_{SIH}	Sync Input High Voltage		2.4	–	–	V
t_{SYNCIH}	Sync Input Hold Time after Falling Edge of Main Clock		5	–	–	ns
t_{SYNCIS}	Sync Input Setup Time before Falling Edge of Main Clock		5	–	–	ns
V_{RESQH}	$\overline{\text{Reset}}$ Input Low Voltage	21	–	–	0.8	V
V_{RESQL}	$\overline{\text{Reset}}$ Input High Voltage		2.8	–	–	V
t_{REIL}	$\overline{\text{Reset}}$ Input Low Time		1	–	–	µs
V_{CTLL}	Control Inputs (M0, M1, ODI, TMI) Low Voltage	5 to 7 32	–	–	0.8	V
V_{CTLH}	Control Inputs (M0, M1, ODI, TMI) High Voltage	5 to 7 32	2.4	–	–	V
R_{REF}	Resistor for Reference Current Adjustment	28	390	–	1560	Ω
C_{REFI}	Capacitor for Internal Reference Voltage	27	–	100	–	nF
R_{LOAD}	Analog Output Load Resistance (R_{REF}= 390 Ω)	22, 24, 26, 29 to 31	–	–	75	Ω
	Analog Output Load Resistance (R_{REF}= 1560 Ω)	22, 24, 26, 29 to 31	–	–	300	Ω
V_{IMIL}	IM Bus Input Low Voltage	5 to 7	–	–	0.8	V
V_{IMIH}	IM Bus Input High Voltage		2.4	–	–	
$f_{\Phi IM}$	ΦIM IM Bus Clock Frequency		0.05	–	1000	kHz
t_{IM1}	IM Clock Input Delay Time after IM Bus Ident Input	5	0	–	–	–
t_{IM2}	IM Clock Input Low Pulse Time		500	–	–	ns
t_{IM3}	IM Clock Input High Pulse Time		500	–	–	ns

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
t_{IM4}	IM Clock Input Setup Time before Ident Input High	5	0	–	–	–
t_{IM5}	IM Clock Input Hold Time after Ident Input High		500	–	–	ns
t_{IM6}	IM Clock Input Setup Time before Ident End-Pulse Input		1	–	–	µs
t_{IM7}	IM Bus Data Input Delay Time after IM Clock Input	6	0	–	–	–
t_{IM8}	IM Bus Data Input Setup Time before IM Clock Input		0	–	–	–
t_{IM9}	IM Bus Data Input Hold Time after IM Clock Input		0	–	–	–
t_{IM10}	IM Bus Ident End-Pulse Low Time	7	1	–	–	µs

3.5.3. Characteristics at T_A = 0 to 65 °C, V_{SUP} = 4.75 to 5.25 V, f_{MCLK} = 28 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
I_{SUPD}	Current Consumption Digital	10	30	–	60	mA	no input signal
I_{SUPA}	Current Consumption Analog	23	80	–	140	mA	R_{REF}= 390 Ω R_{LOAD}= 50 Ω
C_{MCLK}	Main Clock Input Capacitance	11	–	7	–	pF	
V_{RGBT}	RGB/YUV Input Threshold Voltage	1 to 4 13 to 20 33 to 44	–	1.5	–	V	
C_{RGBI}	RGB/YUV Input Capacitance	1 to 4 13 to 2 33 to 44	–	7	–	pF	
V_{SYNCT}	Sync Input Threshold Voltage	8, 9	–	1.5	–	V	
C_{SYNCI}	Sync Input Capacitance	8, 9	–	7	–	pF	

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{CTLT}	Control Inputs (M0, M1, ODI, TMI) Threshold Voltage	5, to 7 32	–	1.5	–	V	
V_{REFI}	Internal Reference Voltage D/A-Converter	27	1.89	1.95	2.01	V	to be measured with $R_I \geq 30$ MΩ
V_{REF}	Reference Voltage D/A-Converter	28	1.89	1.95	2.01	V	R_{REF} = 390 Ω
$-I_{RGBO}$	Analog Output Current RGB D/A-Converter at maximum signal	22, 24, 26	10.3	10.8	11.3	mA	R_{REF} = 390 Ω R_L = 0
	Analog Output Current RGB D/A-Converter at maximum signal	22, 24, 26	2.59	2.7	2.81	mA	R_{REF} = 1560 Ω R_L = 0
$-I_{RGBO}$	Analog Output Current RGB D/A-Converter at zero signal	22, 24, 26	0.76	0.8	0.84	mA	R_{REF} = 390 Ω R_L = 0
	Analog Output Current RGB D/A–Converter at zero signal	22, 24, 26	0.19	0.2	0.21	mA	R_{REF} = 1560 Ω R_L = 0
V_{RGBO}	Analog Output Voltage RGB at maximum signal	22, 24, 26	0.77	0.81	0.85	V	R_{REF} = 390 Ω R_L = 75 Ω
V_{RGBO}	Analog Output Voltage RGB at zero signal	22, 24, 26	0.057	0.06	0.063	V	R_{REF} = 390 Ω R_L = 75 Ω
$-I_{YCO}$	Analog Output Current Y, C, CVBS D/A–Converter at maximum signal	29 to 31	15.9	16.6	17.3	mA	R_{REF} = 390 Ω R_L = 0
	Analog Output Current Y, C, CVBS D/A–Converter at maximum signal	29 to 31	3.97	4.15	4.32	mA	R_{REF} = 1560 Ω R_L = 0
V_{YCO}	Analog Output Voltage Y, C, CVBS at maximum signal	29 to 31	1.2	1.25	1.3	V	R_{REF} = 390 Ω R_L = 75 Ω
V_{AMAX}	Maximal Output Voltage Range D/A Converter	22, 24, 26, 29 to 31	–	–	1.4	V	
DN_{DAC}	Differential Nonlinearity D/A-Converter	22, 24, 26, 29 to 31	–	0.2	0.5	LSB	R_{REF} = 390 Ω R_L = 75 Ω
IN_{DAC}	Integral Nonlinearity D/A Converter	22, 24, 26, 29 to 31	–	0.25	0.5	LSB	

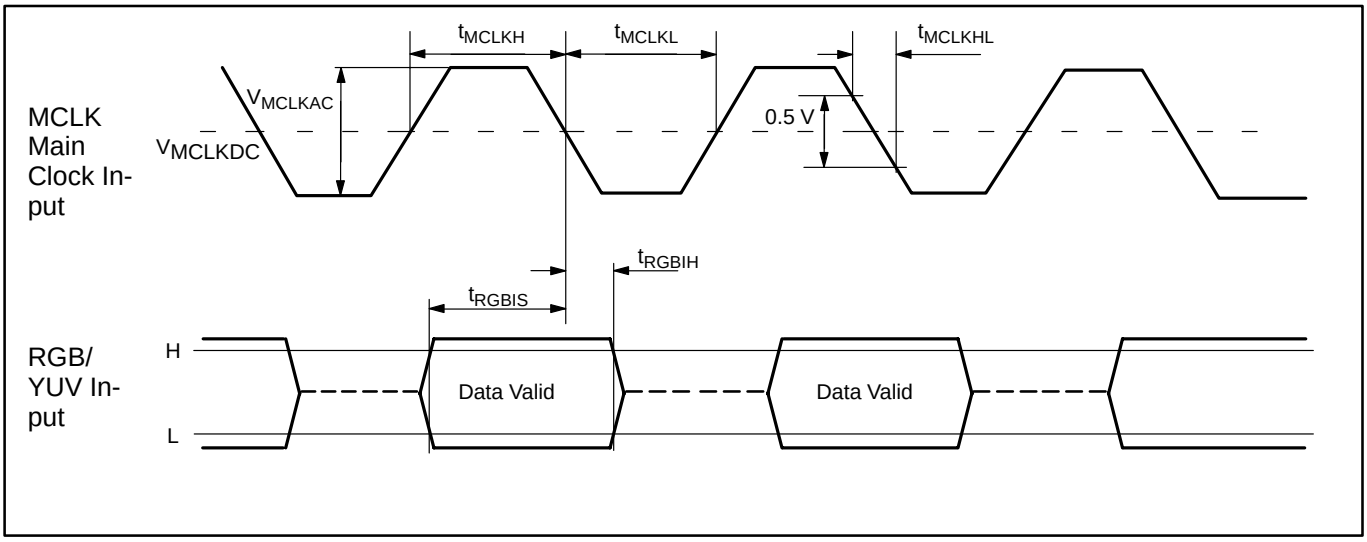

Fig. 3–7: Digital Clock, Input Signal Waveforms

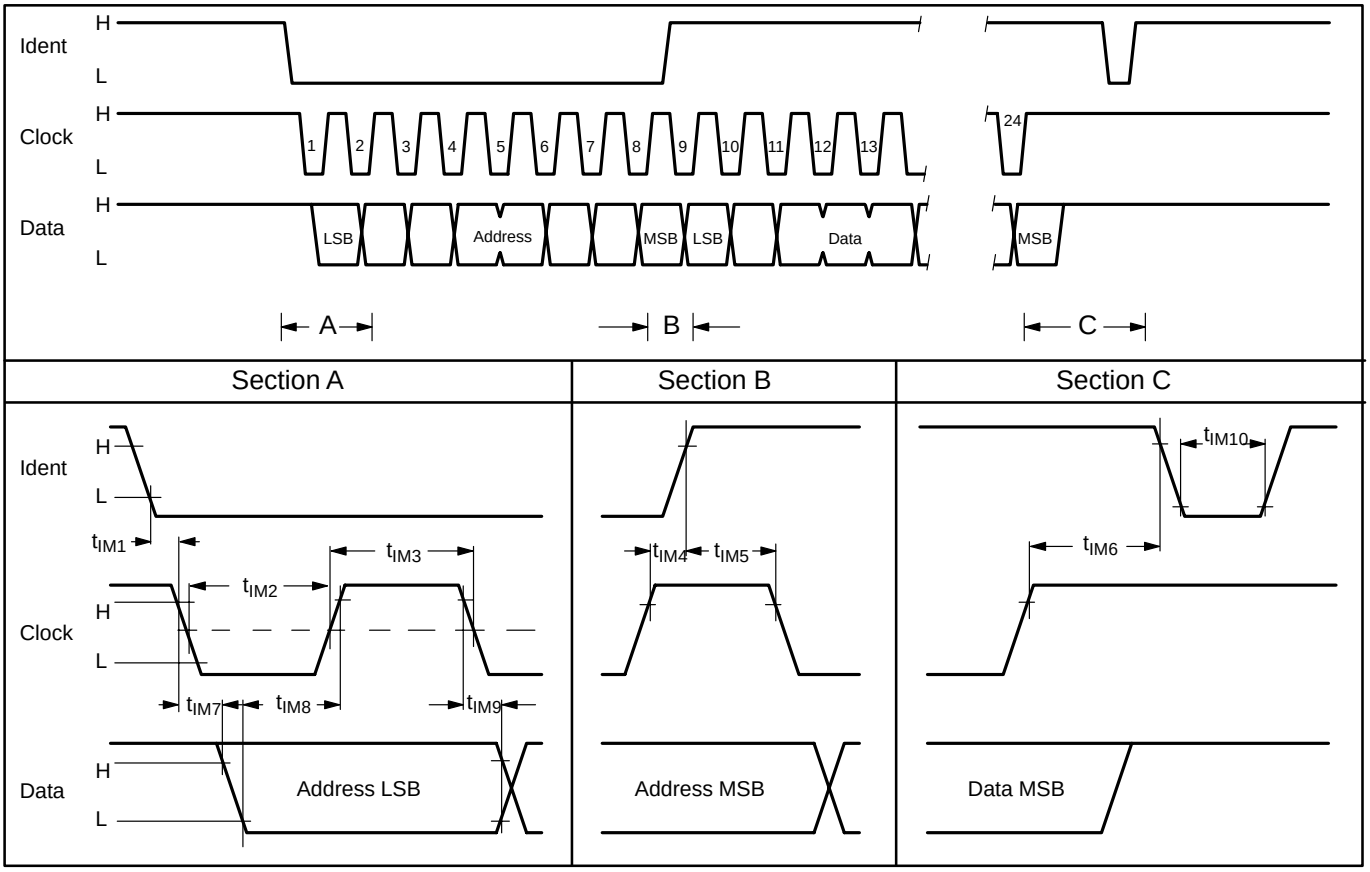

Fig. 3–8: IM Bus Waveforms

4. Programming

4.1. Adjustment of the MSE 3010

For an easy adjustment of the MSE 3010, the CLIMB software can be used. The parameter names mentioned below refer to the CLIMB software. The register subaddress is always given in parenthesis.

4.1.1. Color Mode

Command name: Function Keys [F2] [F3] [F4]
With this command in the CLIMB program, all parameters will be loaded from the lookup table for the desired color mode. There are three lookup tables for three color modes (F2= PAL, F4= SECAM, F3= NTSC).

4.1.2. Initialization (all modes)

Command name: INIT or [F1]
This is a command in the CLIMB program. It initializes the MSE 3000 with the parameters set to the most recent values. Before using this command, a hardware reset (power-on reset) should be done.

4.1.3. Input Switch (all modes) (40)

Command name: YUVIN
This command switches between RGB and YUV input. YUVIN=1 means the YUV input is selected. In this case the RGB D/A converters deliver the analog YUV signals.

4.1.4. Sync Input (all modes) (40)

Command name: CSYNCIN
At “0” the separated horizontal and vertical sync signals are selected. At “1” the composite sync signal has to be fed into the hsync/csync input. In this case the vsync input can be used for a blanking signal.

4.1.5. Blanking Signal (all modes) (40)

Command name: BLANKIN
At “0” the vsync input is used for vertical sync signal. At “1” the vsync input is used for a combined blanking signal.

4.1.6. Encoder Blanking (all modes) (37)

Command name: ENCBLD
At “0” the blanking signal at the vsync input is enabled for the encoder. The start and end values of the internal blanking signals must be adjusted so, that the the external blanking signal is not overlapped. A “1” disables the blanking for the decoder. In this case the internal adjustable blanking signals can be used.

4.1.7. RGB Pedestal (all modes) (37)

Command name: RGBPEDD
During the external blanking signal the analog RGB outputs are blanked. The output signals are zero. During the active video time a pedestal value is added to the output signals. With RGBPEDD=1 this pedestal can be disabled.

4.1.8. Color Lowpass (all modes) (14,15)

Command names: CLPS, CLPP
The color lowpass filter works for the R-Y and B-Y component signals out of the matrix.
CLPS is the filter selection from 0 to 7 where 0 is the largest and 7 is the smallest bandwidth. A small bandwidth reduces the cross luminance distortions (crawling at horizontal color transitions).

CLPP is the peaking adjustment in the color lowpass filter. The peaking increases the gain of the higher frequencies. If the peaking is too high, overshoot at horizontal color transitions occurs. The value for CLPP has to be negative, a typical value is –50. The peaking decreases the DC gain of the filter. Therefore the values for UGAIN and VGAIN have to be increased.

4.1.9. Color Component Gain (all modes) (17, 18)

Command names: UGAIN, VGAIN
This is the gain adjustment for the color component signals. The B-Y signal is multiplied with the UGAIN value to result in the U component signal. The R-Y signal is multiplied with the VGAIN value to result in the V component signal.

UGAIN	Value = 128 · gain	range 0...127
VGAIN	Value = 128 · gain	range 0...127

4.1.10. Chroma Preemphasis (SECAM only) (11,12)

Command names: PREEMA, PREEMB
The preemphasis filter is used in SECAM mode only. It consists of a transversal path and a recursive path. The input signals are –U and +V line sequential from the output of the chroma lowpass filter 1. The Preemphasis Fil-

ter runs with half the clock frequency. Therefore for the calculation the sample frequency is fc/2. The transfer function is:

H(z) =	$4 \cdot (1 - a \cdot z^{-4}) / (1 - b \cdot z^{-4})$	
where	A = 128 · a	range 0 ...127
	B = 64 · b	range 0 ... 63

4.1.11. Chroma Antibell (SECAM only) (9,10)

Command names: BELLA, BELLB
The Antibell filter is used in the SECAM mode only. It is a transversal filter with the two coefficients A and B. The input signal is delivered from the SECAM frequency modulator and has an amplitude of ±127 steps. The Antibell Filter runs with half the clock frequency. Therefore for the calculation the sample frequency is fc/2. The transfer function is:

H(z) =	$8 \cdot (1 + a \cdot z^{-1} + b \cdot z^{-2})$	
where	A = 128 · a	range –128 ... +127
	B = 128 · b	range –128 ... +127

The correct center frequency can be adjusted with the clock frequency > 25.3 MHz, for example:

$h(z) = 1 - 2 \cdot r \cdot \cos\varphi \cdot z^{-1} + r^2 \cdot z^{-2}$
fs = 14.188 MHz, f_0 = 4.28 MHz → $\varphi = 108.6°$
r = 0.94 (chosen)
$a = -2 \cdot 0.94 \cdot \cos(108.6°) = 0.6$ → A = 77
$b = 0.94^2 = 0.884$ → B = 113

4.1.12. Color Carrier Frequency (all modes) (0...5)

Command names: UCCFHB, UCCFMB, UCCFLB, VCCFHB, VCCFMB, VCCFLB

The adjustment of the color carrier frequency (or center frequency in SECAM mode) is controlled by 6 registers, of 8 bits each. The first three registers are for the U center frequency (low, middle and high byte). The last three registers are for the V center frequency. In PAL or NTSC mode, only the V registers are used. In SECAM mode the U values are for the blue center frequency, the V values are for the red center frequency. The formula for the calculation of the value is:

$$\text{Value} = 2^{25} \cdot f_{subcarrier} / f_{clock}$$

Example:
fc= 28.63636 MHz, fc= 3.579545 MHz
Value= 4194304.0
The (rounded) value is hexadecimal 400000
HB= $40, MB= $00, LB= $00

Application Note:

The color carrier frequency is normally not synchronized with the horizontal frequency. To avoid an attached receiver (e.g. DPU in the DIGIT 2000 system) detecting a coupled signal and switching over from line synchronization to counter mode, the adjusted color carrier frequency should deviate from the standard frequency by approx. 5 Hz.

4.1.13. Limiter for Frequency Modulator (6,7)

Command names: UPLIM, LOLIM
In PAL and NTSC mode, The lower limit should be set to zero, the upper limit should be set to maximum. The correct adjustment is necessary in SECAM mode. The formula for the calculation of the value is:

$$\text{Value} = 2^{10} \cdot f_{limit} / f_{clock}$$

Example:
fc= 28.37516 MHz, $f_{upper\ limit}$= 4.75625 MHz
Value= 171.64
UPLIM= $AC (rounded hex)

4.1.14. Color Burst Amplitude (NTSC/PAL only) (13)

Command name: BURST
This is the value of the burst amplitude. The adjustment is relative to a maximum chroma amplitude of 1. This value's sign has to be negative. The positive sign can be used for test purposes. The value for PAL is $\sqrt{2}$ smaller than the value for NTSC as the sample points are shifted 45 degrees. The formulas for the calculation are:

Value =	–128 · Burst amplitude (NTSC)
range	–128...+127
Value =	–91 · Burst amplitude (PAL)
range	–128...+127

4.1.15. C Gain (all modes) (8)

Command name: CGAIN

The gain for the color subcarrier can be adjusted in front of the chroma bandpass filter. This adjustment influences the color carrier including the burst. The formula for the calculation of these values is:

CGAIN	Value = 32 · gain	range 0...31

4.1.16. Chroma Bandpass (all modes) (27...30)

Command names: CBPC1, CBPC2, CBPS1...S5, CBPG1...G5

The Chroma Bandpass Filter runs with half the clock frequency. Therefore for the calculation the sample frequency is fc/2. It consists of 5 parts in the following order:

Part 1:
One or two variable zeroes, adjustable with C1, C2, S1, G1. Switch S1 switches between one and two variable zeroes. The transfer functions are:

S1 = 0	$H(z) = 2^{-G1} \cdot (a + b \cdot z^{-1} + z^{-2})$	
where	C1 = 16 · b	range –63... +63
	C2 = 16 · a	range –63... +63
	G1 range 0...3	

S1 = 1	$H(z) = 0.5 \cdot 2^{-G1} \cdot (1 + a \cdot z^{-1} + z^{-2}) \cdot (1 + b \cdot z^{-1} + z^{-2})$	
where	C1 = 16 · (a + b)	range –63... +63
	C2 = 16·a·b +32	range –63... +63
	G1 range 0...3	

Part 2...5:
These are four identical filters, zeroes at f=0 or f= fs/2. Part 2 uses parameter S2 and G2. Part 3 uses S3 and G3. Part 4 uses S4 and G4. Part 5 uses S5 and G5. The transfer functions are:

Sn = 0	$H(z) = 2^{-Gn} \cdot (1 + z^{-1})$
Sn = 1	$H(z) = 2^{1-Gn}$
Sn = 2	$H(z) = 2^{-Gn} \cdot (1 - z^{-1})$
where	n = 2...5
	Sn = 0...2
	Gn = 0, 1

Example:
Bandpass, fc = 28.37516 MHz → fs = 14.18758 MHz
Part 1:
1 zero at f_1 = 2 MHz, 1 zero at f_2 = 6.8 MHz MHz
a = –2·cos(50.75°) = –1.265
b = –2·cos(172.55°) = 1.983
C1 = 16(a+b) = 11
C2 = 16·a·b + 32 = –8
S1 = 1 (2 variable zeroes)
G1 = 1 (gain adjustment)
Part2...5:
1 zero at f_0=fs/2, 3 zeroes at f_0= 0
S2 = 2, G2 = 1
S3 = 2, G3 = 1
S4 = 2, G4 = 0
S5 = 0, G5 = 0

4.1.17. Luminance Lowpass Filter (all modes) (38)

Command name: YLP
The luminance lowpass filter exists in two zeroes at fs/2. The transfer function is: $H(z) = 0.25(1 + 2z^{-1} + z^{-2})$
This filter works for the Y signal in the CVBS output and Y (SVHS) output. If YLP = 0 the filter is off, if YLP = 1 the filter is on.

4.1.18. Chroma Trap (all modes) (32,33)

Command names: TRAPC, TRAPS1, S2, _S3, _S4, TRAPG2, G3
This filter is in the luminance channel for the attenuation of the luminance signals in the area of the color carrier. It consists of 4 parts in series. Part 1 is an adjustable zero. Part 2 and part 3 are zeroes at fs/2 and part 4 is a peaking filter. At the end of part 2 and part 3 a gain of 1 or 2 can be selected. The transfer functions are:

Part 1:		
S1 = 0	H(z) = 1	
S1 = 1	$H(z) = 1 + c \cdot z^{-1} + z^{-2}$	
	where C = 32 · c	range –64...+63
Part 2		
S2 = 0	$H(z) = 2^{G2}$ (G2 = 0 or 1)	
S2 = 1	$H(z) = 2^{G2-1} \cdot (1 + z^{-1})$	
Part 3		
S3 = 0	$H(z) = 2^{G3}$ (G3 = 0 or 1)	
S3 = 1	$H(z) = 2^{G3-1} \cdot (1 + z^{-1})$	
Part 4		
S4 = 0	$H(z) = z^{-2}$	
S4 = 1	$H(z) = 0.25 \cdot (-1 + 4.25 \cdot z^{-2} - z^{-4})$	

Example:
Part 1:
fs = 28.63636 MHz, 1 zero at f_0 = 4.1 MHz
c = –2·cos(51.54°) = –1.244
C = 32 · c = –40
S1 = 1 (filter on)
Part 2:
1 zero at fs/2
S2 = 1
G2 = 1
Part 3:
1 zero at fs/2
S3 = 1
G3 = 1
Part 4:
Peaking on
S4 = 1

4.1.19. Luminance Gain SVHS (all modes) (31)

Command name: YGAINL
The luminance gain for the luminance signal at the SVHS output can be adjusted after the equalisation delay. The formula for the calculation of this value is:

YGAINL	Value = 64 · gain	range 0...63

4.1.20. Luminance Gain CVBS (all modes) (34)

Command name: YGAINCV
The luminance gain for the luminance signal at the composite video output can be adjusted after the chroma trap. The formula for the calculation of this value is:

YGAINCV	Value = 64 · gain	range 0...63

4.1.21. Luminance Delay (all modes) (35)

Command name: YDELAY
The delay of the luminance signal can be adjusted in steps of one clock period. The range is 0...63 clock periods. The formula for the calculation of this value is:

YDELAY	Value = delay·fc	range 0...63

4.1.22. Matching Delay SVHS Luma (all modes) (33)

Command name: YDELAYL
The matching delay of the luminance signal at the SVHS output can be adjusted in steps of one clock period. The range is 0...7 clock periods. The value depends on the setting of the chroma trap. The formula for the calculation of this value is:

YDELAYL	Value = delay·fc	range 0...7

4.1.23. Horizontal Pulses (all modes) (19...25, 39, 41)

Command names: KEYS, –E, TIMGENE, HSYNCS, –E, YBLANKS, –E, CBLANKS, –E
All these pulses are started with the low transition of the hsync input. The end of the timing generator (TIMGEN) stops the pulse generation. It must therefore have the highest value of all. While the timing generator is running, the hsync input is disabled. This is necessary to prevent the timing generator to trigger at the H/2 pulses in the vertical sync signal. All pulses, except timing generator are adjustable within a step width of two clock periods, and have a range of 2 to 510 clock periods. The timing generator has a range of 4 to 1020 clock periods.

KEY	Value = $t_{delay} \cdot f_{clock} / 2$	range 1...255
TIMGENE	Value = $t_{delay} \cdot f_{clock} / 4$	range 1...255
HSYNC	Value = $t_{delay} \cdot f_{clock} / 2$	range 1...255
YBLANK	Value = $t_{delay} \cdot f_{clock} / 2$	range 1...255
CBLANK	Value = $t_{delay} \cdot f_{clock} / 2$	range 1...255

4.1.24. Vertical Pulses (all modes) (15, 26, 36)

Command names: CSYNCD, VSYNCD, VSYNCDET, VBLANK
The delay of the composite sync can be fine-adjusted in the range of 0 to 7 clock periods.
The delay of the vertical sync pulse is adjustable in 0 to 7 H/2 steps.
The detection level for the vertical sync separator can be adjusted to start the generated vertical blanking at the start of the equalisation pulses or at the start of vertical sync pulses. A counter which runs with fc/8 starts at each rising edge of the composite sync signal. At the falling edge the counted number is compared with the detection level. If the counted number is smaller than the detection level a vertical blanking pulse will be generated.
The duration of the vertical blanking pulse (VBLANK) can be adjusted between 0 and 15.

CSYNCD	Value = $t_{delay} \cdot f_c$	range 0...7
VSYNCD	Value = $n_{H/2}$	range 0...7
VSYNC-DET	Value = $f_c \cdot t_{high} / 8$	range 0...255
VBLANK	Value = n_H	range 0...15

Example for VSYNCDET:
fc = 28.6 MHz
High time at normal line = 59.3 µs · 28.6 MHz / 8 = 212
High time at equal. pulses = 29.65 µs · 28.6 MHz / 8 = 106
High time at vsync pulses = 4.7 µs · 28.6 MHz / 8 = 17
For a start of the vertical blanking at the equal. pulses the detection level has to be between 106 and 212.
For a start of the vertical blanking at the vsync pulses the detection level has to be between 17 and 106.

Table 4–1: Data transfer to the MSE 3010

IM Bus Address	IM BUS DATA								
	MSE Data								MSE Sub-address
	15	14	13	12	11	10	9	8	0 ... 7
169	DCO Center Frequency for R-Y (Bit 16 ... 23)								0
	DCO Center Frequency for R-Y (Bit 8 ... 15)								1
	DCO Center Frequency for R-Y (Bit 0 ... 7)								2
	DCO Center Frequency for B-Y (Bit 16 ... 23)								3
	DCO Center Frequency for B-Y (Bit 8 ... 15)								4
	DCO Center Frequency for B-Y (Bit 0 ... 7)								5
	DCO Upper Frequency Limit for SECAM								6
	DCO Lower Frequency Limit for SECAM								7
	X	X	X	Color Carrier Gain Adjustment					8
	SECAM Antibell Filter Coefficient A								9
	SECAM Antibell Filter Coefficient B								10
	X	SECAM Preemphasis Filter Coefficient A							11
	X	X	SECAM Preemphasis Filter Coefficient B						12
	PAL/NTSC Color Burst Amplitude								13
	Chroma Lowpass Filter Peaking Coefficient								14
	X	Composite Sync Delay			X	Chroma Lowpass Filter Select			15
	X	X	X	Chroma Lowpass Filter Test Switches					16
	X	B-Y Gain							17
	X	R-Y Gain							18
	Luminance Blanking Start								19
	Luminance Blanking End								20
	Horizontal Sync Start								21
	Horizontal Sync End								22

Table 4–1, continued

IM Bus Address	IM BUS DATA								
	MSE Data								MSE Sub-address
	15	14	13	12	11	10	9	8	0 ... 7
169	Key Pulse Start								23
	Key Pulse End								24
	Horizontal Timing Generator Disable Duration								25
	Vertical Blanking Duration (at Csync Input)					Vertical Sync Delay (at Vsync Input)			26
		Chroma Bandpass Filter Coefficient C1							27
		Chroma Bandpass Filter Coefficient C2							28
		Gain 5 0:Gain=1 1:Gain=0.5	Gain 4 0:Gain=1 1:Gain=0.5	Gain 3 0:Gain=1 1:Gain=0.5	Gain 2 0:Gain=1 1:Gain=0.5	Gain 1 0:Gain=1 1:Gain=0.5 2:Gain=0.25 3:Gain=0.125		Switch 1 0:1 Variable Zero 1:2 Variable Zeroes	29
	Sign 5	Switch 5	Sign 4	Switch 4	Sign 3	Switch 3	Sign 2	Switch 2	30
	Switch: 0: Filter on 1: Filter off				Sign: $0 = 1 + z^{-1}$ $1 = 1 - z^{-1}$				
			Y Output Luminance Gain						31
	Switch 1 0 : Filter 1 off 1 : Filter 1 on	Chroma Trap Coefficient for Filter 1 (Variable Zero)							32
	Y Output Matching Delay			Gain 3 Gain 0: 1 1: 2	Gain 2 Gain 0: 1 1: 2	Switch 4 Peaking 0 = off 1 = on	Switch 3 $0 : z^{-1}$ 1: 0.5 $(1+z^{-1})$	Switch 2 $0 = z^{-1}$ 1: 0.5 · $(1+z^{-1})$	33
			CVBS Output Luminance Gain						34
			CVBS, Y Output Luminance Delay						35
	Detection Level for Vertical Sync Separator								36
	Test Switch	Encoder Blanking Disable	RGB Pedestal Disable	Test Switches					37

Table 4–1, continued

IM Bus Address	IM Bus Data MSE Data								MSE Sub-address
	15	14	13	12	11	10	9	8	0 ... 7
169	Test Switches		Luma Lowpass 1 : on	Test Switches					38
	Chroma Blanking Start								39
	0: Vsync 1: Blanking	0: H/Vsync 1: Csync	0: RGB 1: YUV	0: PAL 1: SECAM	0: PAL 1: NTSC	1: Load Parameter Table	Parameter Table Select		40
	Chroma Blanking End								41

Table 4–2, Default parameters for NTSC Mode (f_C= 28.63636 MHz)

Data (Binary) 7 6 5 4 3 2 1 0	*(Hex)*	*Subaddr. (Hex)*
0 1 0 0 0 0 0 0	40	00
0 0 0 0 0 0 0 0	00	01
0 0 0 0 0 0 0 0	00	02
0 1 0 0 0 0 0 0	40	03
0 0 0 0 0 0 0 0	00	04
0 0 0 0 0 0 0 0	00	05
1 1 1 1 1 1 1 1	FF	06
0 0 0 0 0 0 0 0	00	07
X X X 1 1 1 0 0	1C	08
0 0 0 0 0 0 0 0	00	09
0 0 0 0 0 0 0 0	00	0A
X 0 0 0 0 0 0 0	00	0B
X X 0 0 0 0 0 0	00	0C
1 1 0 1 0 0 1 1	D3	0D
1 1 0 0 1 1 1 0	CE	0E
X 1 0 1 X 1 0 1	55	0F
X X X 0 0 0 0 0	00	10
X 0 1 0 1 1 1 0	2E	11
X 1 0 1 0 0 1 0	52	12
0 0 0 0 0 1 1 0	06	13
0 1 0 1 1 1 0 0	5C	14
0 0 0 0 0 0 0 1	01	15
0 0 0 0 0 0 1 0	02	16
0 0 1 1 0 1 0 1	35	17
0 1 0 0 0 1 1 1	47	18
1 1 0 0 1 0 0 0	C8	19
1 1 1 1 X 0 0 1	F1	1A
X 0 0 0 0 0 0 0	00	1B
X 0 0 0 0 0 0 0	00	1C
X 1 1 1 1 0 0 0	78	1D
0 1 0 1 0 1 0 1	55	1E
X X 1 0 0 1 0 1	25	1F
1 1 0 1 1 0 0 0	D8	20
0 1 1 1 1 1 1 1	7F	21
X X 0 1 0 0 1 1	13	22
X X 0 0 1 1 0 1	0D	23
1 0 0 1 1 1 1 1	9F	24
X 0 0 0 0 0 0 0	00	25
0 0 1 0 0 0 0 0	20	26
0 0 0 0 1 0 1 1	0B	27
1 1 0 0 1 0 0 0	C8	28
0 1 0 1 0 0 1 0	52	29

Table 4–3, Default parameters for PAL Mode (f_C= 28.37516 MHz)

Data (Binary) 7 6 5 4 3 2 1 0	*(Hex)*	*Subaddr. (Hex)*
0 1 0 1 0 0 0 0	50	00
0 0 0 0 0 0 0 0	00	01
0 0 0 0 0 0 0 0	00	02
0 1 0 1 0 0 0 0	50	03
0 0 0 0 0 0 0 0	00	04
0 0 0 0 0 0 0 0	00	05
1 1 1 1 1 1 1 1	FF	06
0 0 0 0 0 0 0 0	00	07
X X X 1 1 0 0 1	19	08
0 0 0 0 0 0 0 0	00	09
0 0 0 0 0 0 0 0	00	0A
X 0 0 0 0 0 0 0	00	0B
X X 0 0 0 0 0 0	00	0C
1 1 1 0 0 0 0 0	E0	0D
1 1 0 0 1 1 1 0	CE	0E
X 1 0 1 X 1 1 1	57	0F
X X X 0 0 0 0 0	00	10
X 0 1 0 0 1 0 1	25	11
X 1 0 0 0 0 1 0	42	12
0 0 0 0 0 1 1 0	06	13
0 1 0 1 1 1 0 0	5C	14
0 0 0 0 0 0 0 1	01	15
0 0 0 0 0 0 1 0	02	16
0 0 1 1 0 1 0 0	34	17
0 1 0 0 0 1 1 1	47	18
1 1 0 0 1 0 0 0	C8	19
1 1 1 1 X 0 0 1	F1	1A
X 0 0 0 0 0 0 0	00	1B
X 0 0 0 0 0 0 0	00	1C
X 1 1 1 1 0 0 0	78	1D
0 1 0 1 0 1 0 1	55	1E
X X 1 0 0 1 0 0	24	1F
1 1 0 1 1 1 0 1	DD	20
1 0 1 1 1 1 1 1	BF	21
X X 0 1 0 0 0 1	11	22
X X 0 1 0 0 0 0	10	23
1 0 0 1 1 1 1 1	9F	24
X 0 0 0 0 0 0 0	00	25
0 0 1 0 0 0 0 0	20	26
0 0 0 0 1 0 1 1	0B	27
1 1 0 0 0 0 0 0	C0	28
0 1 0 1 0 0 1 0	52	29

Table 4–4, Default parameters for SECAM Mode (f_C= 28.37516 MHz)

Data (Binary) 7 6 5 4 3 2 1 0	*(Hex)*	*Subaddr. (Hex)*
0 1 0 0 1 1 1 1	4F	00
1 0 0 0 0 0 0 0	80	01
0 1 1 0 1 1 0 0	6C	02
0 1 0 0 1 1 0 0	4C	03
1 0 1 0 1 1 1 1	AF	04
1 1 0 1 0 0 0 1	D1	05
1 0 1 0 1 0 1 1	AB	06
1 0 0 0 1 1 0 0	8C	07
X X X 0 0 1 1 0	06	08
0 1 0 0 1 1 0 1	4D	09
0 1 1 1 0 0 0 1	71	0A
X 1 1 0 1 1 1 1	6F	0B
X X 1 0 1 0 0 0	28	0C
0 0 0 0 0 0 0 0	00	0D
1 1 0 0 1 1 1 0	CE	0E
X 1 0 1 X 1 0 1	55	0F
X X X 0 0 0 0 0	00	10
X 0 1 0 1 0 0 1	29	11
X 1 0 0 0 0 0 0	40	12
0 0 0 0 1 0 0 0	08	13
0 1 0 1 1 1 1 0	5E	14
0 0 0 0 0 0 0 1	01	15
0 0 0 0 0 0 1 0	02	16
0 0 0 0 0 0 0 1	01	17
0 0 0 0 0 0 1 0	02	18
1 1 0 0 1 0 0 0	C8	19
1 1 1 1 X 0 0 1	F1	1A
X 0 0 0 1 0 1 1	0B	1B
X 1 1 1 0 1 1 1	77	1C
X 0 0 1 1 0 1 1	1B	1D
0 0 1 0 1 0 1 0	2A	1E
X X 1 0 0 1 0 0	24	1F
1 1 0 1 1 1 0 0	DC	20
1 0 1 1 0 1 1 1	B7	21
X X 1 0 0 1 0 0	24	22
X X 0 1 1 0 0 1	19	23
1 0 0 1 1 1 1 1	9F	24
X 1 0 0 0 0 0 0	40	25
0 0 1 0 0 0 0 0	20	26
0 0 0 0 1 1 1 1	0F	27
1 1 0 1 0 0 0 0	D0	28
0 0 1 1 1 0 0 0	38	29

Table 4–5, Default parameters for PAL-M Mode (f_C= 28.63636 MHz)

Data (Binary) 7 6 5 4 3 2 1 0	*(Hex)*	*Subaddr. (Hex)*
0 0 1 1 1 1 1 1	3F	00
1 1 1 0 1 1 1 0	EE	01
0 0 0 0 0 1 0 0	04	02
0 0 1 1 1 1 1 1	3F	03
1 1 1 0 1 1 1 0	EE	04
0 0 0 0 0 1 0 0	04	05
1 1 1 1 1 1 1 1	FF	06
0 0 0 0 0 0 0 0	00	07
X X X 1 1 1 0 0	1C	08
0 0 0 0 0 0 0 0	00	09
0 0 0 0 0 0 0 0	00	0A
X 0 0 0 0 0 0 0	00	0B
X X 0 0 0 0 0 0	00	0C
1 1 0 1 1 0 0 0	D8	0D
1 1 0 0 1 1 1 0	CE	0E
X 1 0 1 X 1 0 1	55	0F
X X X 0 0 0 0 0	00	10
X 0 1 0 1 1 1 0	2E	11
X 1 0 1 0 0 2 0	52	12
0 0 0 0 0 1 1 0	06	13
0 1 0 1 1 1 0 0	5C	14
0 0 0 0 0 0 0 1	01	15
0 0 0 0 0 0 1 0	02	16
0 0 1 1 0 1 0 1	35	17
0 1 0 0 0 1 1 1	47	18
1 1 0 0 1 0 0 0	C8	19
1 1 1 1 X 0 0 1	F1	1A
X 0 0 0 0 0 0 0	00	1B
X 0 0 0 0 0 0 0	00	1C
X 1 1 1 1 0 0 0	78	1D
0 1 0 1 0 1 0 1	55	1E
X X 1 0 0 1 0 1	25	1F
1 1 0 1 1 0 0 0	D8	20
0 1 1 1 1 1 1 1	7F	21
X X 0 1 0 0 1 1	13	22
X X 0 0 1 1 0 1	0D	23
1 0 0 1 1 1 1 1	9F	24
X 0 0 0 0 0 0 0	00	25
0 0 1 0 0 0 0 0	20	26
0 0 0 0 1 0 1 1	0B	27
1 1 0 0 0 0 0 0	C0	28
0 1 0 1 0 0 1 0	52	29

MICRONAS INTERMETALL GmbH
Hans-Bunte-Strasse 19
D-79108 Freiburg (Germany)
P.O. Box 840
D-79008 Freiburg (Germany)
Tel. +49-761-517-0
Fax +49-761-517-2174
E-mail: docservice@intermetall.de
Internet: http://www.intermetall.de

Printed in Germany
Order No. 6251-351-1PD