# 3.3V PLL Clock Driver

**MPC974**

**LOW VOLTAGE**
**PLL CLOCK DRIVER**

The MPC974 is a fully integrated PLL based clock generator and clock distribution chip which operates from a 3.3V supply. The MPC974 is ideally suited for high speed, timing critical designs which need a high level of clock fanout. The device features 15 high drive LVCMOS outputs, each output has the capability of driving a 50Ω parallel terminated transmission line or two 50Ω series terminated transmission lines on the incident edge.

- Fully Integrated PLL
- Two Reference Clock Inputs for Redundant Clock Applications
- High Impedance Output Control
- Logic Enable on the Outputs
- 3.3V $V_{CC}$ Supply
- Output Frequency Configurable
- TQFP Packaging
- ±100ps Typical Cycle–to–Cycle Jitter

**FA SUFFIX**
52–LEAD TQFP PACKAGE
CASE 848D-03

The MPC974 features 3 independent frequency programmable banks of outputs. The frequency programmability offers the capability of establishing output frequency relationships of 1:1, 2:1, 3:1, 3:2 and 3:2:1. In addition, the device features a separate feedback output which allows for a wide variety of input/output frequency multiplication alternatives. The VCO_Sel pin provides an extended VCO lock range for added flexibility and general purpose usage.

The TCLK0 and TCLK1 inputs provide a method for dynamically switching the PLL between two different clock sources. The PLL has been optimized to provide small deviations in output pulse width and well controlled, slow transition back to lock when the inputs are switched between two references that are equal in frequency but out of phase with each other. This feature makes the MPC974 an ideal solution for fault tolerant applications which require redundant clock sources.

All of the control pins are LVTTL/LVCMOS level inputs. The Fsel pins control the VCO divide ratios that are applied to the various output banks and the feedback output. The MR input will reset the internal flip flops and place the outputs in high impedance when driven LOW. The OE pin will force all of the outputs except the feedback output LOW to allow for acquiring phase lock prior to providing clocks to the rest of the system. Note that the OE pin is not synchronized to the internal clock. As a result, the initial pulse after de–assertion of the OE pin may be distorted. The PLL_En pin allows the PLL to be bypassed for board level functional test. When bypassed the signal on the selected TCLK will be routed around the PLL and will drive the internal dividers directly.

The MPC974 is packaged in the 52–lead TQFP package to provide optimum electrical performance as well as minimize board space requirements. The device is specified for 3.3V $V_{CC}$.

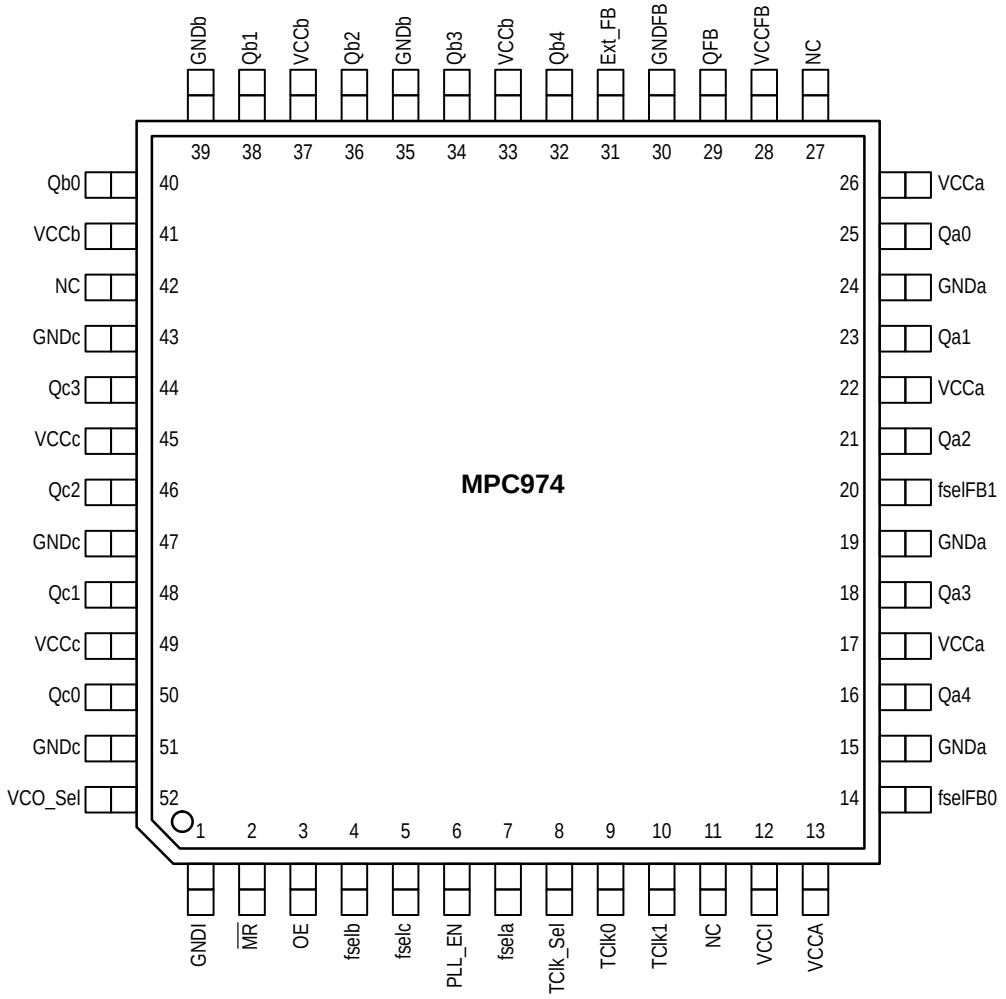



**Figure 1. 52–Lead Pinout** (Top View)

**FUNCTION TABLE 1**

| fsela | Qa | fselb | Qb | fselc | Qc |
|---|---|---|---|---|---|
| 0 | ÷2 | 0 | ÷2 | 0 | ÷4 |
| 1 | ÷4 | 1 | ÷4 | 1 | ÷6 |

**FUNCTION TABLE 2**

| fselFB0 | fselFB1 | QFB |
|---|---|---|
| 0 | 0 | ÷4 |
| 0 | 1 | ÷6 |
| 1 | 0 | ÷8 |
| 1 | 1 | ÷12 |

**FUNCTION TABLE 3**

| VCO_Sel | fVCO |
|---|---|
| 0 | VCO/2 |
| 1 | VCO/4 |

**FUNCTION TABLE 4**

| Control Pin | Logic ‘0’ | Logic ‘1’ |
|---|---|---|
| $\overline{\text{MR}}$ | Master Reset/Output High Z | – |
| PLL_EN | Bypass PLL | Enable PLL |
| TClk_Sel | TCLK0 | TCLK1 |
| OE | Qa, Qb, Qc Logic LOW | All Outputs Enabled |

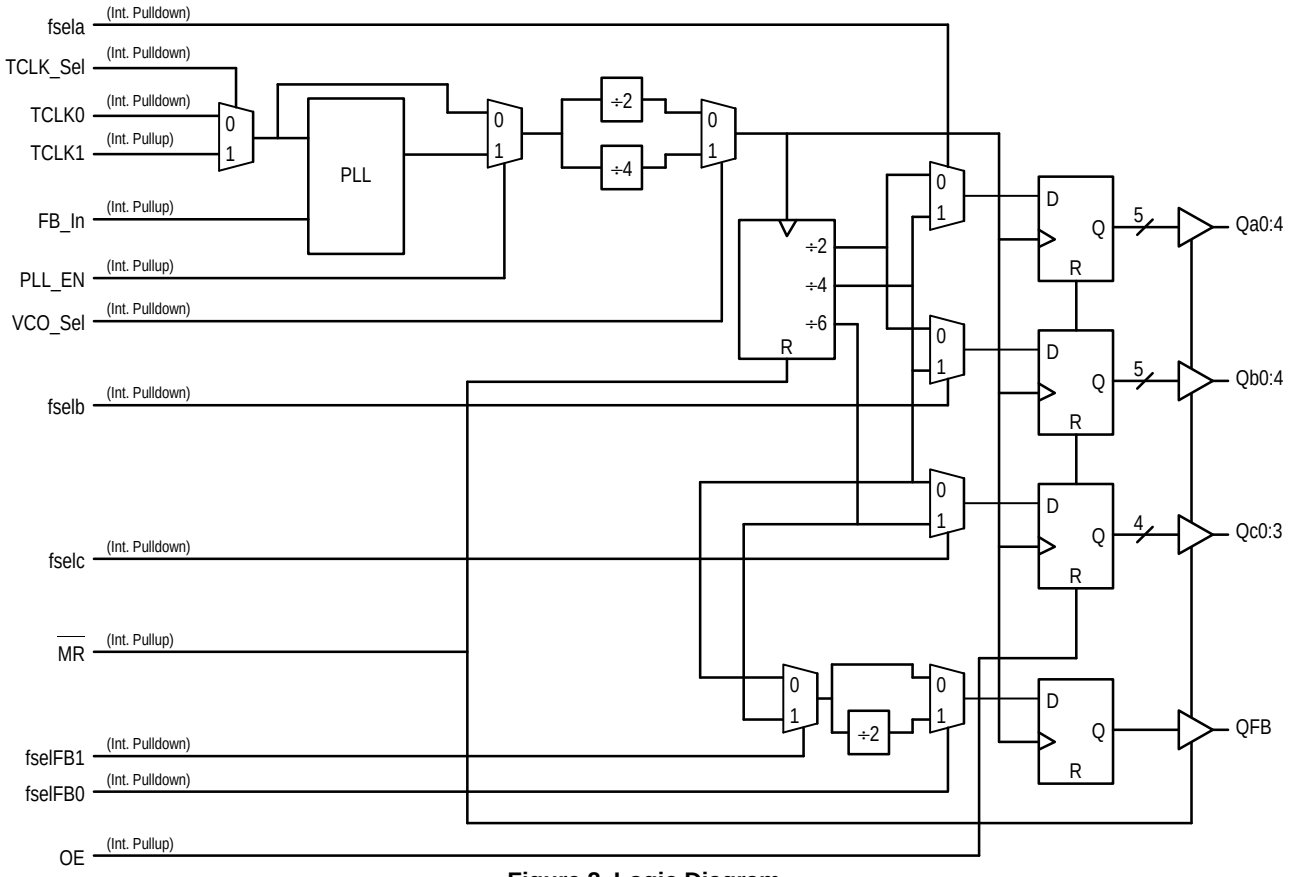



**Figure 2. Logic Diagram**

## ABSOLUTE MAXIMUM RATINGS*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 5.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | 8 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

## DC CHARACTERISTICS ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | $V_{CC}$ | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –20mA (Note 1.) |
| $V_{OL}$ | Output LOW Voltage | | | 0.5 | V | $I_{OL}$ = 20mA (Note 1.) |
| $I_{IN}$ | Input Current | | | ±100 | µA | Note 2. |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 120 | mA | |
| $C_{IN}$ | Input Capacitance | | | 8 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | 25 | | pF | Per Output |

1. The MPC974 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}$/2) transmission lines on the incident edge (see Applications Info section).
2. Inputs have either pull–up or pull–down resistors which affect input current.

**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$ = 0 to 70°C)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_r$, $t_f$ | TCLK Input Rise/Falls | | 3.0 | ns | |
| $f_{ref}$ | Reference Input Frequency | Note 3. | Note 3. | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | 75 | % | |

3. Input reference frequency is limited by the divider selection and the VCO lock range.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time (Note 4.) | 0.15 | | 1.5 | ns | 0.8 to 2.0V |
| $t_{pw}$ | Output Duty Cycle (Note 4.) | $t_{CYCLE}/2$ –800 | $t_{CYCLE}/2$ ±500 | $t_{CYCLE}/2$ +800 | ps | |
| $f_{VCO}$ | PLL VCO Lock Range fseln, fselFBn = ÷4 to ÷12 | 200 | | 500 | MHz | Note 5. |
| $t_{pd}$ | SYNC to Feedback Propagation Delay | –250 | | 100 | ps | Notes 4., 6. |
| $t_{os}$ | Output-to-Output Skew | | | 350 | ps | Note 4. |
| $f_{max}$ | Maximum Output Frequency Q (÷2)<br>Q (÷4)<br>Q (÷6) | | | 125<br>63<br>42 | MHz | VCO_Sel = 0 |
| $t_{PZL}$ | Output Enable Time | 2 | | 10 | ns | |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | 2 | | 10 | ns | |
| $t_{jitter}$ | Cycle–to–Cycle Jitter (Peak–to–Peak) | | ±100 | | ps | |
| $t_{lock}$ | Maximum PLL Lock Time | | | 10 | ms | |

4. 50Ω transmission lines terminated to $V_{CC}/2$.
5. The PLL will be unstable if the total divide between the VCO and the feedback pin is less < 8. VCO_SEL = '0', fsela or fselb = '0' cannot be used for the PLL feedback signal.
6. $t_{pd}$ is specified for 50MHz input reference. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The $t_{pd}$ does not include jitter.

## APPLICATIONS INFORMATION

### Programming the MPC974

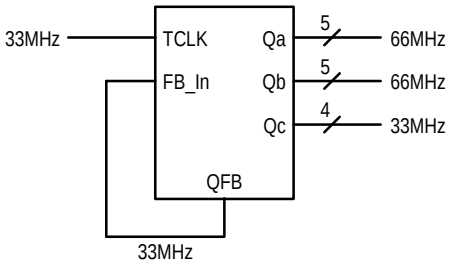
The MPC974 clock driver outputs can be configured into several frequency relationships, in addition the external feedback option allows for a great deal of flexibility in establishing unique input–to–output frequency relationships. The output dividers for the four output groups allows the user to configure the outputs into 1:1, 2:1, 3:2 and 3:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Function Table 1 illustrates the various output configurations, the table describes the outputs using the VCO frequency as a reference. As an example for a 3:2:1 relationship the Qa outputs would be set at VCO/2, the Qb's and Qc's at VCO/4 and the Qd's at VCO/6. These settings will provide output frequencies with a 3:2:1 relationship.

The division settings establish the output relationship, but one must still ensure that the VCO will be stable given the frequency of the outputs desired. The VCO lock range can be found in the specification tables. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL is such that for output frequencies between 10 and 125MHz the MPC974 can generally be configured into a stable region.

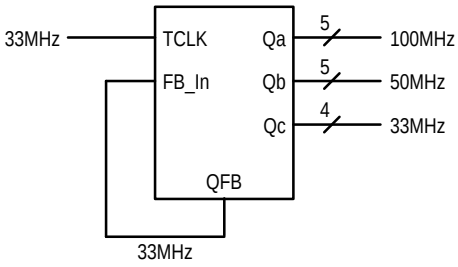
The relationship between the input reference and the output frequency is also very flexible. The separate PLL feedback output allows for a wide range of output vs input frequency relationships. Function Table 1 can be used to identify the potential relationships available. Figure 3 illustrates several programming possibilities, although not exhaustive it is representative of the potential applications.

### Using the MPC974 as a Zero Delay Buffer

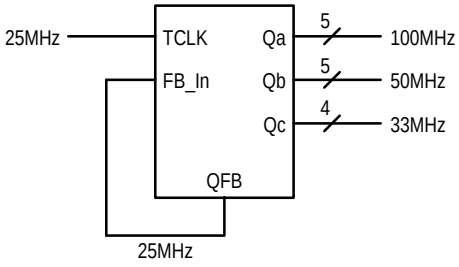
The external feedback option of the MPC974 clock driver allows for its use as a zero delay buffer. By using one of the outputs as a feedback to the PLL the propagation delay through the device is near zero. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The static phase offset is a function of the input reference frequency of the MPC974. The Tpd of the device is specified in the specification tables.



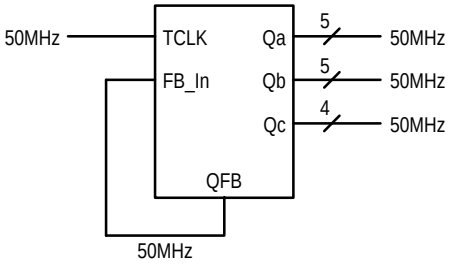

| fsela | fselb | fselc | fselFB | VCO_Sel |
|---|---|---|---|---|
| 0 | 0 | 0 | 00 | 0 |




| fsela | fselb | fselc | fselFB | VCO_Sel |
|---|---|---|---|---|
| 0 | 1 | 1 | 10 | 0 |




| fsela | fselb | fselc | fselFB | VCO_Sel |
|---|---|---|---|---|
| 0 | 1 | 1 | 01 | 0 |




| fsela | fselb | fselc | fselFB | VCO_Sel |
|---|---|---|---|---|
| 1 | 1 | 0 | 00 | 0 |

**Figure 3. MPC974 Programming Schemes**

To minimize part–to–part skew the external feedback option again should be used. The PLL in the MPC974 decouples the delay of the device from the propagation delay variations of the internal gates. From the specification table one sees a Tpd variation of only ±150ps, thus for multiple devices under identical configurations the part–to–part skew will be around 850ps (300ps for Tpd variation plus 350ps output–to–output skew plus 200ps for jitter). To minimize this value, the highest possible reference frequencies should be used. Higher reference frequencies will minimize both the $t_{pd}$ parameter as well as the input to output jitter.

### Power Supply Filtering

The MPC974 is a mixed analog/digital product and exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC974 provides separate power supplies for the output buffers ($V_{CCO}$) and the internal PLL (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC974.

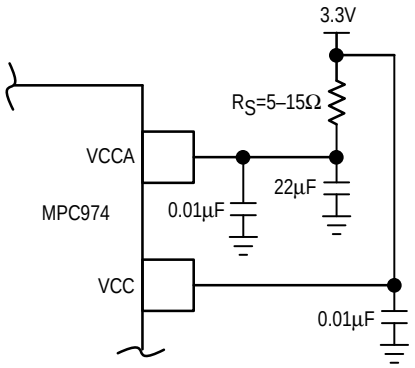



**Figure 4. Power Supply Filter**

Figure 4 illustrates a typical power supply filter scheme. The MPC974 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the VCCA pin of the MPC974. From the data sheet the $I_{VCCA}$ current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 4 must have a resistance of 10–15Ω to meet

the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC974 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Driving Transmission Lines**

The MPC974 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

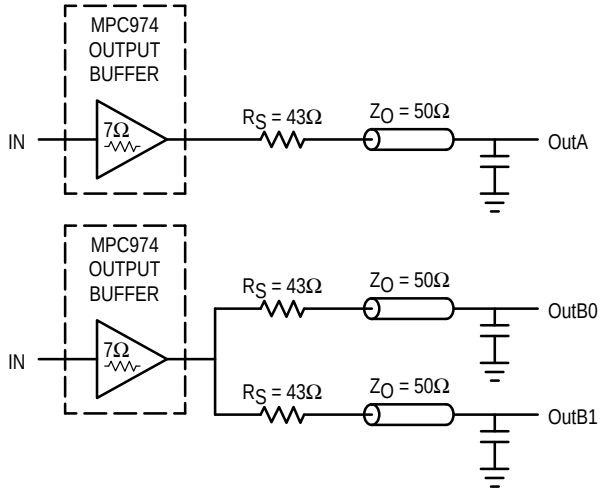



**Figure 5. Single versus Dual Transmission Lines**

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC974 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 5 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC974 clock driver is effectively doubled due to its capability to drive multiple lines.

The waveform plots of Figure 6 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC974 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC974. The output waveform in Figure 6 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

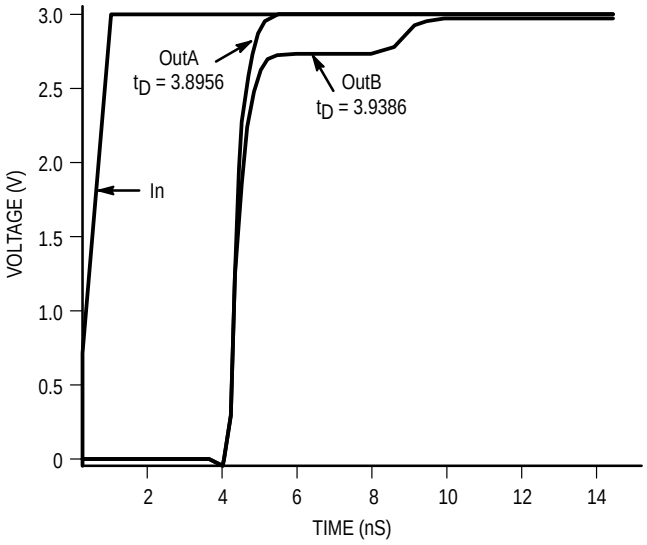



**Figure 6. Single versus Dual Waveforms**

VL = VS ( Zo / Rs + Ro +Zo) = 3.0 (25/53.5) = 1.40V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 7 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

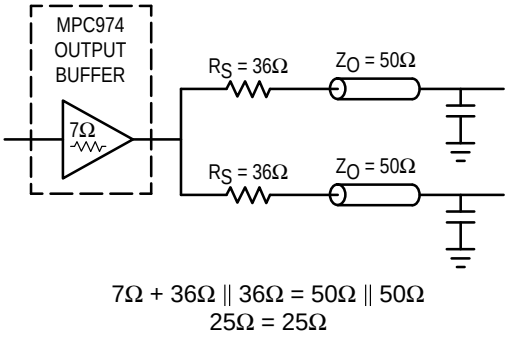
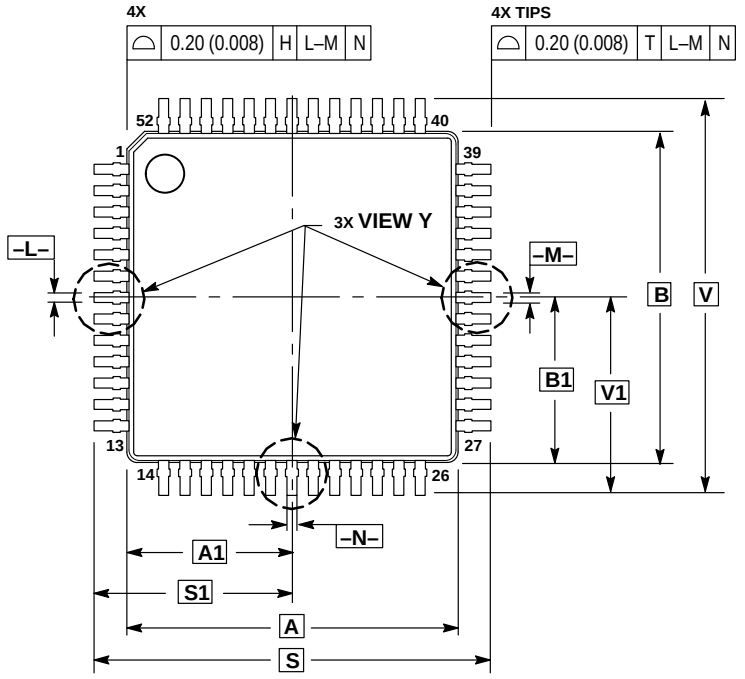
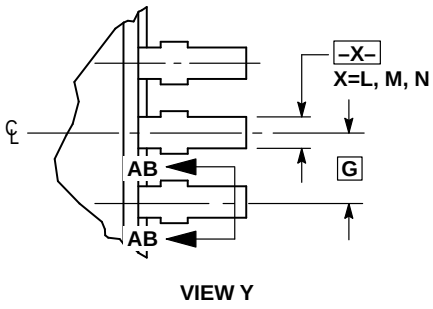


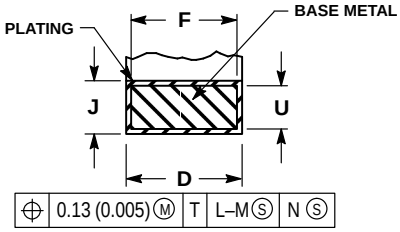

**Figure 7. Optimized Dual Line Termination**

## OUTLINE DIMENSIONS

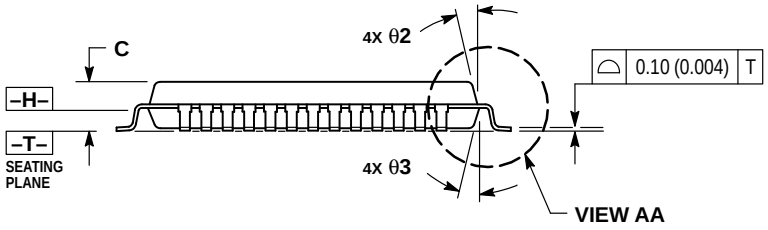
**FA SUFFIX**
TQFP PACKAGE
CASE 848D-03
ISSUE C

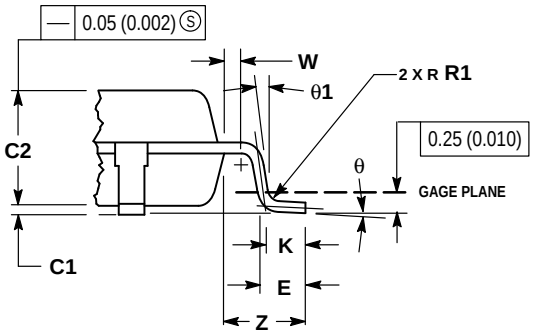



**SECTION AB–AB**
**ROTATED 90° CLOCKWISE**




VIEW AA

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 10.00 BSC | | 0.394 BSC | |
| A1 | 5.00 BSC | | 0.197 BSC | |
| B | 10.00 BSC | | 0.394 BSC | |
| B1 | 5.00 BSC | | 0.197 BSC | |
| C | — | 1.70 | — | 0.067 |
| C1 | 0.05 | 0.20 | 0.002 | 0.008 |
| C2 | 1.30 | 1.50 | 0.051 | 0.059 |
| D | 0.20 | 0.40 | 0.008 | 0.016 |
| E | 0.45 | 0.75 | 0.018 | 0.030 |
| F | 0.22 | 0.35 | 0.009 | 0.014 |
| G | 0.65 BSC | | 0.026 BSC | |
| J | 0.07 | 0.20 | 0.003 | 0.008 |
| K | 0.50 REF | | 0.020 REF | |
| R1 | 0.08 | 0.20 | 0.003 | 0.008 |
| S | 12.00 BSC | | 0.472 BSC | |
| S1 | 6.00 BSC | | 0.236 BSC | |
| U | 0.09 | 0.16 | 0.004 | 0.006 |
| V | 12.00 BSC | | 0.472 BSC | |
| V1 | 6.00 BSC | | 0.236 BSC | |
| W | 0.20 REF | | 0.008 REF | |
| Z | 1.00 REF | | 0.039 REF | |
| θ | 0° | 7° | 0° | 7° |
| θ1 | 0° | — | 0° | — |
| θ2 | 12° REF | | 12° REF | |
| θ3 | 5° | 13° | 5° | 13° |

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