Product Preview

Low Voltage 1:27 Clock Distribution Chip

MPC941

LOW VOLTAGE 1:27 CLOCK DISTRIBUTION CHIP

The MPC941 is a 1:27 low voltage clock distribution chip. The device features the capability to select either a differential LVPECL or an LVTTL/LVCMOS compatible input. The 27 outputs are LVCMOS or LVTTL compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output–to–output skews of 250ps, the MPC941 is ideal as a clock distribution chip for the most demanding of synchronous systems. For a similar product with a smaller number of outputs, please consult the MPC940 data sheet.

- LVPECL or LVCMOS/LVTTL Clock Input
- 250ps Maximum Targeted Output–to–Output Skew
- Drives Up to 54 Independent Clock Lines
- Maximum Output Frequency of 250MHz
- High Impedance Output Enable
- 52–Lead TQFP Packaging
- 3.3V V_{CC} Supply Voltage

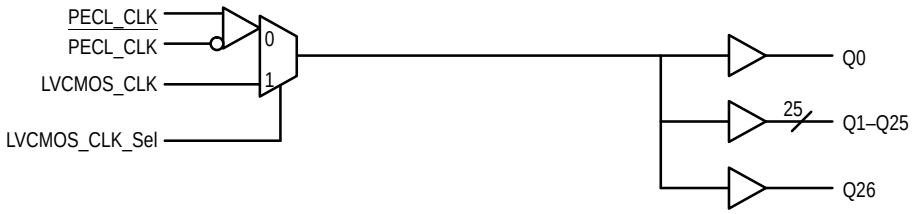
FA SUFFIX
52–LEAD TQFP PACKAGE
CASE 848D–03

With a low output impedance, in both the HIGH and LOW logic states, the output buffers of the MPC941 are ideal for driving series terminated transmission lines. More specifically, each of the 27 MPC941 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC941 has an effective fanout of 1:54 in applications where each line drives a single load. With this level of fanout, the MPC941 provides enough copies of low skew clocks for most high performance synchronous systems.

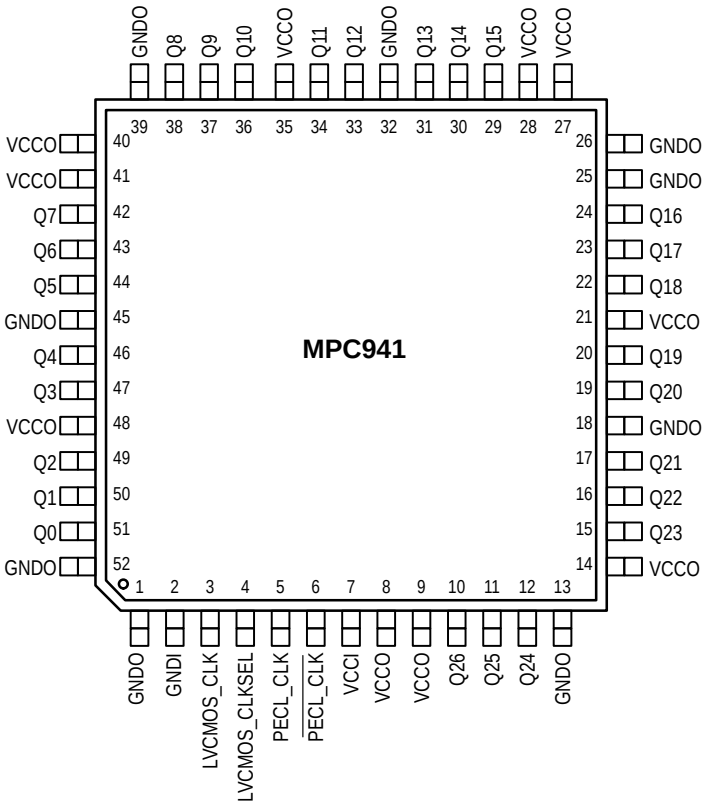
The differential LVPECL inputs of the MPC941 allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS/LVTTL input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLK_Sel pin will select the TTL level clock input.

The MPC941 is fully 3.3V compatible. The 52–lead TQFP package was chosen to optimize performance, board space and cost of the device. The 52–lead TQFP has a 10x10mm body size with a conservative 0.65mm pin spacing.

LOGIC DIAGRAM



Pinout: 52–Lead TQFP (Top View)



FUNCTION TABLE

LVCMOS_CLK_Sel	Input
0	PECL_CLK
1	LVCMOS_CLK

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	PECL_CLK Other				V	
V_{IL}	Input LOW Voltage	PECL_CLK Other				V	
V_{PP}	Peak–to–Peak Input Voltage	PECL_CLK				mV	
V_{CMR}	Common Mode Range	PECL_CLK				V	
V_{OH}	Output HIGH Voltage					V	Note NO TAG
V_{OL}	Output LOW Voltage					V	Note NO TAG
I_{IN}	Input Current					µA	
C_{IN}	Input Capacitance					pF	
C_{pd}	Power Dissipation Capacitance					pF	
I_{CC}	Maximum Quiescent Supply Current					mA	

1. The MPC941 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge.

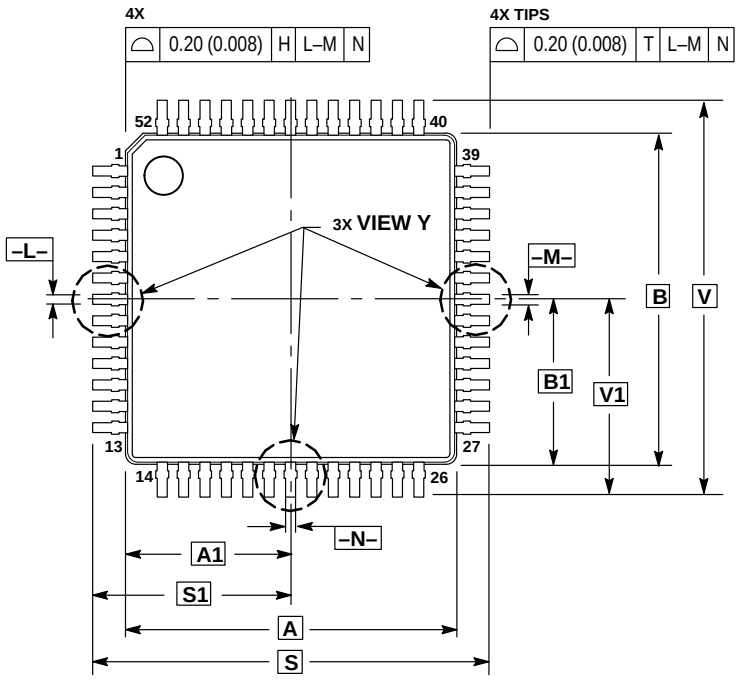
AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

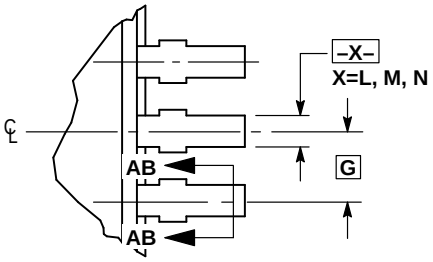
Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency			250		MHz	Note NO TAG
t_{pd}	Propagation Delay	PECL_CLK to Q TTL_CLK to Q		3.0 3.0		ns	Note NO TAG
$t_{sk(o)}$	Output–to–Output Skew			250		ps	Note NO TAG
$t_{sk(pr)}$	Part–to–Part Skew	PECL_CLK to Q TTL_CLK to Q		650 650		ps	Note NO TAG
t_{pwo}	Output Pulse Width			t_{CYCLE}/2 ±500		ps	Note NO TAG, Measured at V_{CC}/2
t_r, t_f	Output Rise/Fall Time		0.20		1.0	ns	0.8V to 2.0V

2. Driving 50Ω transmission lines.
3. Part–to–part skew at a given temperature and voltage.

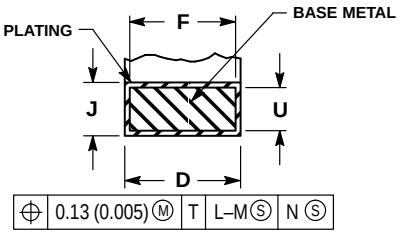
OUTLINE DIMENSIONS

FA SUFFIX
PLASTIC TQFP PACKAGE
CASE 848D–03
ISSUE C

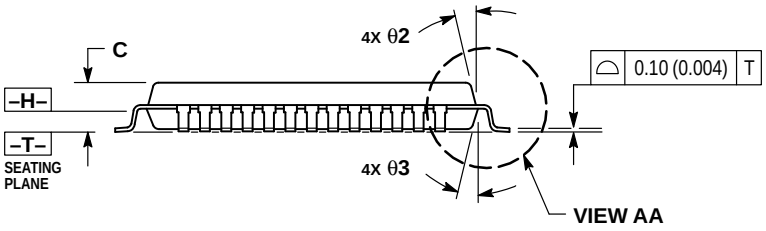


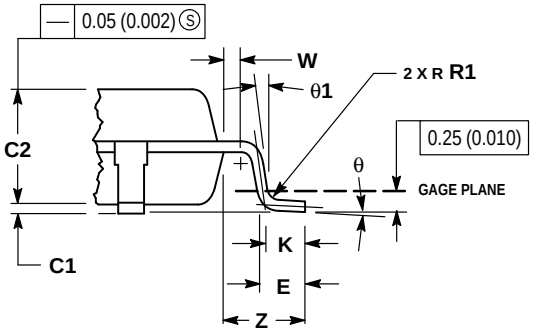


VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE





VIEW AA

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	—	1.70	—	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12° REF		12° REF	
θ3	5°	13°	5°	13°

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