

## *Product Preview*

# **Low Voltage CMOS 1:18 Clock Distribution Chip**

The MPC909 is a 1:18 low voltage clock distribution chip. The 18 outputs are LVCMOS or LVTTTL compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output-to-output skews of 250ps, the MPC909 is ideal as a clock distribution chip for the cost sensitive, high performance designs. With low cost as one of the critical parameters, technology, design and test choices were made which adversely affect part-to-part skew performance. For very high performance applications, where part-to-part skew is critical, please refer to the MPC940 datasheet.

- LVCMOS/LVTTTL Clock Inputs and Outputs
- 250ps Maximum Targeted Output-to-Output Skew
- Drives Up to 36 Independent Clock Lines
- Maximum Output Frequency of 100MHz
- High Impedance Output Enable
- 32-Lead TQFP Packaging
- 3.3V  $V_{CC}$  Supply Voltage

With a low output impedance, in both the HIGH and LOW logic states, the output buffers of the MPC909 are ideal for driving series terminated transmission lines. More specifically, each of the 18 MPC909 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC909 has an effective fanout of 1:36 in applications where each line drives a single load. With this level of fanout, the MPC909 provides enough copies of low skew clocks for many high performance synchronous systems.

The MPC909 is fully 3.3V compatible. The 32-lead TQFP package was chosen to optimize performance, board space and cost of the device. The 32-lead TQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

**MPC909**

**LOW VOLTAGE CMOS  
1:18 CLOCK  
DISTRIBUTION CHIP**

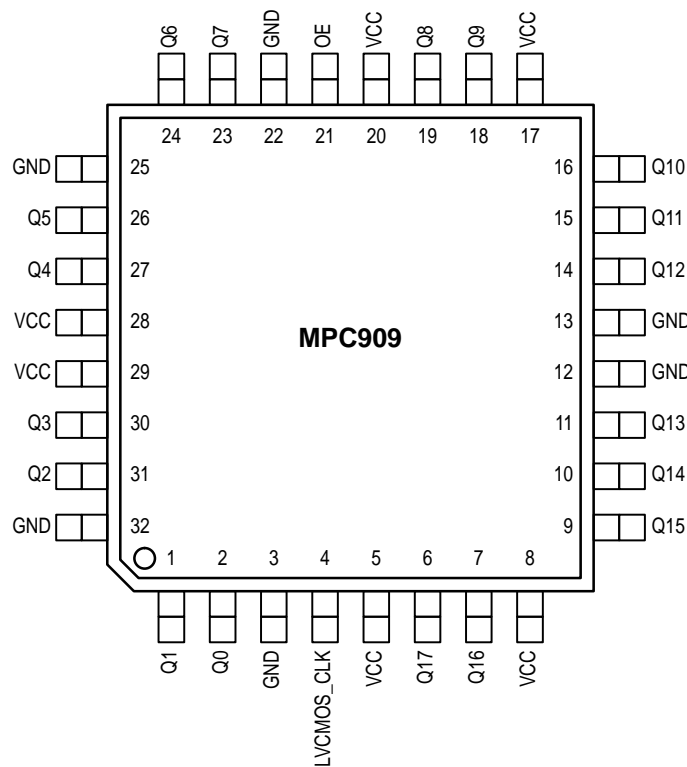


**FA SUFFIX**  
32-LEAD TQFP PACKAGE  
CASE 873A-02





Figure 1. Logic Diagram



FUNCTION TABLE

OE	Output
0	High-Z
1	Enabled

Figure 2. 32-Lead Pinout (Top View)

**ABSOLUTE MAXIMUM RATINGS\***

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Supply Voltage	-0.3	3.6	V
$V_I$	Input Voltage	-0.3	$V_{DD} + 0.3$	V
$I_{IN}$	Input Current		$\pm 20$	mA
$T_{Stor}$	Storage Temperature Range	-40	125	°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**DC CHARACTERISTICS** ( $T_A = 0^\circ$  to  $70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 5\%$ , or  $2.5\text{V} \pm 5\%$ )

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
$V_{IH}$	Input HIGH Voltage	2.0		3.6	V	
$V_{IL}$	Input LOW Voltage			0.8	V	
$V_{OH}$	Output HIGH Voltage	2.4			V	Note 1., $I_{OH} = -20\text{mA}$
$V_{OL}$	Output LOW Voltage			0.5	V	Note 1., $I_{OL} = 20\text{mA}$
$I_{IN}$	Input Current			TBD	$\mu\text{A}$	
$C_{IN}$	Input Capacitance			TBD	pF	
$C_{pd}$	Power Dissipation Capacitance			TBD	pF	
$I_{CC}$	Maximum Quiescent Supply Current			TBD	mA	

1. The MPC909 outputs can drive series or parallel terminated  $50\Omega$  (or  $50\Omega$  to  $V_{CC}/2$ ) transmission lines on the incident edge.

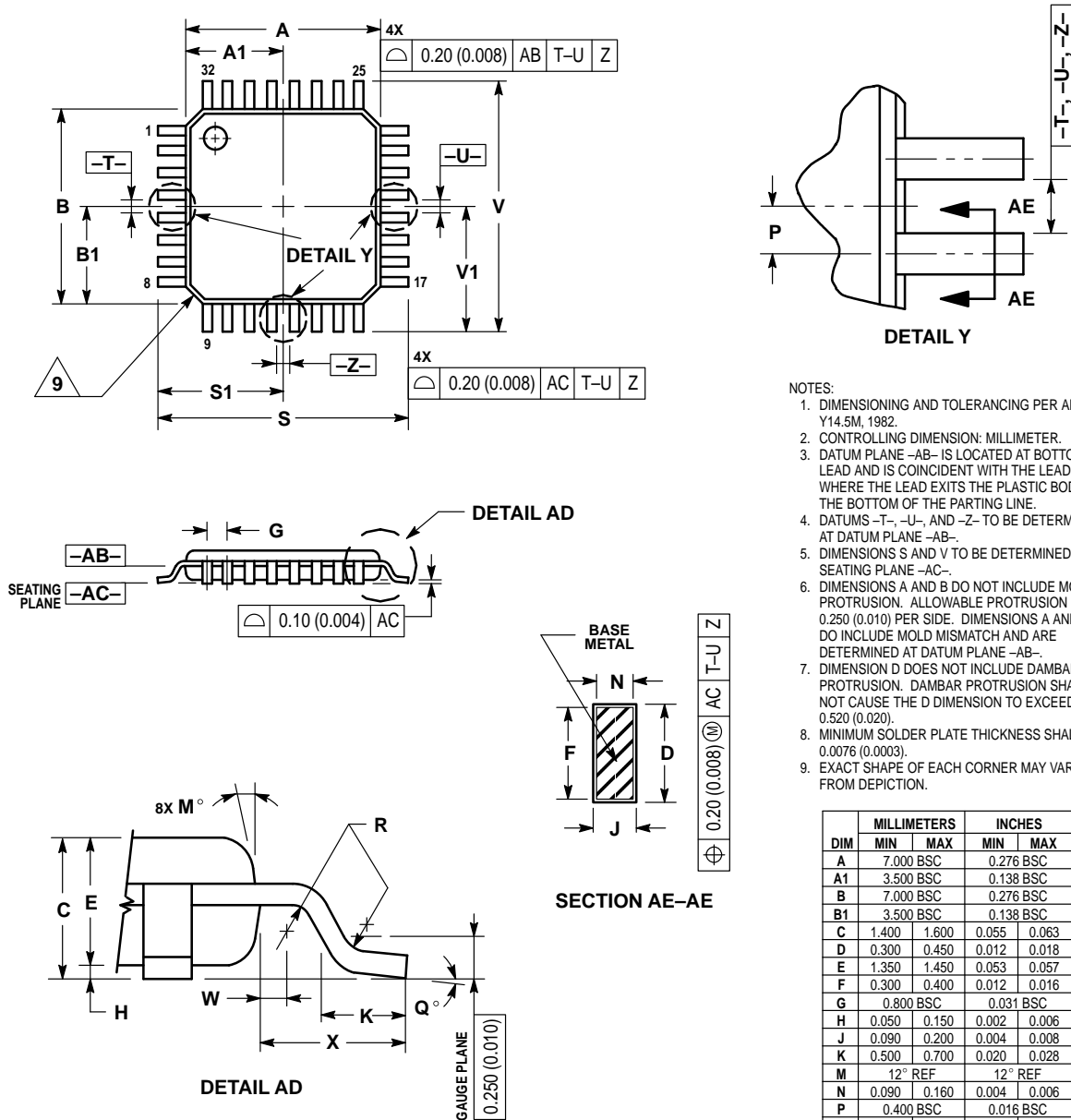
**AC CHARACTERISTICS** ( $T_A = 0^\circ$  to  $70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 5\%$ , or  $2.5\text{V} \pm 5\%$ )

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
$F_{max}$	Maximum Input Frequency			100	MHz	Note 2.
$t_{pd}$	Propagation Delay LVCMOS_CLK to Q OE to Q	1.0 1.0		5.0 8.0	ns	Note 2.
$t_{sk(o)}$	Output-to-Output Skew			250	ps	Note 2.
$t_{pwo}$	Output Pulse Width	45		55	%	Note 2., Measured at $V_{CC}/2$
$t_r, t_f$	Output Rise/Fall Time	0.20		1.0	ns	0.8V to 2.0V


2. Driving  $50\Omega$  transmission lines

OUTLINE DIMENSIONS

FA SUFFIX  
TQFP PACKAGE  
CASE 873A-02  
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
  4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
  5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
  6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
  7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
  8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
  9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

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#### How to reach us:

**USA/EUROPE/Locations Not Listed:** Motorola Literature Distribution;  
P.O. Box 5405, Denver, Colorado 80217. 303-675-2140 or 1-800-441-2447

**JAPAN:** Nippon Motorola Ltd.: SPD, Strategic Planning Office, 4-32-1,  
Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan. 81-3-5487-8488

**Mfax™:** RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609  
– US & Canada ONLY 1-800-774-1848

**ASIA/PACIFIC:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,  
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

**INTERNET:** <http://motorola.com/sps>



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