

MPC2605

Integrated Secondary Cache for PowerPC™ Microprocessor Applications

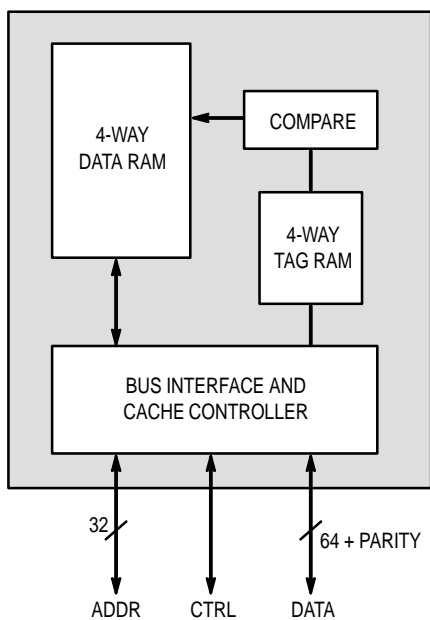
The Secondary Cache Solution For PowerPC Microprocessors:

The MPC2605 is the highest performing secondary cache solution available for use in PowerPC 60x buses. The MPC2605 is a four-way set associative integrated look-aside cache with copy-back or optional write-through capability. An increase in system performance is achieved by integrating the data, tag, host interface, and least recently used (LRU) memory with a cache controller in a single chip.

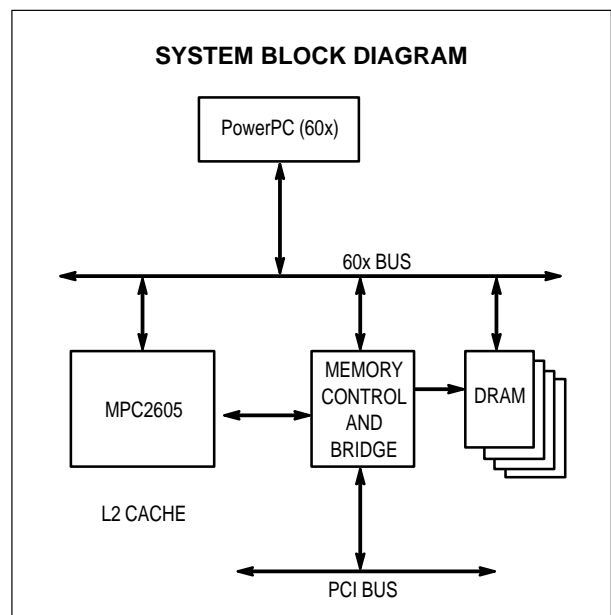
These solutions offer minimum latency and zero wait state burst performance — burst reads occur at 2–1–1–1 clock rates.

The multi-way set associativity feature increases cache hit rates, which makes the cache behave like a direct-mapped cache twice its size. This yields a higher performance system solution at 256KB prices.

MPC2605 BLOCK DIAGRAM



SYSTEM BLOCK DIAGRAM



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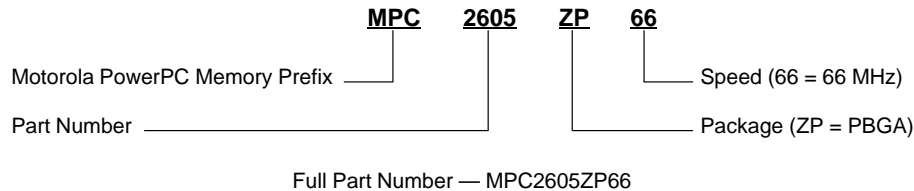
PRODUCTS

The MPC2605 groups together all the functions required to implement a level 2 cache design integrated into one chip, eliminating the need for glue logic.


The MPC2605 is a member of the PowerPC family components.

SUMMARY

- Supply Voltage — 3.3 V
- Speed — 66 MHz
- Burst Read — 2–1–1–1
- Data Bus Size — 64 + Parity
- Write Policy — Copy-Back or Write-Through
- Associativity — 4-Way
- Scan — IEEE 1149.1 JTAG
- Number of Chips for 256KB — 1
- Number of Chips for 512KB — 2
- Number of Chips for 1MB — 4



For additional information call 512-933-SRAM, or your local Motorola sales representative.
FAX (512) 933-6809

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