Advance Information

Field Programmable Analog Array Evaluation Board

MPAA3BRD

FIELD PROGRAMMABLE ANALOG ARRAY EVALUATION BOARD

The MPAA3BRD is an analog circuit design, prototyping, and evaluation tool for the MPAA020 Analog Array. The board contains all the supporting circuitry as well as several options for flexible, fast analog design.

The MPAA3BRD contains the following features:

- Serial interface connector used to easily download an analog design configuration via the MPA1/POD Serial Port Download Cable. The MPAA020 may be configured via the Download Cable or by an optional on–board serial boot PROM
- On–board socket to accept serial boot PROM
- 3 momentary–action push–button switches for RESET, BFR (Boot From ROM), and PWRUP (Power–Up) signals
- Boot status LED's
- On–board 1MHz oscillator plus an on–board option to provide a user–defined external clock source
- Two stereo audio mini jacks for input/output of signals
- An input BNC connector input to an on–board 4–pole, 200kHz Sallen Key anti–aliasing filter. On–board options allow the Sallen Key filter to receive either dc or ac coupled signals
- An output connector receiving the output of an on–board 4–pole, 200kHz Sallen Key filter. On–board options allow the output from the filter to be dc or ac coupled
- Three options to generate Signal Ground:
    1. Use the MPAA020's internal 2.5V reference (referred to as VMR)
    2. Use the on–board 2.5V reference IC
    3. Or use an external user–defined reference voltage
- On–board 5V regulator for connection to a higher voltage unregulated supply
- On–board mini–jack for input from an optional 9V ac to dc wall plug
- Wire–wrap area with two independent supply buses
- Header pins provide access to each pin of the MPAA020 for easy connection of input and output signals. Header pins are configured so that signals may be monitored using low–inductance probes

In addition to the above features, the Evaluation Board contains many user options to provide additional flexibility in design and evaluation of an analog configuration. The options and features are discussed in detail below. Also, this detailed explanation is contained within the MPAA020 User's Manual.

Powering the MPAA 3 Evaluation Board

The Evaluation Board may be powered one of three ways.

Note: To utilize the on–board 5V regulator in 1) and 2) below, a jumper must be installed on the pins of header JP9.

1. Power the board using Banana Plug Connectors, J4 ("PWR") and J5 ("GND"). At least 8V should be applied to power the on–board 5V regulator.
2. Power the board using the DC power supply mini connector, J4. The AC to DC power supply should have an output of 9V DC and a current sourcing capability of 500mA. An example of such a supply can be purchased through Newark (800–4NEWARK), part number 46F5048.
3. By REMOVING the jumper between the pins of header JP9, a 5V supply may be connected to the left pin of header JP9, labeled "+5V", to directly power the on–board circuitry. As with any analog circuit design, the 5V supply should be stable and clean (noise–free) for best performance.

MPAA020 and Headers

Each pin of the MPAA020 is connected to a header pin for signal input/monitoring and evaluation purposes. Various input signal instrumentation that can be connected to the headers may include, but is not limited to arbitrary waveform generators, signal generators, dc supplies, sensor/ transducer output signals, etc. The various output signal instrumentation that can be connected to the headers may include, but is not limited to oscilloscopes, multimeters, network and frequency analyzers, etc. Other voltage–controlled circuitry can be connected to the analog array; however, one must remember that the analog array has limited current sourcing/sinking capability (see MPAA020 data sheet for maximum current sinking and sourcing specifications). In such applications, additional interface circuitry should be considered.

The header pins are labeled to indicate the pins of the MPAA020. JP2 is connected to the digital interface pins of the MPAA020 including the pins that are required to download the configuration data stream for the circuit designed using the EasyAnalog™ Design Software. These pins for the serial data communications are connected to JP3. JP3 is the header to which the Serial Port Download Cable should be attached. The pins of headers JP6, JP7, and JP12 provide probe/ connection points for the analog array's I/O's.

Note: JP2, as labeled, contains a column of +5V (outer column) and Ground (inner column) connections with the digital signal lines connected to the middle column of the header. JP6, JP7, and JP12 contain an inner column/row of Ground–connected pins with the analog array's I/O's being connected to the outer column/row of pins. This configuration is useful for connecting low–inductance probes to the I/O pins of the MPAA020.

Oscillator and User–defined Oscillator Option

The evaluation board contains an on–board 1MHz oscillator to drive the analog array's internal clock when a jumper is installed between the middle pin and the pin labeled "1MHz CLK" of header JP8. However, user–defined clock frequencies ranging from 1kHz to 1MHz may be implemented by installing a jumper between the middle pin and the pin labeled "EXT CLK". of header JP8. The external clock is input through the BNC connector, J1, which is also labeled "EXT CLK".

Analog Array Programming Modes and Op Amp Disable

The MPAA020 contains four bits in its digital interface to select various programming modes. The modes are selected via switch, SW4. The following table describes the modes that may be implemented on the evaluation board:

From the above table, bit M1 should always be high and bit M0 should always be low to configure the analog array. Bit M2 should always be high when configuring the analog array from either the EasyAnalog Design Software and the Download Cable (a jumper must be installed to connect the middle pin and the pin labeled "CABLE" of JP1) or a serial EPROM (a jumper must be installed to connect the middle pin and the pin labeled "ROM" of JP1). Bit M3 is unused and should be set low.

Mode Bits		Description
[M1]	[M0]	Bits M1 and M0 of Switch SW4
1	0	BFR Mode – Boot From ROM, serial data, low pin count EPROM generates own addresses

Mode Bits		Description
[M3]	[M2]	Bits M3 and M2 of Switch SW4
0	1	Use external clock for configuration
0	0	Use MPAA internal clock for configuration (not required for evaluation board use)

In addition to the configuration modes, switch SW4 contains an additional bit, "OP DIS", to disable the op amps and op amp buffers of the analog array. Switch "OP DIS" high to disable the op amps. Upon switching "OP DIS" low, the op amps are enabled.

RESET, BFR (Boot From ROM), and PWRUP (Power–Up) Push Buttons

These buttons have dedicated functionalities as described below:

RESET, SW1

Pushing the RESET button, SW1, clears the MPAA020 configuration memory and begins a configuration sequence, as determined by the programming mode bits, when the RESET button is released.

BFR (Boot From ROM), SW2

Pushing the BFR button, SW2, clears the MPAA020 configuration memory and begins a configuration sequence, as determined by the programming mode bits.

PWRUP (Power–Up), SW3

By holding down the PWRUP button during a configuration sequence, user outputs and inputs are disabled until the button is released. This button has the same effect as "OP DIS" (Op amp disable) of SW4.

PWR ON (Power On), ERR (Error), and END (End of Configuration) LED's

- The PWR ON LED is illuminated when power is supplied to the board.
- The ERR LED is illuminated when, during a configuration sequence, a serial data transmission checksum error has occurred. If a serial data transmission checksum error occurs, download the configuration file again (from the EasyAnalog Design Software and the download pod). If using a serial EPROM and a checksum error occurs, cycle power or press one of the POR, RESET, or BFR buttons to re–load the configuration code from the serial EPROM.
- The END LED turns off upon successful configuration of the analog array. The analog circuit design created using the EasyAnalog Design Software is now fully functional in the MPAA020.

Serial EPROM

An optional serial EPROM, inserted into socket U1, is used to load an analog circuit configuration into the

MPAA020 upon power–up (i.e. without the necessity of using the EasyAnalog Design Software and the Download Cable). Make sure when configuring the MPAA020 from a serial EPROM that a jumper is installed from the middle pin to the pin labeled “ROM” of header JP1.

A recommended device is Motorola’s 8–pin MPA1765 (64K) serial EPROM. The DIP version, MPA1765P, is required for use with the evaluation board.

The Sallen Key Input Filter and AC IN (for input signals)

To demonstrate optional external anti–aliasing filtering of an input signal to the analog array, one of the analog array’s input buffer amplifiers (pins LDX, LDY, and LDZ) is dedicated as an input (using the EasyAnalog Design Software, user must turn on the input buffer and ensure the switch between LDX and LDY is OPEN) from the output of the 4th order 200kHz (3dB point) anti–aliasing Sallen Key input filter. The output of the filter is located at the LDZ pin.

A BNC connector, J7, is provided for the input signal to the anti–aliasing filter. The input signal is referenced to earth ground (GND) as required by some signal generators. All input signals connected to J7 are AC coupled.

If AC coupling of the input signal is not desired, the input signal may be input directly to the anti–aliasing filter by attaching the signal to the top pin of header JP11 (JP11 is also labeled “SIGIN”). The ground connection of the input signal may then be attached to either signal ground (bottom pin of header JP11) or to earth ground. The intention of JP11 is to allow the input signals that are referenced to signal ground to be measured using low inductance probes.

The Sallen Key Output Filter and Output Coupling Options

To demonstrate optional external filtering of the analog array’s output, one of the analog array’s input buffer amplifiers (pins RDX, RDY, and RDZ) is dedicated as an output (using the EasyAnalog Design Software, user must turn on the input buffer and ensure the switch between RDX and RDY is OPEN) from the 4th order 200kHz (3dB point) Sallen Key output filter.

The output of the Sallen Key filter can be AC or DC coupled, as may be desired or required of some instrumentation.

To measure the DC–coupled signal output from the Sallen Key filter, remove all jumpers from headers JP4 and JP5. Measure the DC–coupled signal on the pin of header JP5 labeled “DCOUT”.

To measure the AC–coupled signal output from the Sallen Key filter, install a jumper from the pin labeled “DCOUT” of JP5 to the pin directly above it of JP4 (the left pin of header JP4). Measure the AC–coupled signal on the pin of header JP4 labeled “ACOUT”.

A ground pin (the right pin of header JP5) is available for measuring either the DC or AC coupled signal using low inductance probes.

Stereo Mini Plugs

Perhaps the most specialized feature of the evaluation board is the stereo mini plugs, J9 and J10. These may be used for any stereo (or mono) input signal (e.g. the output of a stereo walkman, CD player, etc.) that requires additional signal conditioning, filtering, etc. For maximum flexibility, J9 and J10 are not hardwired to specific pins of the MPAA020; rather, via headers JP14 and JP15, the signals from J9 and J10 may be connected to any of the pins on headers JP6, JP7, and JP12 via the square–pin–to–square–pin jumper cables supplied with the evaluation board. For each of the headers, JP14 and JP15, ground is connected to the leftmost pin, the left channel input signal is connected to the middle pin, and the right channel input signal is connected to the rightmost pin.

Signal Ground (SGND) Connection Options

There are three options to generating the signal ground for the analog array’s operation:

- Normally, the signal ground for the MPAA020 is 2.5V as generated internally to the MPAA020 and measurable at the pin labeled “VMR” on header JP7. To use the internally generated signal ground, DO NOT install a jumper across header JP11.
- Since the internally generated reference, VMR, does not have high current sourcing capability for applications that require additional instrumentation/circuitry to use the signal ground reference, the evaluation board also contains an on–board 2.5V reference, U2, for such applications. To use the 2.5V reference for signal ground, install a jumper across JP10, AND, via the EasyAnalog Design Software, disable the internally generated reference, VMR.
- For the third option, a user–defined signal ground may be implemented using an external power supply, voltage reference, etc., via the Banana Plug Connector, J6 (also called “SGND”). To implement a user–defined signal ground, connect the desired voltage (between 0V and 5 V) to the SGND Banana Plug Connector, and most importantly, DO NOT install a jumper across header JP11 AND, via the EasyAnalog Design Software, disable the internally generated reference, VMR.

In all three options above, whether the signal ground reference is created via the VMR, the on–board voltage reference, or externally, the Banana Plug Connector, SGND, is available to monitor/connect the signal ground reference to external instrumentation/circuitry.

The Independent Supply Buses, P POS and P NEG, and the Wire–Wrap Area

The Banana Plug Connectors, P POS and P NEG, are connected to the top–most row and bottom–most row, respectively, of the wire wrap area. These P POS and P NEG “power supply buses” are independent of the evaluation board power and ground connections so that any required voltage for circuitry built on the wire–wrap area can be implemented (i.e. split supplies, higher voltage supplies, etc.).

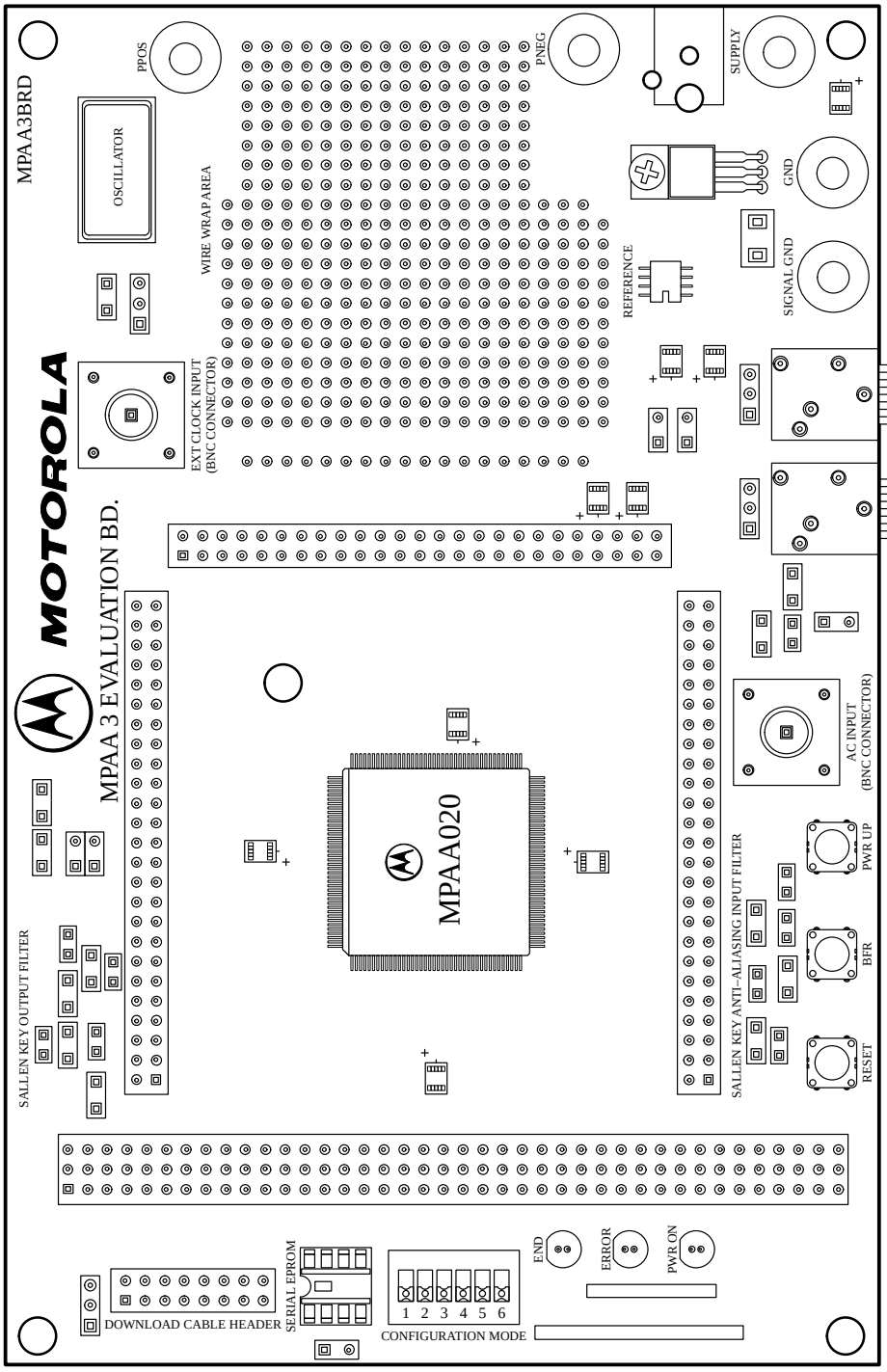

Figure 1. Evaluation Board Physical Layout
(NOT TO SCALE)

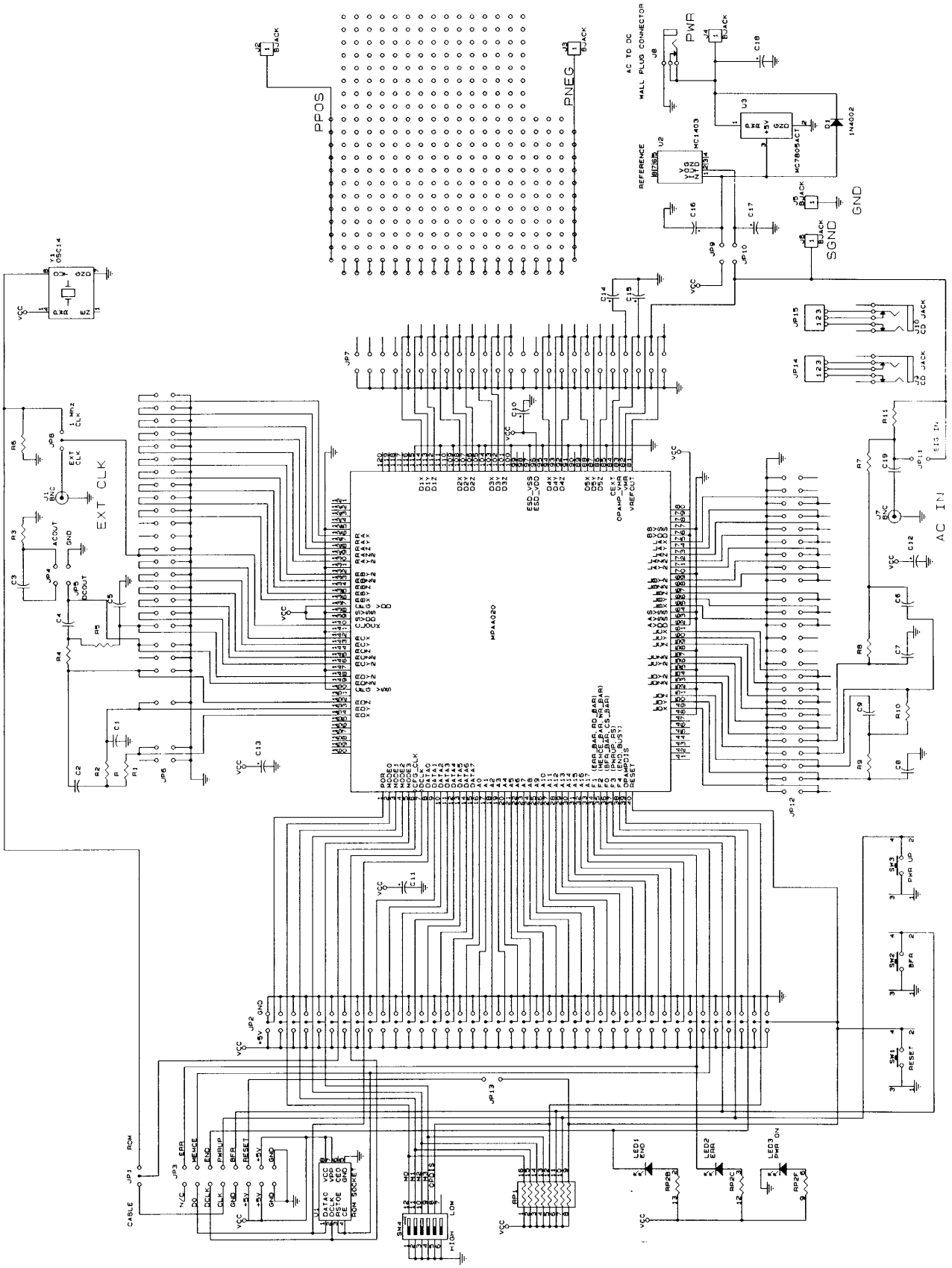

Figure 2. Board Schematic Diagram

The wire–wrap area can be used to implement any circuitry in addition to the circuitry already contained in the evaluation board. The single column header directly left of the wire–wrap area may be used to connect any signals from circuitry on the wire–wrap area to any of the pins on headers JP6, JP7, and JP12 via the square–pin–to–square–pin jumper cables supplied with the evaluation board. For ease of use, each row of the single column header is electrically connected to the corresponding row of the last, leftmost column of the wire wrap area (see Figure 2 Board Schematic on page 5).

Equipment Requirements

The equipment listed below is useful for testing, monitoring, and debugging the circuit designed in the EasyAnalog Design Software.

Computer. A PC computer is required to download the analog circuit configuration (created using the EasyAnalog Design Software) serial data stream via the Download Cable. See the computer requirements listed in the EasyAnalog Design Software instructions.

Power Supply. See **Powering the MPAA 3 Evaluation Board** section on page 1 for power supply requirements and options.

Signal Generator. An arbitrary waveform generator or signal generator is useful for creating input signals to the evaluation board.

Oscilloscope. An oscilloscope is useful for monitoring output signals from the evaluation board.

Multimeter. A digital multimeter can be used to measure various dc signals (e.g. verifying power supply to the board, measuring dc output signals from the evaluation board, etc.)

Spectrum/Network Analyzer. For filter analysis, a spectrum/network analyzer is useful to view the 3dB point(s), passband gain, etc. of a filter design.

Logic Analyzer (optional): For those interested, the serial data stream from the Serial Port Download Cable may be monitored using a logic analyzer. An oscilloscope can also be used for this function.

Miscellaneous Equipment. Additional hardware such as square–pin–to–square–pin jumper cables (supplied with evaluation board), mini–grabber jumper cables, banana plug cables, BNC cables, and, for the wire–wrap area, 22 gauge solid wire (recommended), wire–wrap pins, and solder may also be required/desired.

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