Introducing Motorola's Field Programmable Analog Array

Product Description

The MPAA series of Field Programmable Analog Arrays are a new family of products that have programmable analog building blocks that can be configured to create circuit functions that solve real–world signal processing problems. When used with supporting CAD tools and macro library functions, these products allow the user to address analog circuit design problems with low risk and minimum analog design expertise.

Motorola's first Field Programmable Analog Array, the MPAA020, is an "electronic breadboard" that provides an ideal medium for quickly designing, debugging, and implementing a wide array of analog circuits, thereby reducing development cycle times and enabling the user to meet market introduction timelines.

Additionally, these Analog Arrays, when used with Motorola's MPA series of Field Programmable Gate Arrays, allow the user to implement Field Programmable Mixed–Signal designs using the products and software from each of the individual FPGA technologies. This mixed–signal design capability extends the user's flexibility even further by providing the capability to simultaneously design, debug, and implement both the analog and digital aspects of a system topology

Applications

Motorola's Field Programmable Analog Array can be used in a wide variety of applications. The first analog array products will target industrial motion, process, and power control applications. Additional applications suited for the analog array include communications (low to medium frequency applications), process control (temperature, heating & cooling systems, pressure control, etc.), automotive, and medical instrumentation and measurement systems.

Analog Technology

The technology for Motorola's Field Programmable Analog Array is based upon switched capacitor circuit technology. The MPAA020's switched capacitor circuit topology is designed to be insensitive to parasitic capacitances; consequently arbitrary signal routing is possible with minimal loss in signal integrity due to these parasitics. Also, since the capacitors are integrated on silicon, the capacitance ratios are tightly matched, allowing precise analog signal processing without the need for calibration or feedback. Analog resources in the Motorola's MPAA020 are contained in Configurable Analog Blocks (CAB's) that incorporate a switched–capacitor CMOS Op Amp, Comparator, Capacitor Arrays, CMOS switches and SRAM. Data stored in SRAM control the switches that program various capacitance values (static & dynamic) in the input and feedback signal paths of the Op Amp. Analog functions such as programmable gain stages, adders, subtractors, rectifiers, sample & hold circuits, and first order filters can be implemented in a single cell (CAB). Higher level functions such as biquad filters, PLL's, level detectors, etc. can be implemented using two or more cells.

Architecture

The MPAA020 contains 41 op amps, 100 programmable capacitors and 6864 switches. The switches control circuit connectivity, capacitor values, and other selectable features. The array is structured in a grid that contains 20 CAB's arranged in a 4 x 5 matrix. The programmable CAB's rely on the Configuration Logic in the upper portion of the chip to control the connectivity within the array and functionality in each CAB. Two buses move data from the shift register to the CAB's; the Data Control Bus retrieves and moves the datafrom the shift register and the Transfer Control Bus latches the data into local SRAM. Custom functions can be added to the chip to meet customer or market specific applications. An 8–bit programmable bandgap voltage reference is available to each CAB. Op amps are provided on the chip periphery that can be configured for unity gain buffering or filtering—e.g. anti–aliasing or smoothing filters (external R's & C's required). Configuring an analog design within the array is performed by downloading 6K bits of data via RS232 communications from a PC or EPROM. The data stream contains information to configure the individual cells, the cell interconnections, internal bandgap voltage reference, and I/O's. During this configuration download process, all cells are placed in a powerdown mode.

MPAA020 Performance

A summary of the MPAA020's performance features are listed in the following table. The MPAA020's circuit topology provides advantages relative to chip area, pin count, and rail–to–rail voltage swing with improvements being made to Signal to Noise Ratio and Signal Bandwidth in Motorola's new family (MPAA1xx) of arrays which will be introduced next year. The MPAA1xx arrays will incorporate a zoned array architecture, operate in a differential mode and have on–board tuning. A higher voltage family is also planned which will operate in applications with voltages greater than 10 volts.

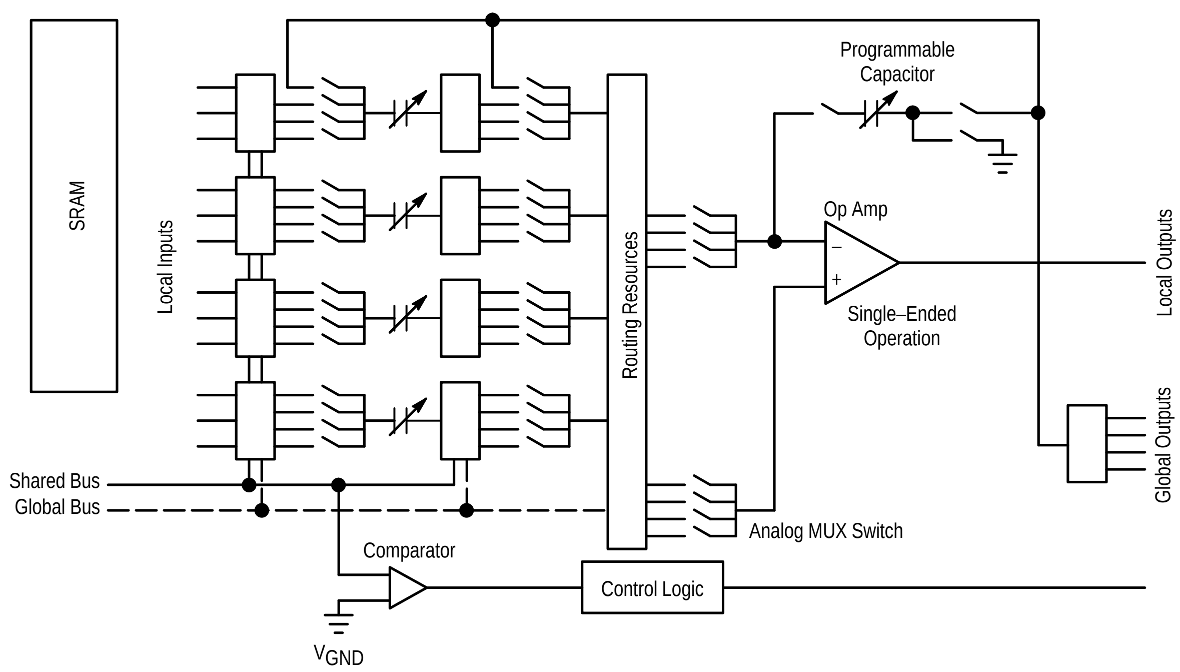

Figure 1. MPAA020 Configurable Analog Block (CAB)

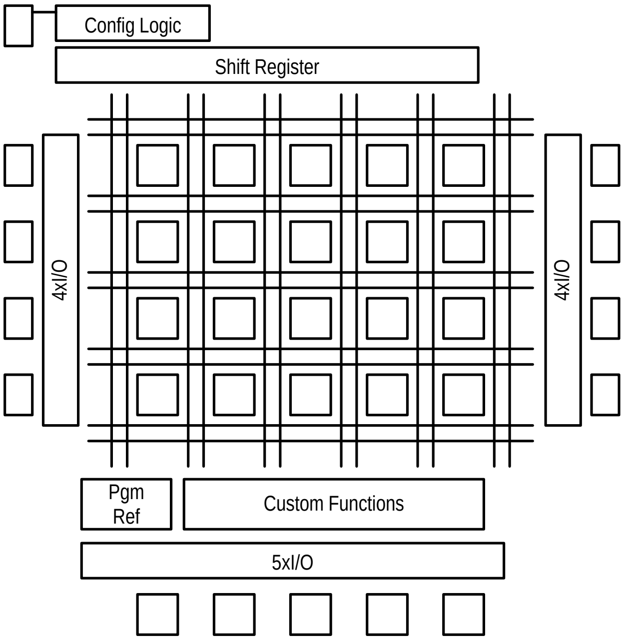

Figure 2. MPAA020 Block Diagram

Partial Macro Library – Analog Functions

Single Cell Macro Functions	Two Cell Macro Functions
Gain Stages (max=20; min=1/20)	Low Q Biquad Filter (Hi or Lo Pass) – 2 Cells
Sum & Diff Amps (3 Weight Inputs)	Low Q Biquad Filter (Notch, Band-Pass) – 3 Cells
Sample & Hold	High Q Biquad Filter (Hi or Lo Pass) – 2 Cells
Track & Hold	High Q Biquad Filter (Notch, Band-Pass) – 3 Cells
Integrator	Maximum Corner Frequency=T/10
N–Path Integrator	Minimum Corner Frequency=T/100
Differentiator	Limiter
Half Wave Rectifier	Interpolator
Full Wave Rectifier	Schmidt Trigger
LPF Rectifier	Voltage Controlled Oscillator
Cosine Filter	Sine Wave Oscillator
Decimator	Square Wave Oscillator
Bi–Linear Filter	Triangle Wave Oscillator

Performance Specifications

Specification		Typical Value
System Master Clock Frequency (**clock**) Internal Sampling Clock Rate		TBD 1 MHz (max.)
Maximum Signal Frequency	Recommended – Nyquist	200 kHz 500 kHz
Input Signal Range		0.5 to (Vdd – 0.5)
Analog Output Drive		100 pF (max.) 1 kohm (min.)
DC Offset		< 10 mV
Harmonic Distortion	1 kHz 200 kHz	< 0.1% < 0.5%
Differential Non–Linearity		< 0.15 LSB
Integral Non–Linearity		< 0.24 LSB
Slew Rate		10 V/µs
Signal to Noise Ratio (SNR)		> 60 dB
Power Supply Rejection Ration (PSRR)		TBD
Power Dissipation (max.) Each cell individually selectable		200 mW (10 mW/cell)
Operating Temperature Range		–40 to + 85°C

Configuring an Analog Circuit Design in the MPAA020:

The configuration logic is responsible for loading external configuration data into the device. Two modes exist: Micro Mode and Boot From ROM Mode (BFR). Micro Mode allows the device to be configured from a microprocessor, or similar system, through a conventional peripheral interface. BFR Mode supports three sub–modes: BFR using an internal address generator with a byte wide data format; 2) BFR using an external address generator with a serial data format; 3) BFR using an external address generator with a byte wide data format.

Design Tools for the Analog Array:

Motorola's MPAA layout tools are architecture–independent by design. Software routing algorithms and chip design adjustments were made to improve performance, increase density and reduce parasitics—i.e. noise, charge injection & crosstalk. The EasyAnalog™ Design Software tool is a user–friendly, PC–based (Windows '95/NT compatible) manual place–and–route tool. The EasyAnalog Design Software allows the user to select analog macros (e.g. gain stage, biquad filter, summing amplifier, etc.) that reside in a library. The EasyAnalog Design Software guides the user through the design and selection of the functional performance specifications (e.g. gain for a gain–stage, frequency for an oscillator and corner frequency for a filter, etc.) for each macro to meet the applications design requirements. All macros that are selected can be manually placed and routed using point–and–click operations. During circuit wiring, dynamic validity checks are performed so that legitimate connection points are highlighted as the cursor is moved over them. The circuit wiring is "correct–by –construction", i.e. when a wire is placed, it is routed, providing immediate feedback to the user as resources are consumed. An algorithm within the macro cell converts the user–specified specifications into the required timing, capacitor and switch settings. Since the user can enter arbitrary parameter values, a routine within the EasyAnalog Design Software informs the user of the actual parameter settings due to finite levels of capacitor quantization. Once the design is complete and the wiring and parameter adjustments are finalized, the software allows the user to download the "configuration" bitstream (data stream containing all the chip's switch settings: static; dynamic; signal) to the chip via the PC's RS232 serial communications port. Once the bitstream is downloaded, the MPAA020 will immediately begin to function as designed. A signal generator and oscilloscope can be used to verify the behavior of the circuit. For each macro within the library, all possible variations of user inputs have been evaluated and detailed performance models constructed. This information provides instantaneous feedback to the user on any changes in operating characteristics and/or device performance based upon user–selected specifications. Evaluation releases of the software will be available on the World Wide Web so users can explore the capabilities of the device. The user can also obtain a demonstration kit which contains the software, an evaluation board, serial download cable for downloading analog design configurations from a PC, and supporting documentation.

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