Designer's™ Data Sheet

Medium Power Surface Mount Products

TMOS P-Channel Field Effect Transistor

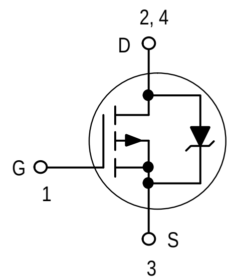
MMFT5P03HD

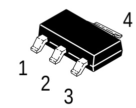
Motorola Preferred Device

TMOS MEDIUM POWER FET
5.2 AMPERES
30 VOLTS
$R_{DS(on)}$ = 100 mΩ

MMFT5P03HD is an advanced power MOSFET which utilizes Motorola's High Cell Density HDTMOS process. This miniature surface mount MOSFET features ultra low $R_{DS(on)}$ and true logic level performance. It is capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MMFT5P03HD devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SOT–223 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified





CASE 318E–04, Style 3
TO–261AA

DEVICE MARKING	ORDERING INFORMATION			
5P03H	**Device**	**Reel Size**	**Tape Width**	**Quantity**
	MMFT5P03HDT3	13″	12 mm embossed tape	4000 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)
Negative sign for P–Channel devices omitted for clarity

Rating		Symbol	Max	Unit
Drain–to–Source Voltage		V_{DSS}	30	V
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)		V_{DGR}	30	V
Gate–to–Source Voltage — Continuous		V_{GS}	± 20	V
1 inch SQ. FR–4 or G–10 PCB 10 seconds	Thermal Resistance — Junction to Ambient Total Power Dissipation @ T_A = 25°C Linear Derating Factor Drain Current — Continuous @ T_A = 25°C Continuous @ T_A = 70°C Pulsed Drain Current (1)	R_{THJA} P_D I_D I_D I_{DM}	40 3.13 25 5.2 4.1 26	°C/W Watts mW/°C A A A
Minimum FR–4 or G–10 PCB 10 seconds	Thermal Resistance — Junction to Ambient Total Power Dissipation @ T_A = 25°C Linear Derating Factor Drain Current — Continuous @ T_A = 25°C Continuous @ T_A = 70°C Pulsed Drain Current (1)	R_{THJA} P_D I_D I_D I_{DM}	80 1.56 12.5 3.7 2.9 19	°C/W Watts mW/°C A A A
Operating and Storage Temperature Range		T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 30 Vdc, V_{GS} = 10 Vdc, Peak I_L = 12 Apk, L = 3.5 mH, R_G = 25 Ω)		E_{AS}	250	mJ

(1) Repetitive rating; pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (1) (3) (V_{GS} = 0 Vdc, I_D = 0.25 mAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 30 —	 — 28	 — —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 24 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 24 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 — —	 1.0 25	µAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (Cpk ≥ 2.0) (1) (3) (V_{DS} = V_{GS}, I_D = 0.25 mAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 —	 1.75 3.5	 3.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (1) (3) (V_{GS} = 10 Vdc, I_D = 5.2 Adc) (V_{GS} = 4.5 Vdc, I_D = 2.6 Adc)		$R_{DS(on)}$	 — —	 79 119	 100 150	mΩ
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 2.0 Adc) (1)		g_{FS}	2.0	4.0	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	475	950	pF
Output Capacitance		C_{oss}	—	220	440	
Transfer Capacitance		C_{rss}	—	70	140	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 4.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω) (1)	$t_{d(on)}$	—	12	24	ns
Rise Time		t_r	—	24	48	
Turn–Off Delay Time		$t_{d(off)}$	—	47	94	
Fall Time		t_f	—	46	92	
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω) (1)	$t_{d(on)}$	—	19	38	
Rise Time		t_r	—	55	110	
Turn–Off Delay Time		$t_{d(off)}$	—	30	60	
Fall Time		t_f	—	40	80	
Gate Charge	(V_{DS} = 24 Vdc, I_D = 4.0 Adc, V_{GS} = 10 Vdc) (1)	Q_T	—	17	24	nC
		Q_1	—	1.7	—	
		Q_2	—	6.3	—	
		Q_3	—	4.6	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(1)	(I_S = 4.0 Adc, V_{GS} = 0 Vdc) (1) (I_S = 4.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	1.1 0.89	1.5 —	Vdc
Reverse Recovery Time	(I_S = 4.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/µs) (1)	t_{rr}	—	39	—	ns
		t_a	—	20	—	
		t_b	—	19	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.042	—	µC

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{\text{3 x SIGMA}} \right|$
(4) Repetitive rating; pulse width limited by maximum junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

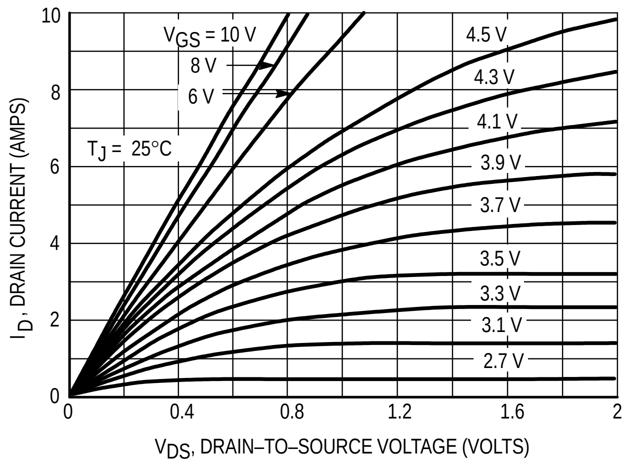


Figure 1. On–Region Characteristics

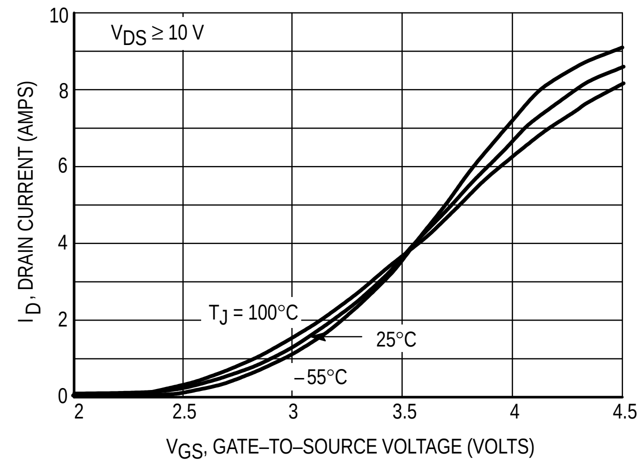


Figure 2. Transfer Characteristics

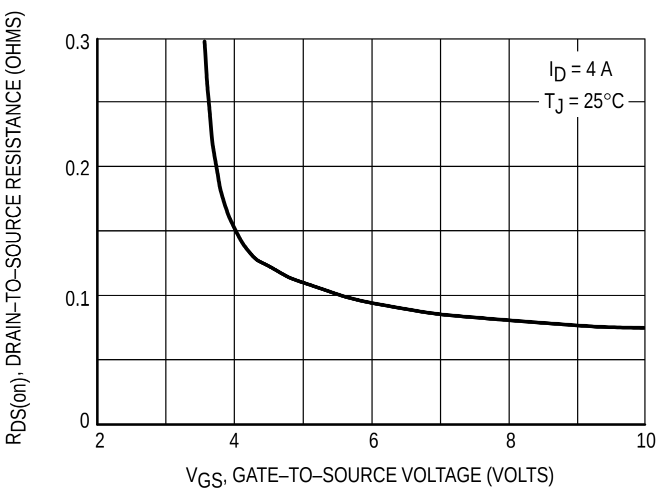


Figure 3. On–Resistance versus Gate–To–Source Voltage

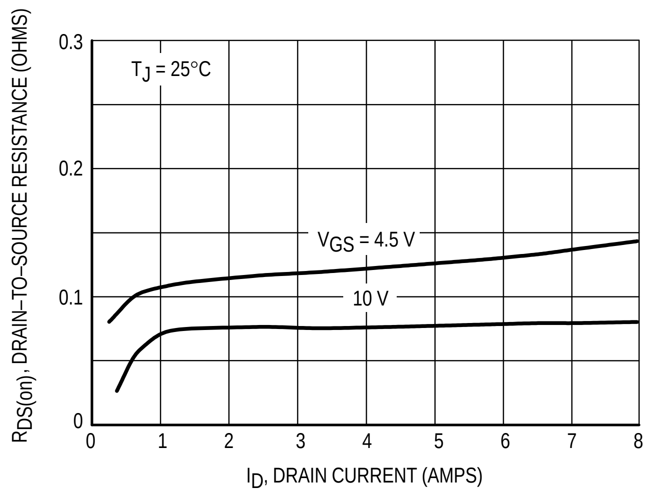


Figure 4. On–Resistance versus Drain Current and Gate Voltage

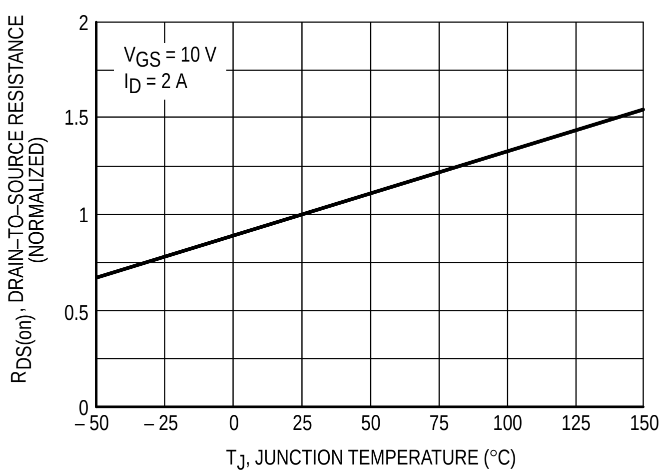


Figure 5. On–Resistance Variation with Temperature

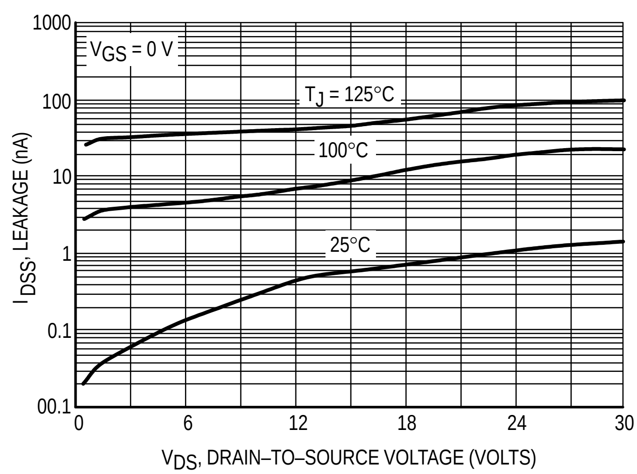


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \ln\ [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G\ C_{iss}\ \ln\ (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

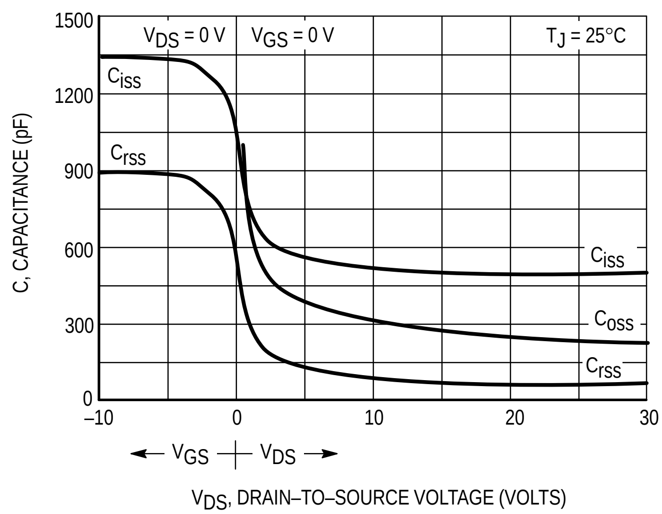


Figure 7. Capacitance Variation

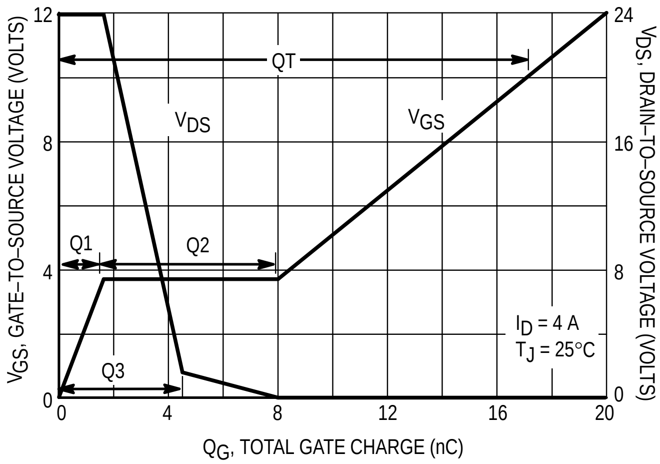


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

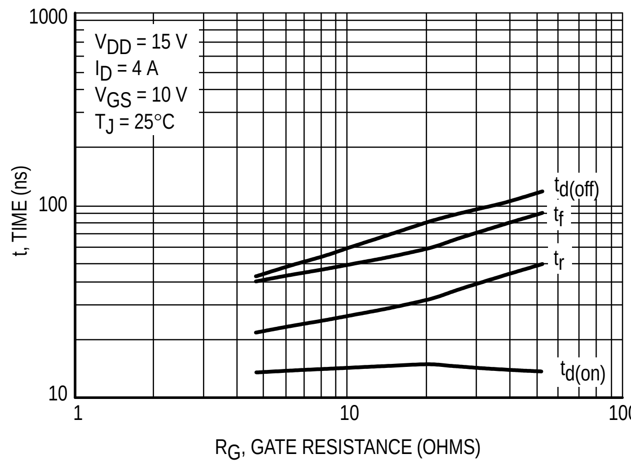


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

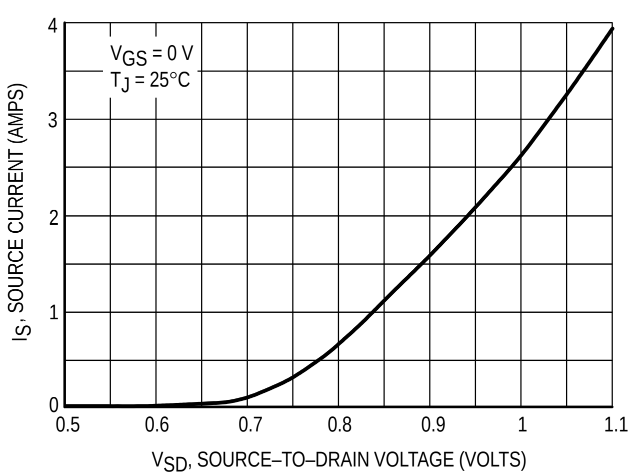


Figure 10. Diode Forward Voltage versus Current

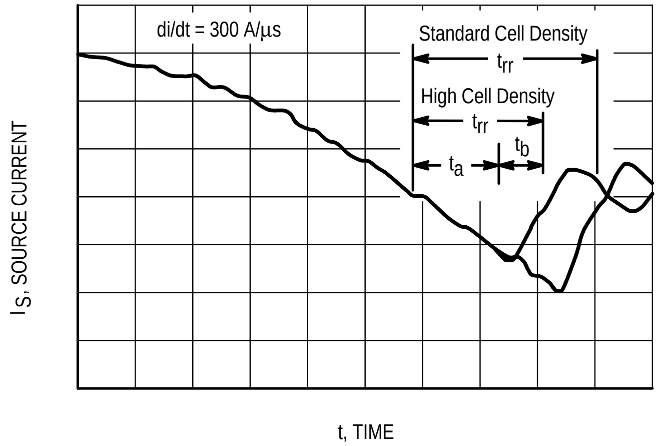


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} – T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

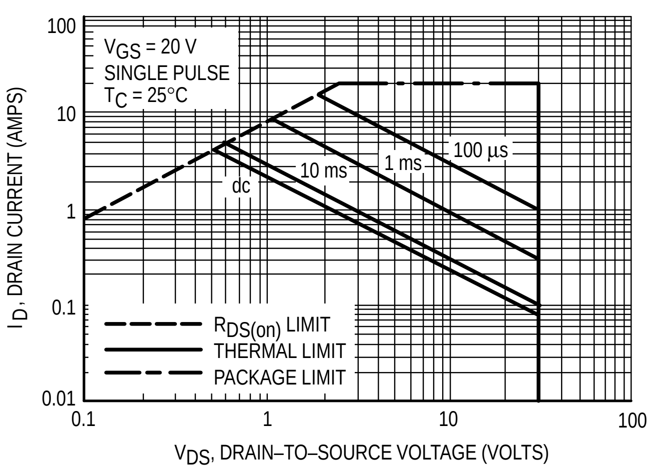


Figure 12. Maximum Rated Forward Biased Safe Operating Area

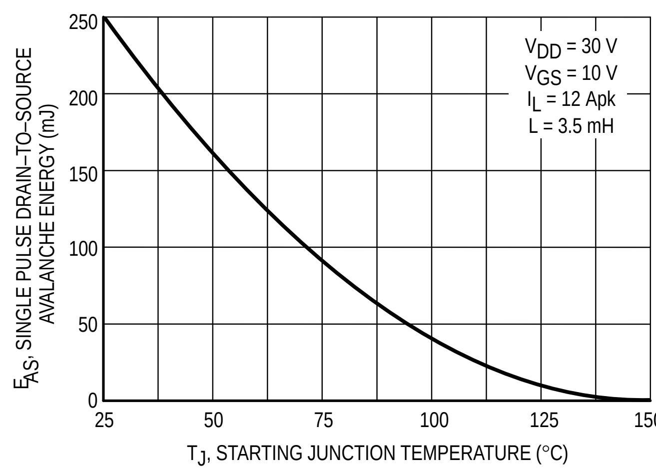


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

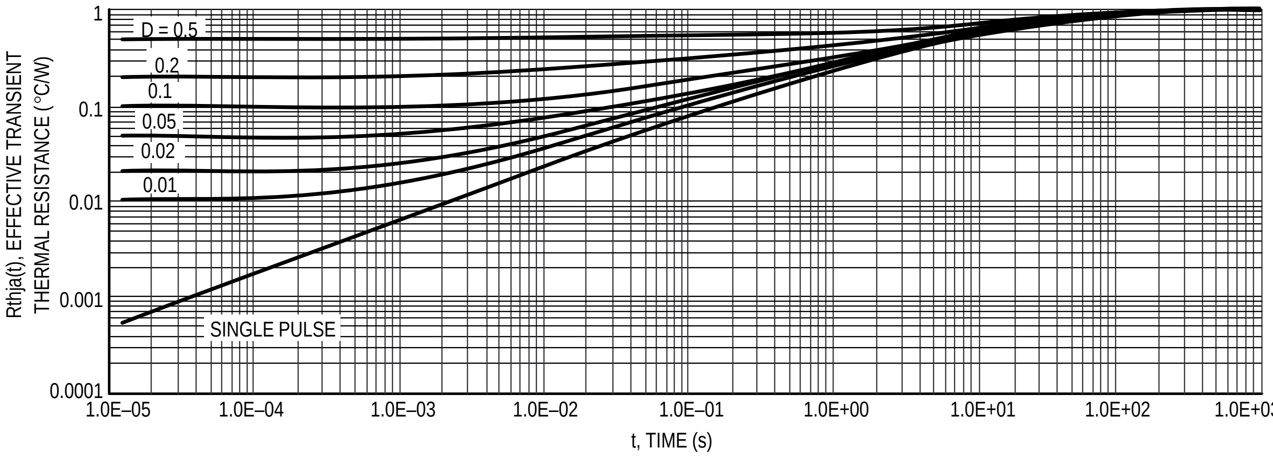


Figure 14. Thermal Response

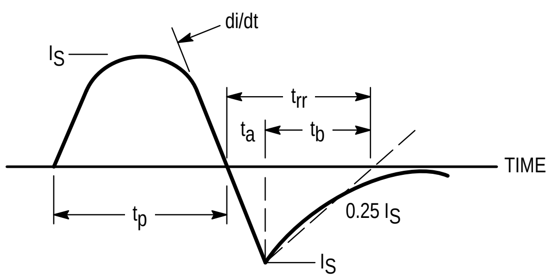
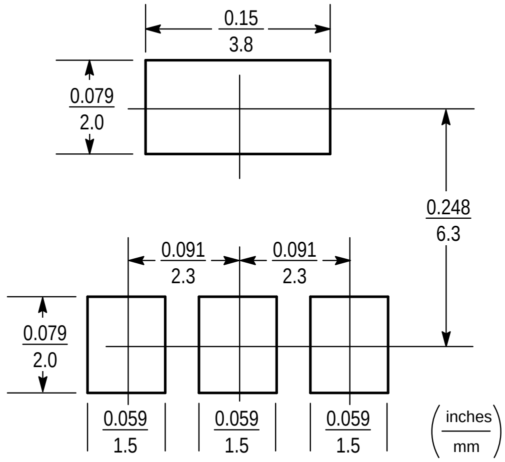


Figure 15. Diode Reverse Recovery Waveform

INFORMATION FOR USING THE SOT–223 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–223

SOT–223 POWER DISSIPATION

The power dissipation of the SOT–223 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–223 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 3.13 watts.

$$P_D = \frac{150°C - 25°C}{40°C/W} = 3.13 \text{ watts}$$

The 40°C/W for the SOT–223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 3.13 watts. There are other alternatives to achieving higher power dissipation from the SOT–223 package. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology.

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

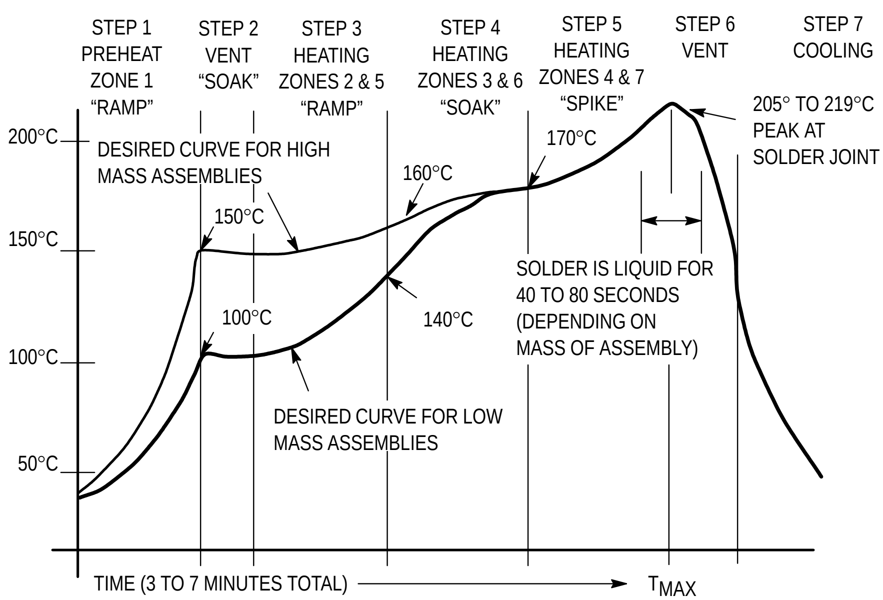
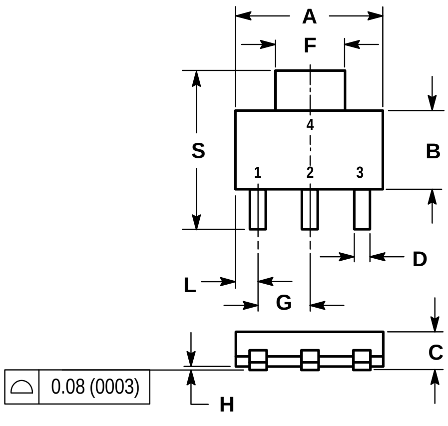
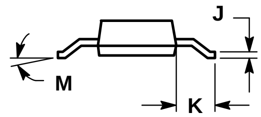


Figure 16. Typical Solder Heating Profile

PACKAGE DIMENSIONS



STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

CASE 318E–04
ISSUE H

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