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SEMICONDUCTOR TECHNICAL DATA

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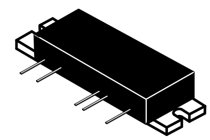
The RF Line
UHF Power Amplifiers

MHW803-2

2 W, 806 to 905 MHz
UHF POWER
AMPLIFIERS



CASE 301E–04, STYLE 1

Capable of wide power range control as encountered in portable cellular radio applications (30 dB typical).

- MHW803–2 806 – 870 MHz
- Specified 7.5 Volt Characteristics
  RF Input Power = 1 mW (0 dBm)
  RF Output Power = 2 Watts
  Minimum Gain ($V_{Control}$ = 4 V) = 33 dB
  Harmonics = – 45 dBc Max @ 2 f_o
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 2,3,4)	$V_{S1,2,3}$	10	Vdc
DC Control Voltage (Pin 1)	V_{Cont}	4	Vdc
RF Input Power	P_{in}	3	mW
RF Output Power (V_{S1} = V_{S2} = V_{S3} = 10 V)	P_{out}	3	W
Operating Case Temperature Range	T_C	– 30 to +100	°C
Storage Temperature Range	T_{stg}	– 30 to +100	°C

ELECTRICAL CHARACTERISTICS V_{S1} = V_{S2} = V_{S3} = 7.5 Vdc, (Pins 2,3,4), T_C = 25°C, 50 Ω System

Characteristic	Symbol	Min	Max	Unit
Frequency Range	—	806	870	MHz
Control Voltage (P_{out} = 2 W, P_{in} = 1 mW) (1)	V_{Cont}	0	4	Vdc
Quiescent Current (V_{S1}, Pin 2 = 7.5 Vdc) (2)	$I_{S1(q)}$	—	65	mA
Power Gain (P_{out} = 2 W, V_{Cont} = 4 Vdc)	G_p	33	—	dB
Efficiency (P_{out} = 2 W, P_{in} = 1 mW) (1)	η	37	—	%
Harmonics (P_{out} = 2 W) (1) 2 f_o (P_{in} = 1 mW) 3 f_o	—	—	– 45 – 55	dBc
Input VSWR (P_{out} = 2 W, P_{in} = 1 mW), 50 Ω Ref. (1)	—	—	2.0:1	—
Noise power 30 kHz Bandwidth, 45 MHz above fo (P_{out} = 2 W (1) T_C = + 25°C (P_{in} = 1 mW) T_C = +100°C	— —	— —	– 85 – 82	dBm dBm
Load Mismatch (V_{S1} = V_{S2} = V_{S3} = 10 Vdc) VSWR = 10:1, P_{out} = 3 W, P_{in} = 3 mW (1)		No Degradation in Power Output		
Stability (P_{in} = 0.5 – 2 mW, V_{S1} = V_{S2} = V_{S3} = 6 – 9 Vdc) P_{out} between 0 mW and 2 W (1) Load VSWR = 6:1, Source VSWR = 3:1)		All spurious outputs more than 60 dB below desired signal		

NOTES:
1. Adjust V_{cont} for specified P_{out}.
2. V_{Cont} = 0 Vdc.

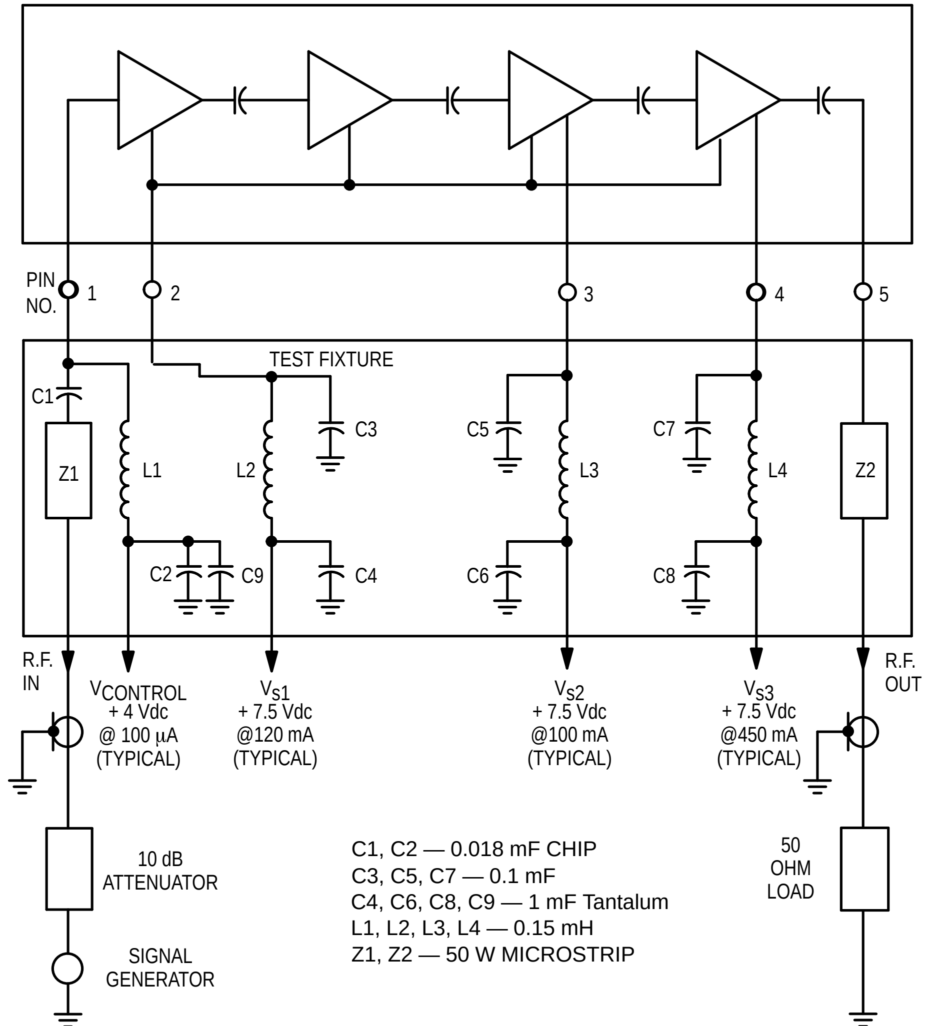


Figure 1. Power Module Test System Block Diagram

TYPICAL CHARACTERISTICS

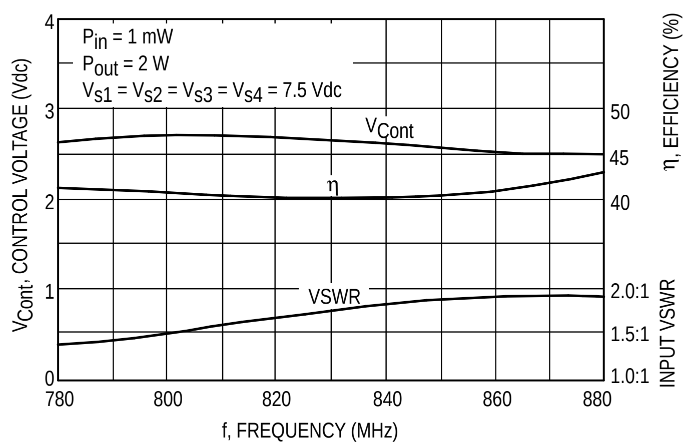


Figure 2. Control Voltage, Efficiency and VSWR versus Frequency

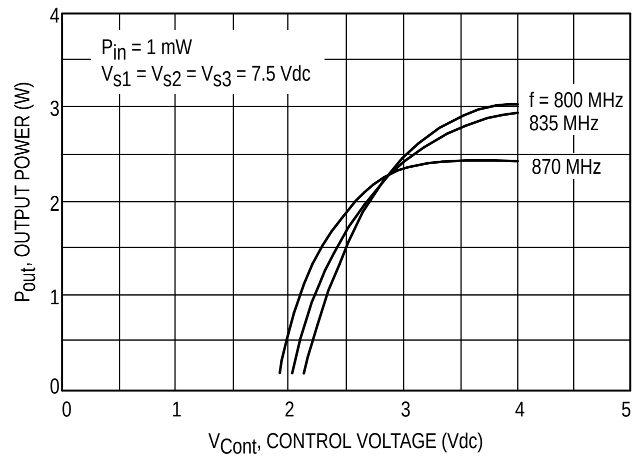


Figure 3. Output Power versus Control Voltage

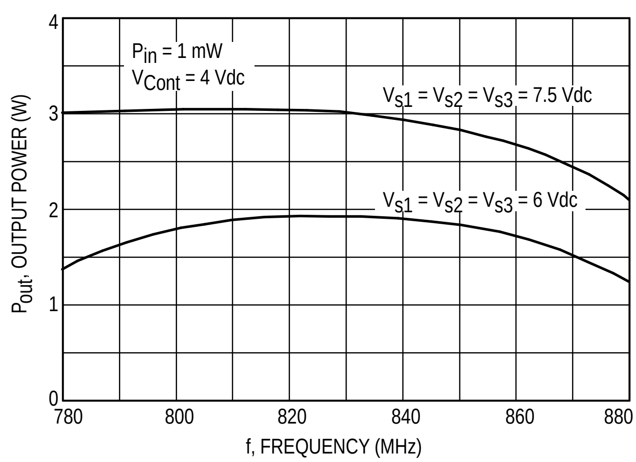


Figure 4. Output Power versus Frequency

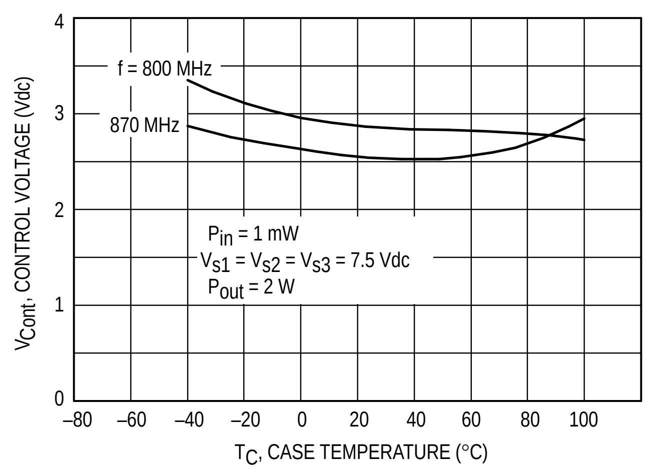


Figure 5. Control Voltage versus Case Temperature

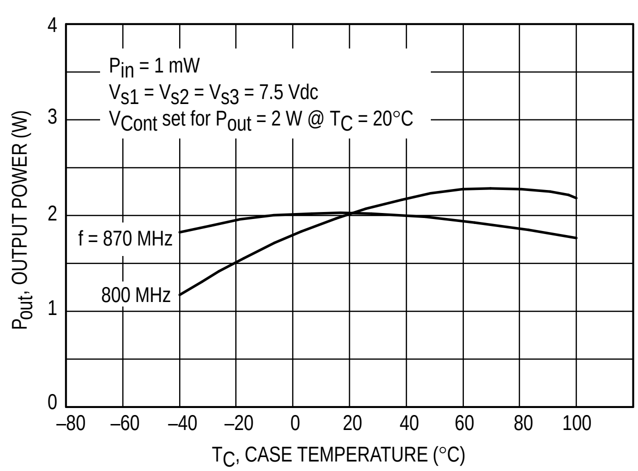


Figure 6. Output Power versus Case Temperature

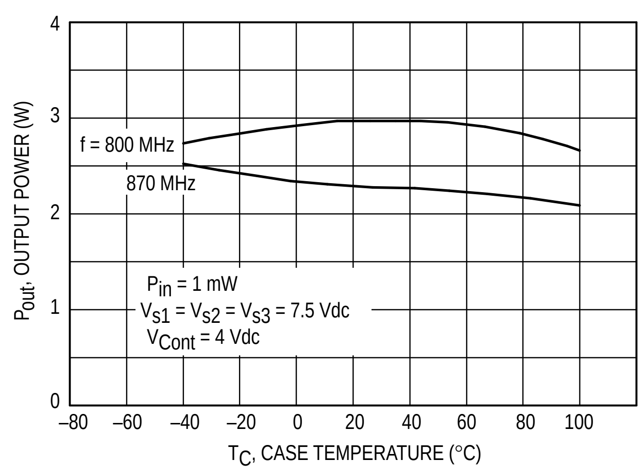


Figure 7. Output Power versus Case Temperature at Maximum Control Voltage

APPLICATIONS INFORMATION

NOMINAL OPERATION

All electrical specifications are based on the nominal conditions of $V_{S1} = V_{S2} = V_{S3} = 7.5$ Vdc (Pins 2, 3, 4) and P_{out} equal to 2 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100°C case operating temperature is 165°C. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use have been made with the factory representative.

GAIN CONTROL

The module output should be limited to 2 watts. The preferred method of power output control is to fix $V_{S1} = V_{S2} = V_{S3} = 7.5$ Vdc (Pins 2, 3, 4), P_{in} (Pin 1) at 1 mW, and vary V_{Cont} (Pin 1) voltage.

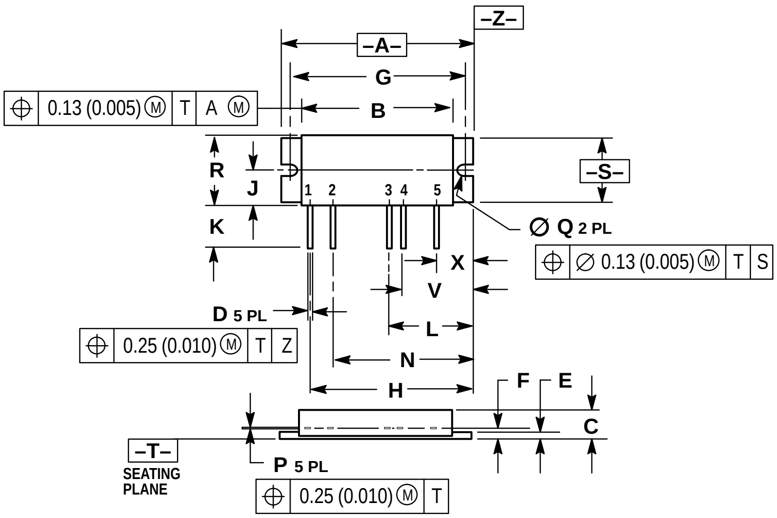
DECOUPLING

Due to the high gain of the three stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3 and 4 are internally bypassed with a 0.018 µF chip capacitor which is effective for frequencies from 5 MHz through 905 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in Figure 1 are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR.

LOAD MISMATCH

During final test, each module is load mismatch tested in a fixture having the identical decoupling networks described in Figure 1. Electrical conditions are $V_{S1} = V_{S2} = V_{S3}$ equal to 10 Vdc, VSWR equal to 10:1, and output power equal to 3 watts.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.760	1.780	44.71	45.21
B	1.370	1.390	34.80	35.30
C	0.245	0.265	6.23	6.73
D	0.018	0.022	0.46	0.55
E	0.080	0.100	2.04	2.54
F	0.130 BSC		3.30 BSC	
G	1.650 BSC		41.91 BSC	
H	1.485 BSC		37.72 BSC	
J	0.267	0.278	6.79	7.06
K	0.230	0.300	5.85	7.62
L	0.785 BSC		19.94 BSC	
N	1.285 BSC		32.64 BSC	
P	0.008	0.012	0.21	0.30
Q	0.120	0.130	3.05	3.30
R	0.535	0.555	13.59	14.09
S	0.445	0.465	11.31	11.81
V	0.685 BSC		17.40 BSC	
X	0.385 BSC		9.78 BSC	

STYLE 1:
PIN 1. RF INPUT/V CONT
2. VS1
3. VS2
4. VS3
5. RF OUTPUT
CASE: GROUND

CASE 301E–04
ISSUE F

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