Product Preview

SMARTDISCRETES™ Internally Clamped, N-Channel IGBT

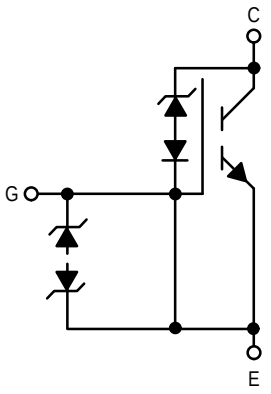
MGP20N14CL

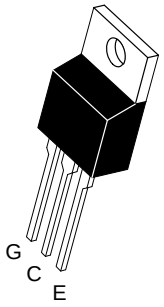
20 AMPERES
VOLTAGE CLAMPED
N–CHANNEL IGBT
$V_{ce(on)}$ = 1.9 VOLTS
135 VOLTS (CLAMPED)

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate–Collector overvoltage protection from SMARTDISCRETES™ monolithic circuitry for usage as an **Ignition Coil Driver**.

- Temperature Compensated Gate–Drain Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessors
- Low Saturation Voltage
- High Pulsed Current Capability

TMOS®





CASE 221A–06, Style 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	CLAMPED	Vdc
Collector–Gate Voltage	V_{CGR}	CLAMPED	Vdc
Gate–Emitter Voltage	V_{GE}	CLAMPED	Vdc
Collector Current — Continuous @ T_C = 25°C — Single Pulsed (t_p = ±10 μs)	I_C I_{CM}	20 60	Adc Apk
Total Power Dissipation @ T_C = 25°C (TO–220) Derate Above 25°C	P_D	150 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Collector–Emitter Avalanche Energy @ Starting T_J = 25°C (V_{CC} = 80 V, V_{GE} = 5 V, Peak I_L = 10 A, L = 10 mH)	E_{AS}	500	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case – (TO–220) — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

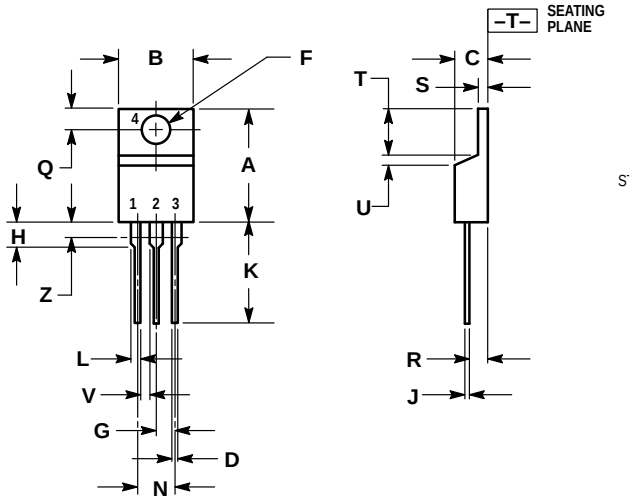
REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Clamp Voltage (I_{Clamp} = 10 mA, T_J = –40 to 150°C)		B_{VCES}	135			Vdc
Zero Gate Voltage Collector Current (V_{CE} = 100 V, V_{GE} = 0 V) (V_{CE} = 100 V, V_{GE} = 0 V, T_J = 150°C)		I_{CES}	— —	— —	10 100	μA
Gate–Emitter Clamp Voltage (I_G = 1 mA)		B_{VGES}	10			Vdc
Gate–Emitter Leakage Current (V_{GE} = ±5 V, V_{CE} = 0 V)		I_{GES}	—	—	1.0	μA
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1 mA) Threshold Temperature Coefficient (Negative)		$V_{CE(th)}$	1.0	1.5 4.4	2.0	V mV/°C
Collector–Emitter On–Voltage (V_{GE} = 5 V, I_C = 10 A) (V_{GE} = 5 V, I_C = 10 Adc, T_J = 175°C)		$V_{CE(on)}$	— —		1.9 1.8	V
Forward Transconductance (V_{CE} > 15 V, I_C = 10 A)		g_{fs}	8.0	15	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	430	600	pF
Output Capacitance		C_{oss}	—	182	250	
Transfer Capacitance		C_{rss}	—	48	100	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 68 V, I_C = 20 A, V_{GE} = 5 V, R_G = 9.1 Ω)	$t_{d(on)}$	—	TBD	TBD	ns
Rise Time		t_r	—	TBD	TBD	
Turn–Off Delay Time		$t_{d(off)}$	—	TBD	TBD	
Fall Time		t_f	—	TBD	TBD	
Total Gate Charge	(V_{CC} = 108 V, I_C = 20 A, V_{GE} = 5 V)	Q_g	—	14	20	nC
Gate–Emitter Charge		Q_{gs}	—	3.0	—	
Gate–Collector Charge		Q_{gd}	—	6.0	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

PACKAGE DIMENSIONS



STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A–06
ISSUE Y

How to reach us:

USA / EUROPE / Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609

INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298