

# SMALLBLOCK™

## Low Voltage Bias Stabilizer

- Maintains Stable Bias Current in Various Discrete Bipolar Junction and Field Effect Transistors
- Provides Stable Bias Using a Single Component Without Use of Emitter Ballast and Bypass Components
- Operates Over a Wide Range of Supply Voltages Down to 1.8 Vdc
- Reduces Bias Current Variation Due to Temperature and Unit-to-Unit Parametric Changes
- Consumes < 0.5 mW at  $V_{CC} = 2.75$  V

This device provides a reference voltage and acts as a DC feedback element around an external discrete, NPN BJT or N-Channel FET. It allows the external transistor to have its emitter/source directly grounded and still operate with a stable collector/drain DC current. It is primarily intended to stabilize the bias of discrete RF stages operating from a low voltage regulated supply, but can also be used to stabilize the bias current of any linear stage in order to eliminate emitter/source bypassing and achieve tighter bias regulation over temperature and unit variations. This device is intended to replace a circuit of three to six discrete components and is available in a SOT-143 package.

The combination of low supply voltage, low quiescent current drain, and small package make it ideal for portable communications applications such as:

- Cellular Telephones
- Pagers
- PCN/PCS Portables
- PCMCIA RF Modems
- Cordless Phones
- Broadband Transceivers and Other Portable Wireless Products

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	15	Vdc
Ambient Operating Temperature Range	$T_A$	-40 to +85	°C
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Junction Temperature	$T_J$	150	°C
Collector Emitter Voltage (Q2)	$V_{CEO}$	-15	V

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Power Dissipation (FR-5 PCB of 1" × 0.75" × 0.062", $T_A = 25^\circ\text{C}$ ) Derate above 25°C	$P_D$	225	mW
		1.8	mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	°C/W

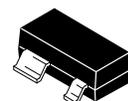
### DEVICE MARKING

MDC5000T1 = E5

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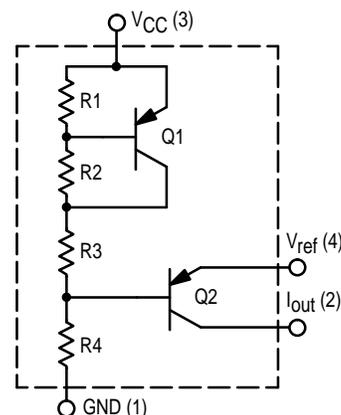
**MDC5000T1**

SILICON  
SMALLBLOCK™  
INTEGRATED CIRCUIT



CASE 318A-05, Style 9  
SOT-143

### INTERNAL CIRCUIT DIAGRAM



**MDC5000T1****ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Supply Voltage	$V_{CC}$	1.8	2.75	10	Volts
Power Supply Current ( $V_{CC} = 2.75\text{ V}$ ) $V_{ref}$ , $I_{out}$ are unterminated See Figure 8	$I_{CC}$	—	110	200	$\mu\text{A}$
Q2 Collector Emitter Breakdown Voltage ( $I_{C2} = 10\ \mu\text{A}$ , $I_{B2} = 0$ )	$V_{(BR)CEO2}$	-15			Volts
Reference Voltage ( $V_{CC} = 2.75\text{ V}$ , $V_{out} = 0.7\text{ V}$ ) ( $I_{out} = 30\ \mu\text{A}$ ) ( $I_{out} = 150\ \mu\text{A}$ ) See Figure 9	$V_{ref}$	2.010 2.075	2.035 2.100	2.060 2.125	Volts
Reference Voltage ( $V_{CC} = 2.75\text{ V}$ , $V_{out} = 0.7\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ ) $V_{CC}$ Pulse Width = 10 mS, Duty Cycle = 1.0% ( $I_{out} = 10\ \mu\text{A}$ ) ( $I_{out} = 30\ \mu\text{A}$ ) ( $I_{out} = 100\ \mu\text{A}$ ) See Figure 9	$\Delta V_{ref}$		$\pm 5$ $\pm 12$ $\pm 25$	$\pm 10$ $\pm 25$ $\pm 50$	mV

TYPICAL OPEN LOOP CHARACTERISTICS  
(Refer to Circuit of Figure 9)

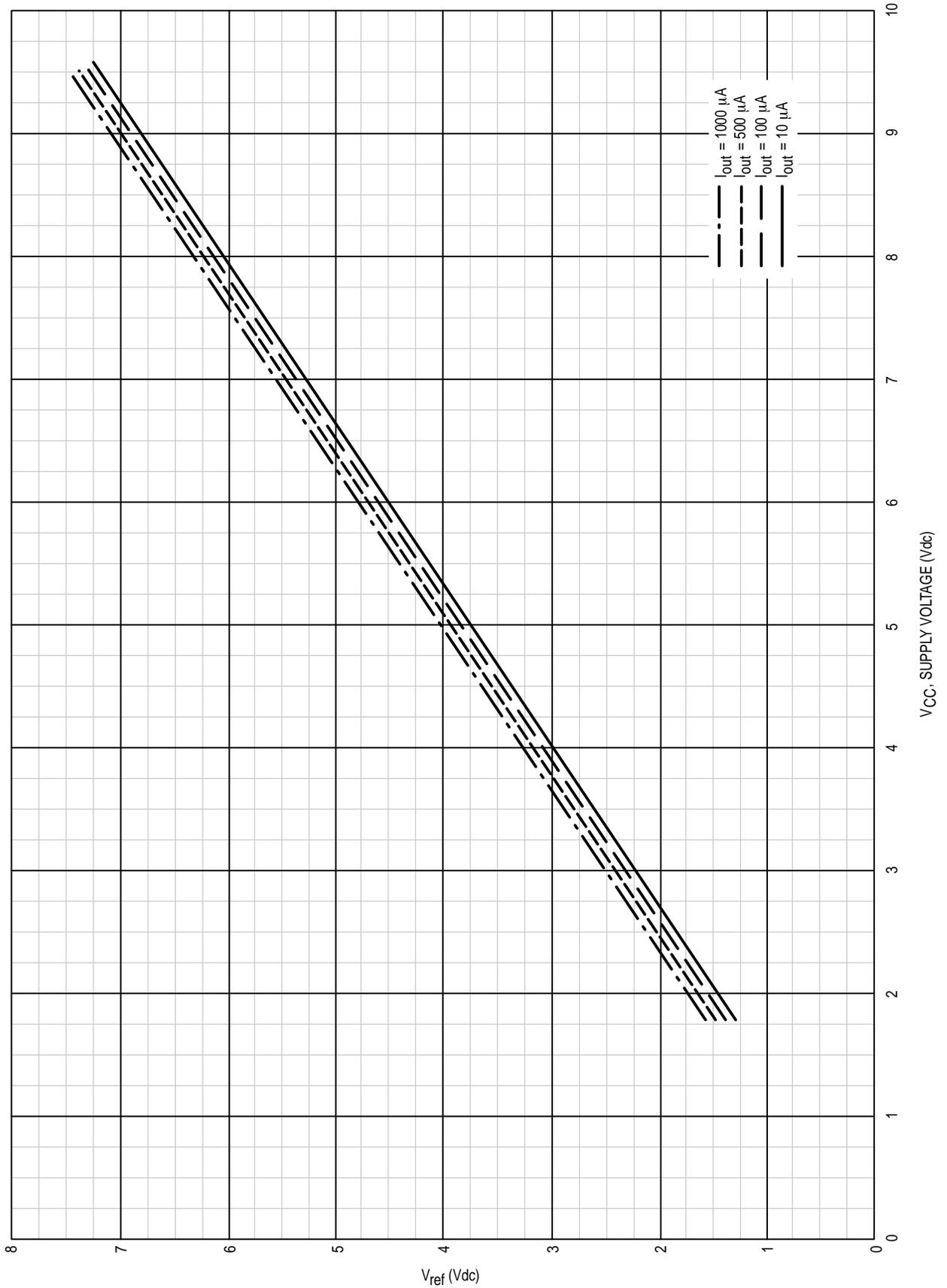
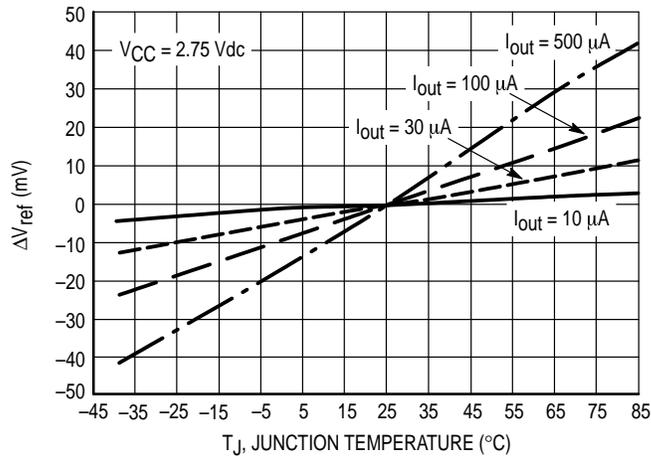
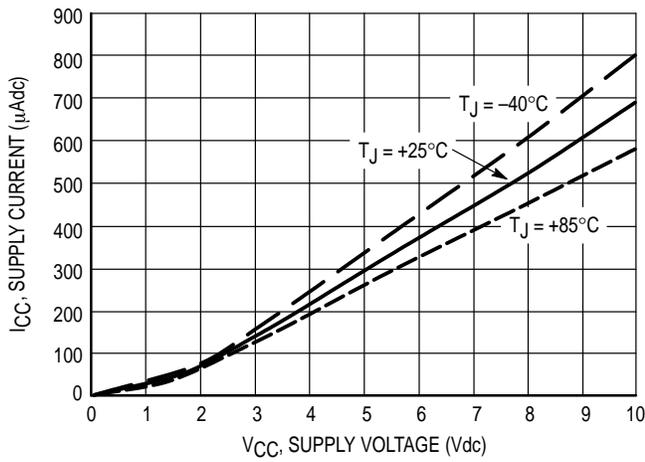


Figure 1.  $V_{ref}$  versus  $V_{CC}$  @  $I_{out}$

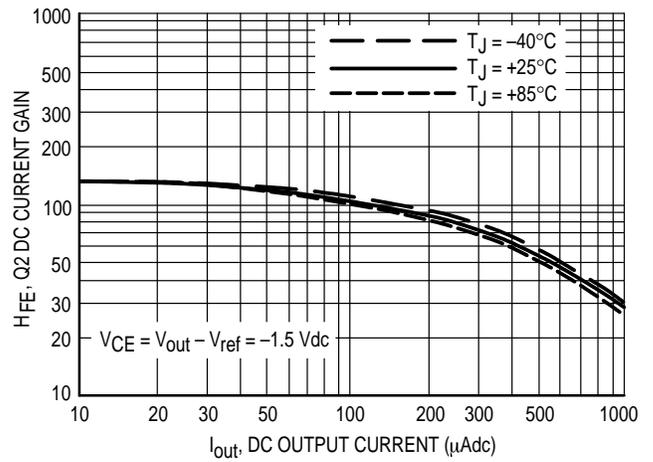
**TYPICAL OPEN LOOP CHARACTERISTICS**  
(Refer to Circuits of Figures 8, 10 & 11)



**Figure 2.  $\Delta V_{ref}$  versus  $T_J$  @  $I_{out}$**



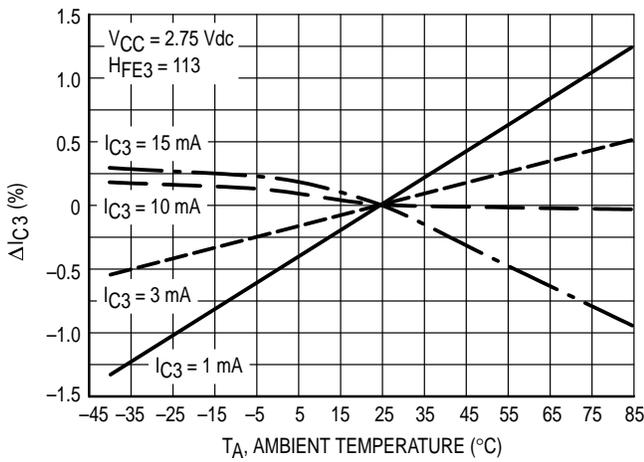
**Figure 3.  $I_{CC}$  versus  $V_{CC}$  @  $T_J$**



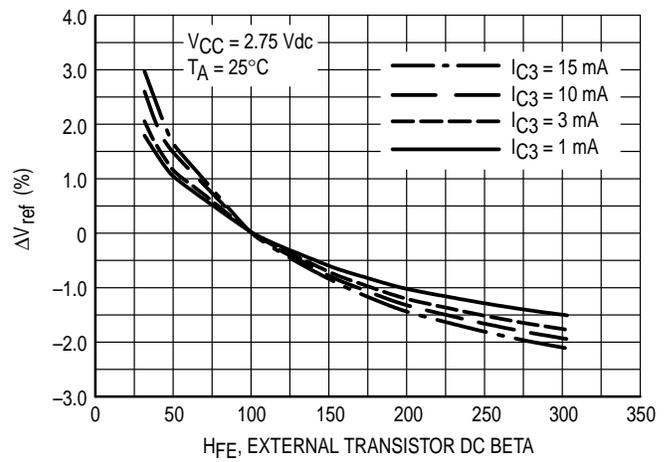
**Figure 4. Q2 Current Gain versus Output Current**

**TYPICAL CLOSED LOOP PERFORMANCE**

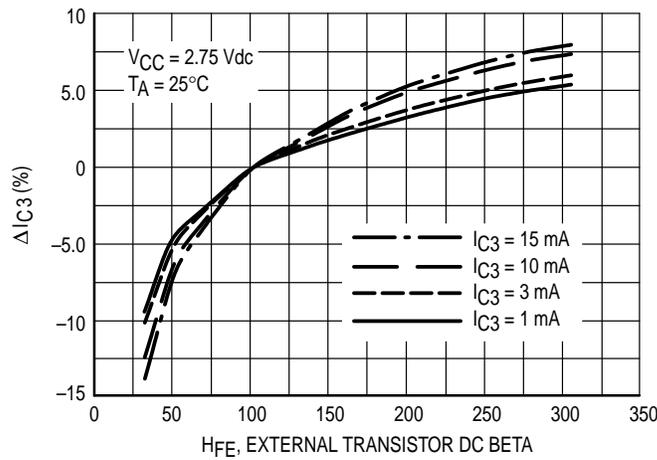
(Refer to Circuits of Figures 12 & 13)



**Figure 5.  $\Delta I_{C3}$  versus  $T_A$  @  $I_{C3}$**



**Figure 6.  $\Delta V_{ref}$  versus External Transistor DC Beta @  $I_{C3}$**



**Figure 7.  $\Delta I_{C3}$  versus External Transistor DC Beta @  $I_{C3}$**

OPEN LOOP TEST CIRCUITS

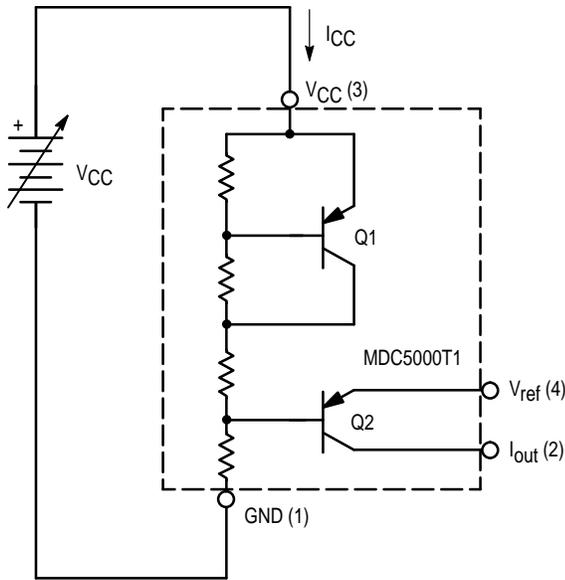
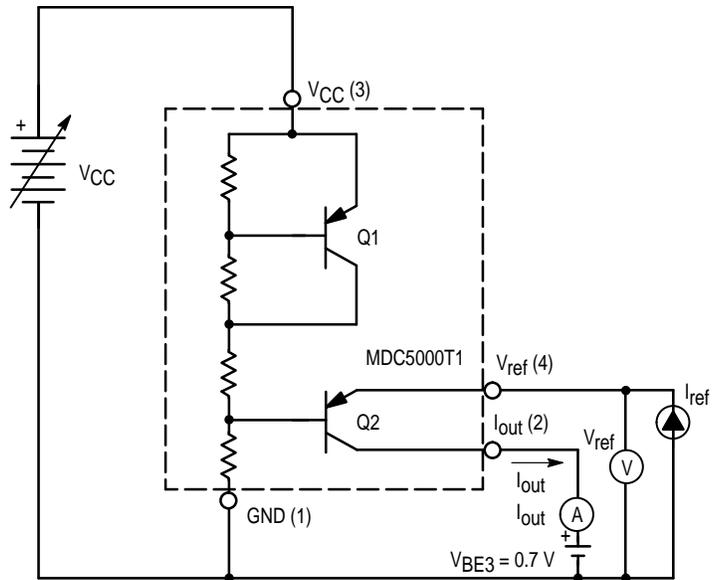
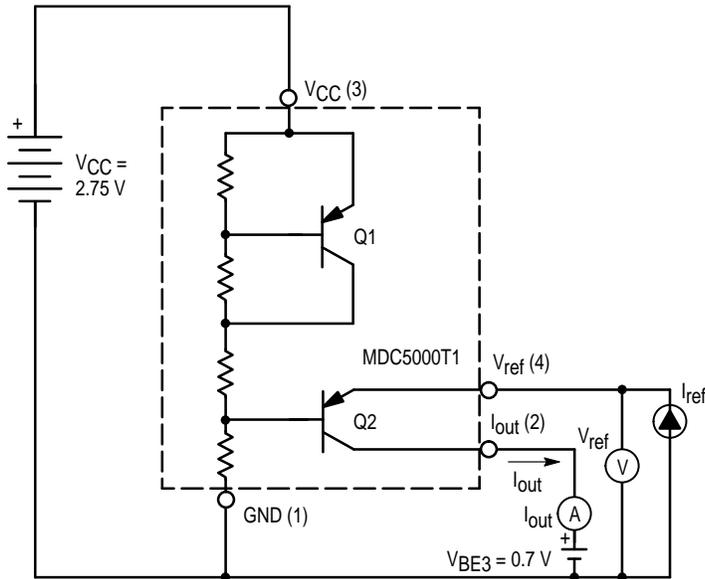


Figure 8.  $I_{CC}$  versus  $V_{CC}$  Test Circuit



NOTE:  $V_{BE3}$  is used to simulate actual operating conditions that reduce  $V_{CE2}$  &  $H_{FE2}$ , and increase  $I_{B2}$  &  $V_{ref}$ .

Figure 9.  $V_{ref}$  versus  $V_{CC}$  Test Circuit



NOTE:  $V_{BE3}$  is used to simulate actual operating conditions that reduce  $V_{CE2}$  &  $H_{FE2}$ , and increase  $I_{B2}$  &  $V_{ref}$ .

Figure 10.  $V_{ref}$  versus  $T_J$  Test Circuit

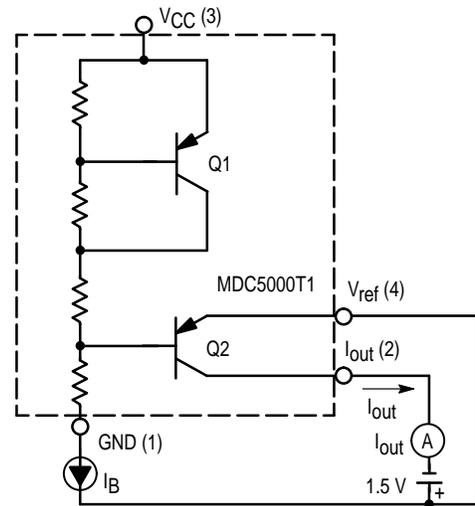
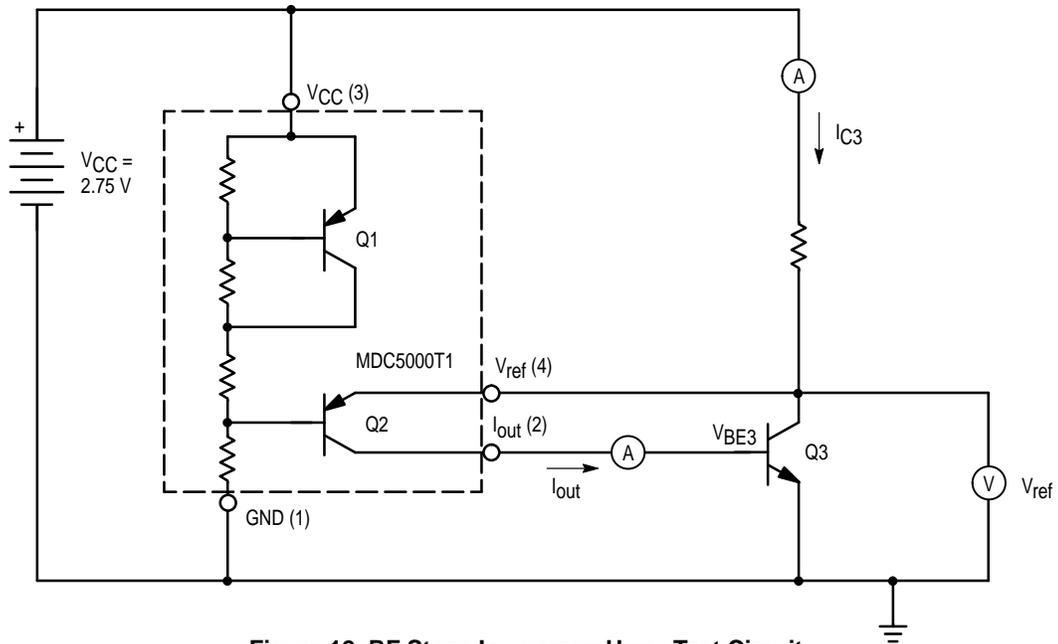
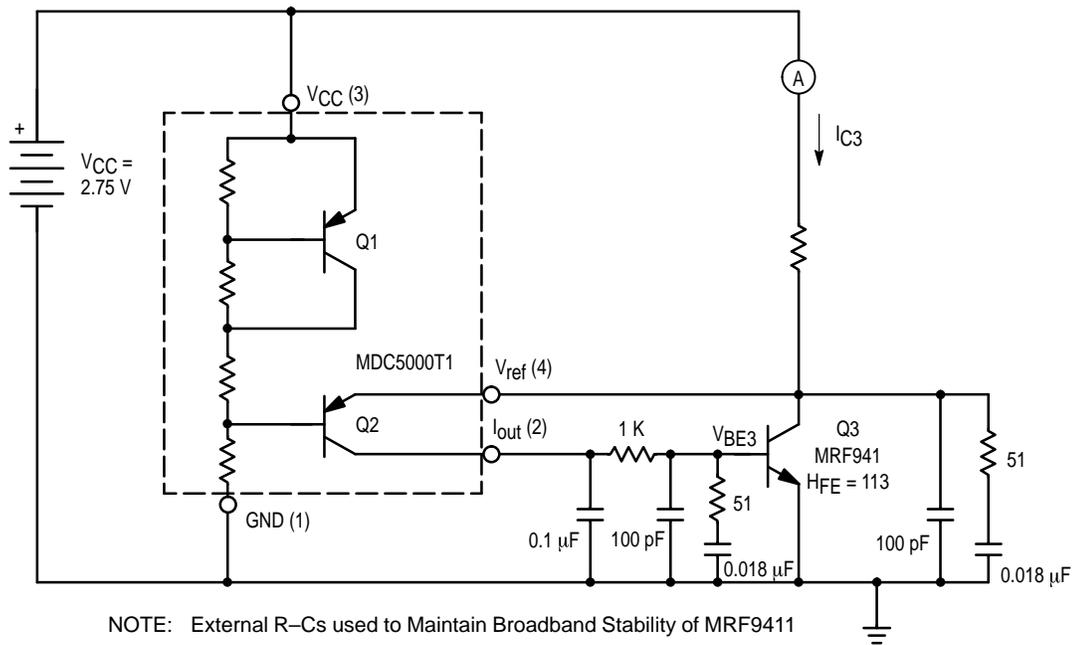


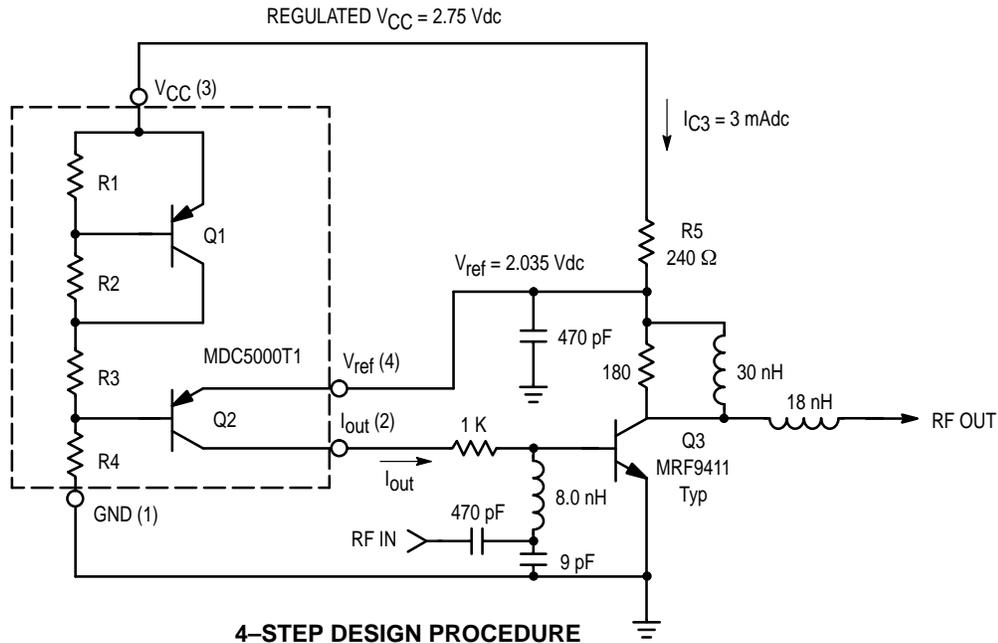
Figure 11.  $H_{FE}$  versus  $I_{out}$  Test Circuit

## CLOSED LOOP TEST CIRCUITS

Figure 12. RF Stage  $I_{C3}$  versus  $H_{FE3}$  Test Circuit

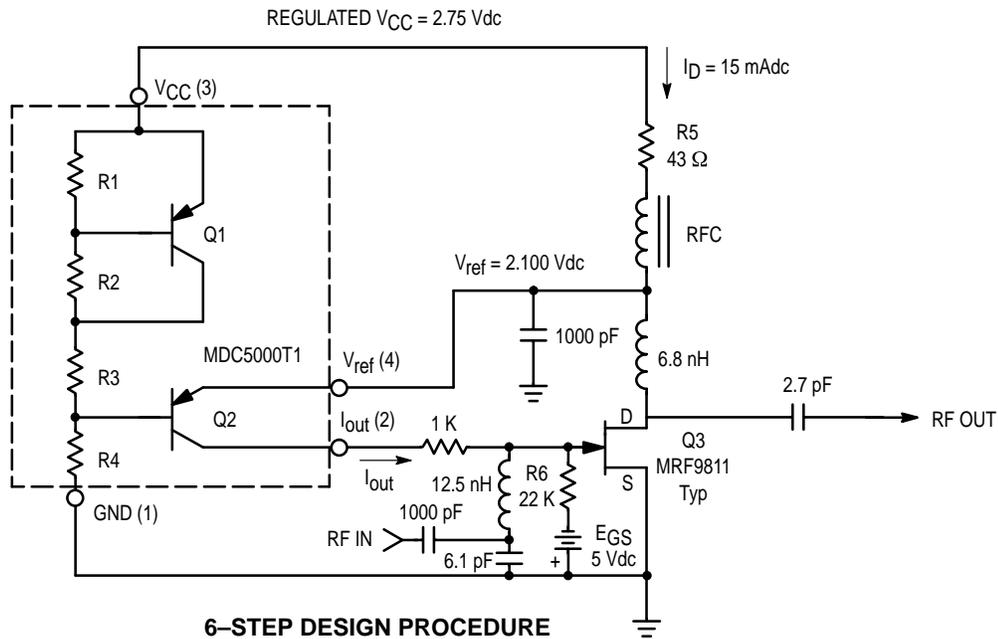
NOTE: External R-Cs used to Maintain Broadband Stability of MRF9411

Figure 13. RF Stage  $I_{C3}$  versus  $T_A$  Test Circuit



- Step 1: Choose  $V_{CC}$  (1.8 V Min to 10 V Max)
- Step 2: Choose bias current,  $I_{C3}$ , and calculate needed  $I_{out}$  from typ HFE3
- Step 3: From Figure 1, read  $V_{ref}$  for  $V_{CC}$  &  $I_{out}$  calculated.
- Step 4: Calculate Nominal  $R5 = (V_{CC} - V_{ref}) \div (I_{C3} + I_{out})$ . Tweak as desired.

**Figure 14. Class A Biasing of a Typical 900 MHz BJT Amplifier**



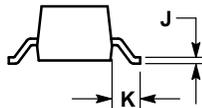
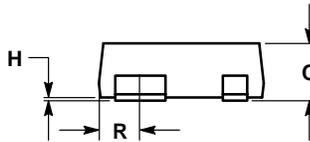
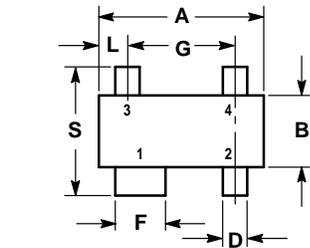
- Step 1: Choose  $V_{CC}$  (1.8 V Min to 10 V Max)
- Step 2: Choose bias current,  $I_D$ , and determine needed gate-source voltage,  $V_{GS}$ .
- Step 3: Choose  $I_{out}$  keeping in mind that too large an  $I_{out}$  can impair MDC5000T1  $\Delta V_{ref}/\Delta T_J$  performance (Figure 2) but too large an  $R6$  can cause  $I_{DGO}$  &  $I_{GSO}$  to bias on the FET.
- Step 4: Calculate  $R6 = (V_{GS} + E_{GS}) \div I_{out}$
- Step 5: From Figure 1, read  $V_{ref}$  for  $V_{CC}$  &  $I_{out}$  chosen
- Step 6: Calculate Nominal  $R5 = (V_{CC} - V_{ref}) \div (I_D + I_{out})$ . Tweak as desired.

**Figure 15. Class A Biasing of a Typical 890 MHz Depletion Mode GaAs FET Amplifier**

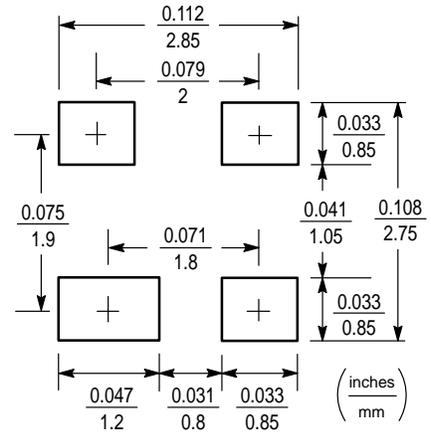
PACKAGE DIMENSIONS

- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.80	3.04	0.110	0.120
B	1.20	1.39	0.047	0.055
C	0.84	1.14	0.033	0.045
D	0.39	0.50	0.015	0.020
F	0.79	0.93	0.031	0.037
G	1.78	2.03	0.070	0.080
H	0.013	0.10	0.0005	0.004
J	0.08	0.15	0.003	0.006
K	0.46	0.60	0.018	0.024
L	0.445	0.60	0.0175	0.024
R	0.72	0.83	0.028	0.033
S	2.11	2.48	0.083	0.098



STYLE 9:  
 PIN 1. GND  
 2. IOUT  
 3. VCC  
 4. VREF



SOT-143 FOOTPRINT

CASE 318A-05  
 ISSUE M

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