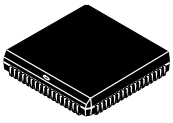
GPS Digital Correlator

The RoadRunner ASIC is a fifth generation GPS digital signal processing integrated circuit. High performance software is included which tracks eight GPS satellites simultaneously. This software sets the industry standard for tracking satellites in a high foliage and urban canyon environment.

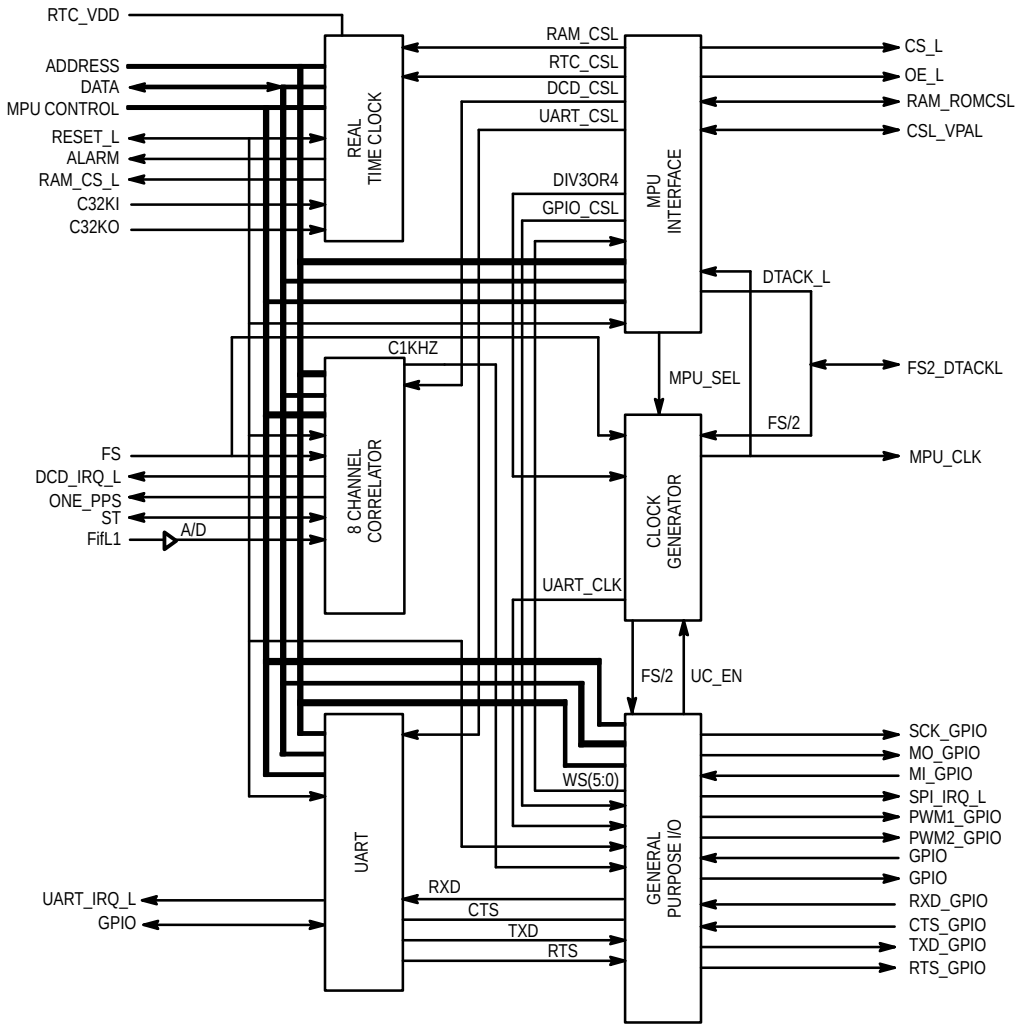
- Eight Parallel Channels
- On–chip A/D Converter
- Supports FAA WAASS PN Codes
- Operates from 5.0 or 3.3 V Power Supply
- On–chip Real Time Clock
- On–chip UART
- SPI Port
- Two PWM's
- Multiple Microprocessor Interface Support (68330, 31, 32, 68HC000, 68EC000)
- Full In–phase and Quadrature Outputs for PROMPT and EARLY Minus LATE Correlators

MCS38140PG05C

8 CHANNEL GPS CORRELATOR



CASE 779–02



Top Level Block Diagram

1.0 Summary

The RoadRunner Application Specific Integrated Circuit (ASIC) represents the 5th generation of Global Positioning System (GPS) digital signal processing integrated circuits used in Motorola commercial GPS products. When combined with an RF down converter, microprocessor, and application software, it can become the heart of a broad line of high performance and low cost GPS sensors. The RoadRunner ASIC provides additional features and achieves higher levels of performance at the same time being a driver for the design of low cost GPS applications.

The RoadRunner ASIC contains circuitry to simultaneously track up to eight satellites. Each independent receiver channel within the ASIC can be commanded to acquire and continuously track a single spread spectrum signal using any of the GPS gold codes or the FAA WAASS PN codes. The ASIC performs the following major functions of a GPS receiver:

- Samples the down converted IF signal with a 1 bit A/D converter
- Down converts the signal to baseband by removal of the IF the carrier frequency
- Signal de–spread with a replica PN code
- Doppler wipe off
- Provides digital in–phase and quadrature PROMPT and EARLY–minus–LATE outputs

The microprocessor and software control each receiver channel independently, and step the channel through the satellite acquisition process until continuous track is achieved. The acquisition and tracking functions are completely controlled by software, allowing for maximum flexibility for system enhancement and integration while maintaining a cost effective implementation.

Digital signal processing software running in the microprocessor controls the satellite tracking function by closing both code and phase/frequency tracking loops and converting the ASIC outputs into pseudorange and pseudorange–rate measurements, and decodes and stores the satellite broadcast ephemeris and clock correction data for use in down stream data processing software. These measurements and data are subsequently used in the receiver's PVT software (position, velocity, and time) in order to translate the range measurements and ephemeris data into user position coordinates.

The RoadRunner's extended features include:

- Multiple microprocessor interface support (68330, 331, 332, 68HC000, 68EC000)
- Full in–phase and quadrature outputs on PROMPT and EARLY minus LATE correlators
- Supports FAA WAASS PN codes
- Runs from 5.0 or 3.3 Volt power supply
- On–chip Real Time Clock
- On–chip UART
- Inexpensive 68 pin package

A top level block diagram of a typical GPS receiver using the RoadRunner ASIC is detailed in Figure 1.1. Five major subsystems are required to complete the design of a GPS receiver. These subsystems include an antenna/LNA, a RF downconverter (such as the Motorola MRFIC1502), a reference oscillator, the RoadRunner ASIC, and a microprocessor/memory system. When the RoadRunner ASIC is combined with the GT Oncore™ system software, the GPS receiver will receive, track, and decode data from up to 8 parallel satellites to provide high performance position, velocity, and time data to a user application.

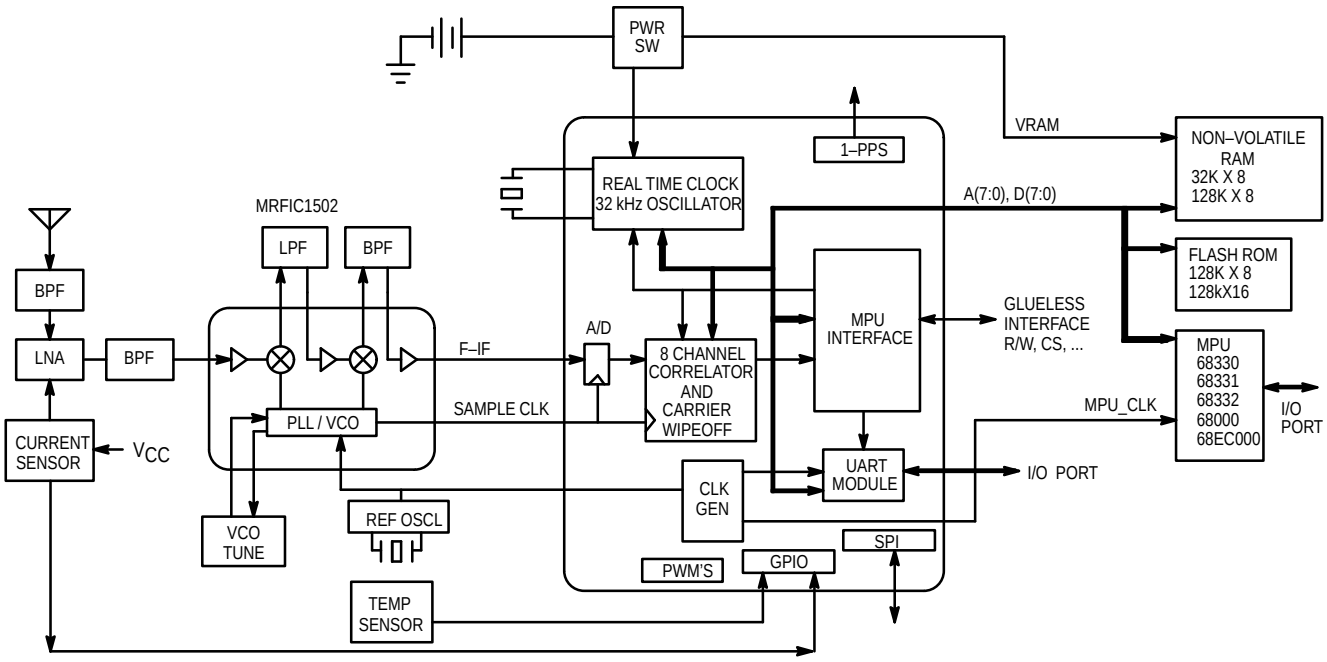


Figure 1.1 A Typical GPS Reciever Block Diagram with a RoadRunner ASIC

2.0 I/O Description and Top Level Block Diagram

Table 2.1 provides a list of the functional pins of the ASIC with the I/O type and a short description. Figure 2.1 shows the top level block diagram of the ASIC showing the connection of each pin to an internal functional block.

Table 2.1 Input–Output Functional Pin Description

Signal Name	Pin#	Type	Description
A23	66	I	Address Bus
A22	67	I	Address Bus
S21	68	I	Address Bus
A7	1	I	Address Bus
A6	2	I	Address Bus
A5	3	I	Address Bus
A4	4	I	Address Bus
A3	5	I	Address Bus
A2	6	I	Address Bus
A1	7	I	Address Bus
A0	8	I	Address Bus
D7	54	I/O	Data Bus & Special reset configure pin
D6	53	I/O	Data Bus & Special reset configure pin
D5	51	I/O	Data Bus
D4	50	I/O	Data Bus
D3	49	I/O	Data Bus
D2	48	I/O	Data Bus
D1	**47**	I/O	Data Bus
D0	46	I/O	Data Bus
RAM_ROMCSL	55	I/O	RAM Chip Select/ROM Chip Select
CSL_VPAL	42	I/O	RR Chip Select/Valid Peripheral Address
AS_L	44	I	Data Strobe
R_W_L	43	I	Read/Write
FS2_DTACKL	26	O	Sampled Clock/2 or Data Transfer Acknowledge
CS_L	56	O	Spare Chip Select
MPU_CLK	34	O	MPU Clock
RESET_L	27	I	Active Low Reset
DCD_IRQ_L	39	O	1 kHz Interrupt
UART_IRQ_L	38	O	UART Interrupt
SPI_IRQ_L	37	O	SPI Interface Interrupt
OE_L	40	O	Output Enable
RAM_CS_L	32	O	RAM Chip Select
FS	16	I	Sample Clock Input
FifL1	10	I	L1 IF Input Port (small signal, 1 bit A/D internal)
ST	36	O	Self Test Output
ONE_PPS	35	O	1PPS Output
MO_GPIO	58	I/O	SPI Serial Data Output/GPIO
MI_GPIO	59	I/O	SPI Serial Data Input/GPIO
SCK_GPIO	57	I/O	SPI Clock Output/GPIO
PWM1_GPIO	61	I/O	Pulse Width Modulated Output 1/GPIO
PWM2_GPIO	62	I/O	Pulse Width Modulated Output 2/GPIO

Table 2.1 Input–Output Functional Pin Description (continued)

Signal Name	Pin#	Type	Description
GPIO	64	I/O	GPIO
GPIO	65	I/O	GPIO
C32KI	28	I	32 kHz Osc. Input
C32KO	29	O	32 kHz Osc. Output
ALARM	31	O	Real Time Clock Timeout Signal
RXD_GPIO	22	I/O	Received Data Input/GPIO
TXD_GPIO	21	I/O	Transmit Data Output/GPIO
CTS_GPIO	19	I/O	Clear To Send Input/GPIO
RTS_GPIO	20	I/O	Request To Send Output/GPIO
GPIO	18	I/O	General Purpose I/O
GND	12, 13, 14, 17, 24, 25, 33, 45, 60		Ground
V_{DD}	11, 15, 23, 41, 52, 63		Correlator Circuit V_{DD}
VDD_RTC	30		RTC/Oscl Circuits V_{DD}

A23–21, A7–A0

The upper three bits of the address bus are used for address decoding for the 68K interface. The lower 8 bits of the address bus is used as an offset to the RoadRunner base address.

D7–D0

The 8–bit bidirectional data bus will be connected to either the upper or lower byte of the microprocessor data bus. D7 and D6 pins are special configuration inputs upon power–up reset. These two pins have pin state detectors that allow internal circuitry to configure the ASIC within 8 system clocks after the RESET_L pin transitions from low to high. These two pins control the MPU type (33x or 680x0), and the source of the MPU clock.

RAM_ROMCSL

In a 6833x microcontroller system, this pin is an input from the programmable chip select intended for RAM. The RoadRunner then provides RAM write protection while RESET_L is active. In a 680x0 system, this pin is an output as the ROM chip select which is active for a hardwired address range and upon Boot.

CSL_VPAL

In a 6833x controller system, this pin is an input from the programmable chip select intended to select the RoadRunner ASIC. The chip select is programmed with the RoadRunner base address. In a 680x0 system, this pin is the valid peripheral address signal connected directly to VPA on the 680x0. This signal will only be active when A23–A21 are all high to terminate an IACK cycle with an autovector, no external peripherals can use this address space in a 680x0 system.

AS_L

The address strobe input from the microprocessor is used to qualify address decoding in a 680x0 system and as a data strobe in any system for RoadRunner registers.

R_W_L

The controller read/write signal is used to differentiate read or write cycles when RoadRunner registers are addressed. It is also used to generate the output enable (OE_L) signal.

FS2_DTACKL

In a 6833x microcontroller system, this pin is the sample frequency divided by two. In a 680x0 system, this signal is the active low DTACK output to the 680x0. In a 680x0 system, DTACK will be generated for all address ranges except for when A23–A21 are all High. Some of these address ranges have DTACK generation with programmable wait states.

CS_L

This pin is a spare chip select output, it has a hard–wired address range of A23–A21 equal to “110”. For a 680x0 system, the DTACK for this address range can be pr ogrammed for 1, 2, 4, or 8 wait states. With the 6833x processor, DSACKs for this address range will have to be generated externally. A zero wait state peripheral should be used here, so that CS_L could be connected to a DSACK pin.

MPU_CLK

The MPU_CLK signal is generated by the RoadRunner to be the input clock for the microprocessor clock synthesizer. For a 6833x microcontroller based system, the frequency is FS/2 divided by 656. For 680x0 systems, this clock is FS divided by 3 or 4

Fs	MPU	MPU_CLK
38.192 MHz	33x	29.109 kHz
38.192 MHz	0x0	12.731/9.548 MHz

RESET_L

The reset signal to the RoadRunner will bring all pertinent parts of the RoadRunner to a known state upon power up.

DCD_IRQ_L

This is a 1 kHz interrupt signal.

UART_IRQ_L

This is the interrupt output from the UART. It is a single interrupt representing all of the UART interrupt sources.

SPI_IRQ_L

This signal is an active low interrupt signal from the SPI circuit on the ASIC.

OE_L

The OE_L signal is an output enable signal used for RAM and ROM.

RAM_CS_L

This signal is a write protected RAM chip select signal. In a 6833x system, the RAM address space will be programmable using a programmable chip select from the microprocessor and input on the RAM_ROMCSL signal. Internally, this signal is gated with the RESET_L signal, so that RAM_CS_L is forced high if RESET_L is low. In a 680x0 system the RAM address space is hardwired, and decoded within the RoadRunner. It will be inactive upon Boot.

Fs

The CMOS level sample frequency input clock is 38.192 MHz.

FifL1

This signal is the small signal L1 IF analog input from the RFIC. An internal 1 bit A/D converter samples this input port at sample frequency of Fs.

ST

This signal is a self–test output signal. When configured into the self–test mode, the ASIC outputs the PN code generated from channel 1 mixed with Fs/4 and the NCO cosine output from channel 1, and provides the resulting signal on the ST output pin. This data can then be fed–back into the A/D converter or RF path in order to generate a signal that the system can detect.

ONE_PPS

This is the One Pulse Per Second output used for timing applications. It is also controllable via software to be a general purpose output signal.

MO_GPIO

Serial Peripheral Interface data output, or general purpose I/O pin. Default after reset is GPIO input.

MI_GPIO

Serial Peripheral Interface data input, or general purpose I/O pin. Default after reset is GPIO input.

SCK_GPIO

Serial Peripheral Interface clock output, or general purpose I/O pin. Default after reset is GPIO input.

PWM1_GPIO

Pulse width modulator output, or general purpose I/O pin. Default after reset is GPIO input.

PWM2_GPIO

Pulse width modulator output, or general purpose I/O pin. Default after reset is GPIO input.

C32KI, C32KO

The C32KI input and C32KO output are 32.768 kHz crystal oscillator signals, to generate a clock for the Real Time Clock. If the oscillator is external, then the clock signal should be input to the C32KI input.

ALARM

Real Time Clock timeout signal which could be used to wake up a system.

RXD_GPIO

This is the Received Data signal to the UART, or general purpose I/O pin. Default after reset is GPIO input.

TXD_GPIO

This is the Transmit Data signal from the UART, or general purpose I/O pin. Default after reset is GPIO input.

CTS_GPIO

This is the Clear To Send signal to the UART, or general purpose I/O pin. Default after reset is GPIO input.

RTS_GPIO

This is the Request To Send signal from the UART, or general purpose I/O pin. Default after reset is GPIO input.

3.0 Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Limit	Unit
DC Supply Voltage	V_{DD}	–0.5 to +7.0	Vdc
DC Supply Current	I_{DD}	—	mA
Operating Ambient Temperature	T_A	–40 to +105	C
Storage Temperature	T_{stg}	–55 to 150	C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	—	5.5	V
Input Voltage	V_{in}	0	—	V_{DD}	V
Digital Current (V_{DD} = 5.0 V)	I_{DD}	—	30	—	mA
RTC I_{DD}	I_{DD}	—	—	1.0	µA
Operating Temperature Range	T_A	–40	—	+105	C

DC CHARACTERISTICS (V_{DD} = 5.0 V ±10%, T_A = –40°C to 105°C)

Characteristic	Symbol	Value	Units
Min High–Level Input Voltage	V_{IH}	70% V_{DD}	V
Max Low–Level Input Voltage	V_{IL}	30% V_{DD}	V
Input Leakage Current, No Pull Up/Down Resistor	I_{in}	±200	µA
Output Leakage Current, 3–State Output	I_{OZ}	±5.0	µA
Input Capacitance	C_{in}	10	pF

DC ELECTRICAL CHARACTERISTICS

Characteristic	Test Cond	Symbol	Min	Max	Unit
PINS 31, 56					
Output Current High	V_{DD} = 3.0 V V_{OH} = 2.4 V	I_{OH}	—	–1.5	mA
Output Current Low	V_{DD} = 3.0 V V_{OL} = 400 mV	I_{OL}	2.0	—	mA
PINS 32, 34, 35, 36, 40					
Output Current High	V_{DD} = 3.0 V V_{OH} = 2.4 V	I_{OH}	—	–2.5	mA
Output Current Low	V_{DD} = 3.0 V V_{OL} = 400 mV	I_{OL}	3.0	—	mA
PINS 18, 19, 22, 46, 47, 48, 49, 50, 51, 53, 54, 57, 59, 61, 62, 64, 65					
Output Current High	V_{DD} = 3.0 V V_{OH} = 2.4 V	I_{OH}	—	–1.5	mA
Output Current Low	V_{DD} = 3.0 V V_{OL} = 400 mV	I_{OL}	2.0	—	mA
PINS 10, 11, 22, 53, 54, 57, 59, 61, 62, 64, 65					
Input Pullup Current	V_{DD} = 5.0 V V_{in} = 0 V	I_{IL}	–60	–10	µA
Tri State Leakage High	V_{DD} = 5.5 V V_{in} = 5.5 V	HIZ	—	5.0	µA
PINS 46, 47, 48, 49, 50, 51					
Tri State Leakage High	V_{DD} = 5.5 V V_{in} = 5.5 V	HIZ(on)	–1.0	1.0	µA
Tri State Leakage Low	V_{DD} = 5.5 V V_{in} = 0 V	HIZ	–5.0	—	µA
PINS 20, 21, 26, 55					
Output Current High	V_{DD} = 3.0 V V_{OH} = 2.4 V	I_{OH}	—	–2.5	mA
Output Current Low	V_{DD} = 3.0 V V_{OL} = 400 mV	I_{OL}	3.0	—	mA

DC ELECTRICAL CHARACTERISTICS (continued)

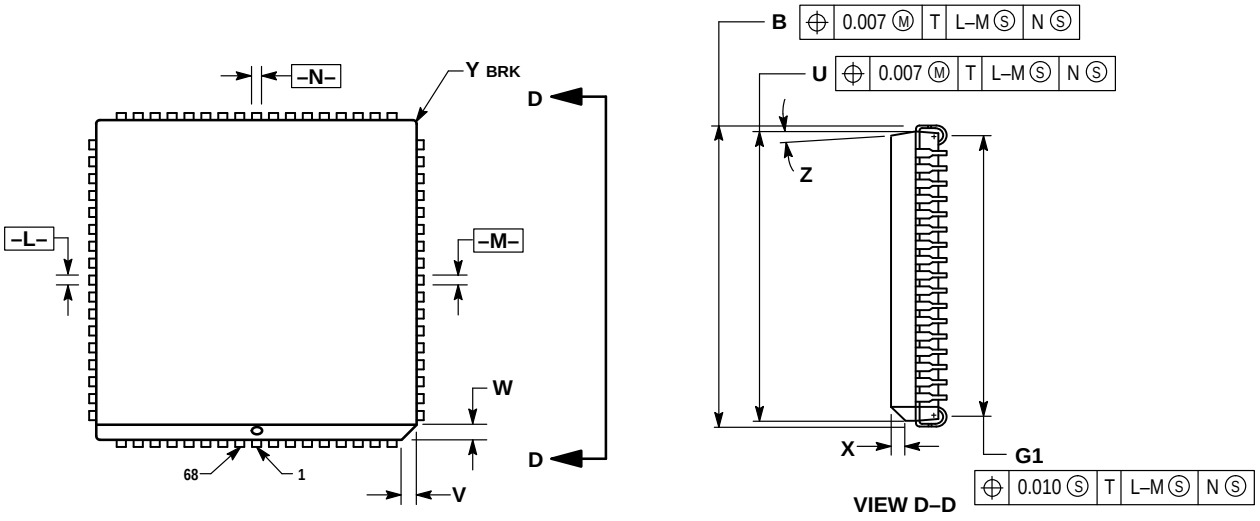
Characteristic	Test Cond	Symbol	Min	Max	Unit
PINS 26, 55					
Input Pullup Current	V_{DD} = 5.0 V V_{in} = 0 V	I_{IL}	–60.0	–10	µA
Tri State Leakage High	V_{DD} = 5.5 V V_{in} = 5.5 V	HIZ	—	5.0	µA
Tri State Leakage Low	V_{DD} = 5.5 V V_{in} = 0 V	HIZ	–5.0	—	µA
PINS 20, 21					
Input Pullup Current	V_{DD} = 5.0 V V_{in} = 0 V	I_{IL}	–60.0	–10	µA
Tri State Leakage High	V_{DD} = 5.5 V V_{in} = 5.5 V	HIZ(on)	–1.0	1.0	µA
PINS 31, 56					
Output Current Low	V_{DD} = 3.0 V V_{OL} = 400 mV	I_{OL}	2.0	—	mA
Tri State Leakage High	V_{DD} = 5.5 V V_{in} = 5.5 V	HIZ	—	5.0	µA
Tri State Leakage Low	V_{DD} = 5.5 V V_{in} = 0 V	HIZ	–5.0	—	µA
PINS 1–8, 16, 27, 43, 44, 66, 67, 68					
Input Leakage High	V_{in} = 5.5 V	I_{IH}	—	1.0	µA
Input Leakage Low	V_{in} = 0 V	I_{IL}	–1.0	—	µA
PINS 28, 29					
Input Leakage High	V_{DD} = 5.5 V V_{in} = 5.5 V	I_{IH}	—	1.0	µA
Input Leakage Low	V_{DD} = 5.5 V V_{in} = 0 V	I_{IL}	–1.0	—	µA
Osc Thres 3.0 V	V_{DD} = 3.0 V	Vth3v	1.23	1.59	V
DC Gain 3.0 V	V_{DD} = 3.0 V	Dcg3v	14.7	30.6	V
GM 3.0 V	V_{DD} = 3.0 V	Gm3v	3.78e–4	1.02e–3	V
Osc Thres 5.5 V	V_{DD} = 5.5 V	Vth5.5v	2.33	2.92	V
DC Gain 5.5 V	V_{DD} = 5.5 V	Dcg5.5v	15.0	46.0	V
GM 5.5 V	V_{DD} = 3.0 V	Gm5.5v	9.97e–4	2.86e–3	V
PIN 10					
Input Bias Current	V_{in} = 5.5 V	I_{IH}	197	348	µA
Input Bias Current	V_{in} = 0 V	I_{IL}	–349	–199	µA
Vself–bias 3.0 V	V_{DD} = 3.0 V	Vslf3v	1.2	1.88	V
Vself–bias 5.0 V	V_{DD} = 5.0 V	Vslf5v	2.41	3.59	V

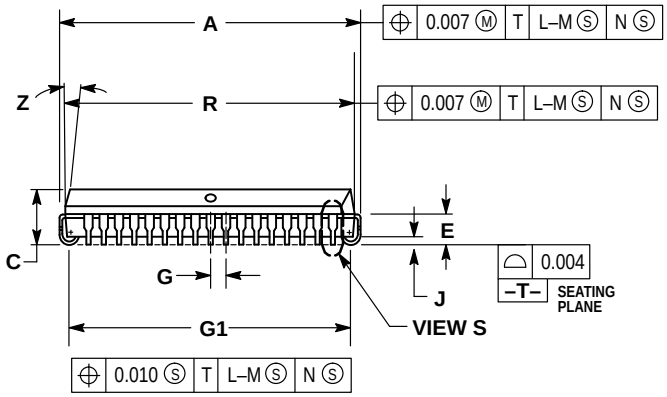
4.0 Minimum/Maximum I/O Timing Characteristics

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V ±10%, T_A = –30°C to 100°C)

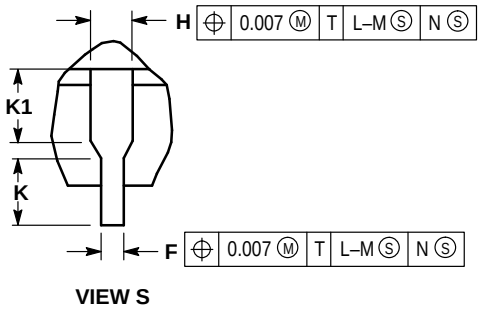
Characteristic	Min	Max	Unit
FS High to ONE_PPS High	3	15	ns
FS High to ONE_PPS Low	3	20	ns
FS, FS2_DTACKL High to MPU_CLK High	3	25	ns
FS, FS2_DTACKL High/Low to MPU_CLK Low	3	30	ns
AS_L Low to CS_L Low	3	30	ns
AS_L High to CS_L High	3	20	ns
AS_L Low to OE_L Low	3	20	ns
AS_L High to OE_L High	3	15	ns
RAM_ROMCSL Low to RAM_CS_L Low (68331)	3	20	ns
RAM_ROMCSL High to RAM_CS_L High (68331)	3	15	ns
AS_L Low to RAM_CS_L Low (68EC000)	3	25	ns
AS_L High to RAM_CS_L High (68EC000)	3	20	ns
RESET_L Low to RAM_CS_L High	3	15	ns
AS_L Low to D7–D0 Valid (Read Cycle)	—	40	ns
AS_L High to D7–D0 Invalid (Read Cycle)	3	—	ns
AS_L High to D7–D0 High–Z (Read Cycle)	—	30	ns
D7–D0 Setup wrt AS_L High (Write Cycle)	5	—	ns
D7–D0 Hold wrt AS_L High (Write Cycle)	5	—	ns
AS_L Low to FS2_DTACKL Low (68EC000, 0 Wait State)	3	25	ns
AS_L High to FS2_DTACKL High (68EC000)	3	20	ns
FS High to FS2_DTACKL Low (68EC000, >0 Wait States)	3	40	ns
AS_L Low to CSL_VPAL Low (68EC000)	3	35	ns
AS_L High to CSL_VPAL High (68EC000)	3	25	ns
R_W_L Setup wrt AS_L Low	5	—	ns
R_W_L Hold wrt AS_L High	5	—	ns
A23–A21,A7–A0 Setup wrt AS_L Low	5	—	ns
A23–A21,A7–A0 Hold wrt AS_L High	5	—	ns
AS_L Pulse Width	45	—	ns

PACKAGE DIMENSIONS





NOTES:
1. DATUMS L, M, AND N DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM T, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLowABLE MOLD FLASH IS 0.010 PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012. DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037. THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025.



	INCHES	
DIM	MIN	MAX
A	0.985	0.995
B	0.985	0.995
C	0.165	0.180
E	0.090	0.110
F	0.013	0.019
G	0.050 BSC	
H	0.026	0.032
J	0.020	—
K	0.025	—
R	0.950	0.956
U	0.950	0.956
V	0.042	0.048
W	0.042	0.048
X	0.042	0.056
Y	—	0.020
Z	2°	10°
G1	0.910	0.930
K1	0.040	—

CASE 779–02
ISSUE C

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