


MCM6706BR



J PACKAGE
300 MIL SOJ
CASE 857-02

PIN ASSIGNMENT

A	1	●	32	NC
A	2		31	A
A	3		30	A
A	4		29	A
\overline{E}	5		28	\overline{G}
DQ	6		27	DQ
DQ	7		26	DQ
V_{CC}	8		25	V_{SS}
V_{SS}	9		24	V_{CC}
DQ	10		23	DQ
DQ	11		22	DQ
\overline{W}	12		21	A
A	13		20	A
A	14		19	A
A	15		18	A
A	16		17	NC

- Single 5.0 V \pm 10% Power Supply
- Fully Static — No Clock or Timing Strokes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6706BR-6 = 6 ns
MCM6706BR-7 = 7 ns
MCM6706BR-8 = 8 ns
- Center Power and I/O Pins for Reduced Noise

The diagram illustrates a memory array architecture. On the left, eight address lines (A) are connected to a **ROW DECODER**. The decoder's output is connected to a **MEMORY MATRIX** block, which is labeled **512 ROWS x 64 x 8 COLUMNS**. The memory matrix is powered by **VCC** and **VSS** lines. Below the memory matrix, a **COLUMN I/O** block is connected to the matrix's output. This block is also connected to an **INPUT DATA CONTROL** block. The input data control block has two inputs: **D0** and **DQ**. The output of the input data control block is connected to the **COLUMN DECODER**, which has six outputs labeled **A**. The **COLUMN DECODER** is also connected to the **MEMORY MATRIX**. At the bottom, there are control signals: **E** (enable), **W** (write), and **G** (gate). These signals are connected to two AND gates. The first AND gate has inputs from **E** and **DQ**. The second AND gate has inputs from **E** and **G**. The outputs of these AND gates are connected to the **MEMORY MATRIX** and the **COLUMN DECODER**.

<u>A</u>	Address
<u>W</u>	Write Enable
<u>E</u>	Chip Enable
<u>G</u>	Output Enable
<u>DQ</u>	Data Input/Output
<u>VCC</u>	+ 5 V Power Supply
<u>VSS</u>	Ground
<u>NC</u>	No Connection

REV 1
10/9/96

TRUTH TABLE

E	G	W	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High-Z	—
L	H	H	Read	High-Z	—
L	L	H	Read	D _{out}	Read Cycle
L	X	L	Write	D _{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	− 0.5 to + 7.0	V
Voltage Relative to V _{SS} for Any Pin Except V _{CC}	V _{in} , V _{out}	− 0.5 to V _{CC} + 0.5	V
Output Current	I _{out}	± 30	mA
Power Dissipation	P _D	2.0	W
Temperature Under Bias	T _{bias}	− 10 to + 85	°C
Operating Temperature	T _A	0 to + 70	°C
Storage Temperature — Plastic	T _{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V _{CC}	4.5	5.0	5.5	V
Input High Voltage	V _{IH}	2.2	—	V _{CC} + 0.3*	V
Input Low Voltage	V _{IL}	− 0.5**	—	0.8	V

* V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

** V_{IL} (min) = − 0.5 V dc @ 30.0 mA; V_{IL} (min) = − 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V _{in} = 0 to V _{CC})	I _{lkg(I)}	—	± 1.0	μA
Output Leakage Current (E = V _{IH} or G = V _{IH} ; V _{out} = 0 to V _{CC})	I _{lkg(O)}	—	± 1.0	μA
Output High Voltage (I _{OH} = − 4.0 mA)	V _{OH}	2.4	—	V
Output Low Voltage (I _{OL} = + 8.0 mA)	V _{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	−6	−7	−8	Unit	Notes
AC Active Supply Current (I _{out} = 0 mA, V _{CC} = max, f = f _{max})	I _{CCA}	215	205	195	mA	1, 2, 3
AC Standby Current (E = V _{IH} , V _{CC} = max, f = f _{max})	I _{SB1}	95	85	75	mA	1, 2, 3
CMOS Standby Current (V _{CC} = max, f = 0 MHz, E ≥ V _{CC} − 0.2 V, V _{in} ≤ V _{SS} , or ≥ V _{CC} − 0.2 V)	I _{SB2}	20	20	20	mA	

NOTES:

- Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
- All addresses transition simultaneously low (LSB) and then high (MSB).
- Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C _{in}	5	pF
Control Pin Input Capacitance (E, G, W)	C _{in}	6	pF
I/O Capacitance	C _{out}	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level 1.5 V
 Input Pulse Levels 0 to 3.0 V
 Input Rise/Fall Time 2 ns

Output Timing Measurement Reference Level 1.5 V
 Output Load See Figure 1a

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	6706BR-6		6706BR-7		6706BR-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t _{AVAV}	6	—	7	—	8	—	ns	3
Address Access Time	t _{AVQV}	—	6	—	7	—	8	ns	
Chip Enable Access Time	t _{ELQV}	—	6	—	7	—	8	ns	
Output Enable Access Time	t _{GLQV}	—	4	—	4	—	4	ns	
Output Hold from Address Change	t _{AXQX}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t _{ELQX}	3	—	3	—	3	—	ns	4, 5, 6
Chip Enable High to Output High-Z	t _{EHQZ}	—	3	—	3.5	—	3.5	ns	4, 5, 6
Output Enable Low to Output Active	t _{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Output Enable High to Output High-Z	t _{GHQZ}	—	3	—	3.5	—	3.5	ns	4, 5, 6

NOTES:

1. W is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady-state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected (E = V_{IL}, G = V_{IL}).
8. Addresses valid prior to or coincident with E going low.

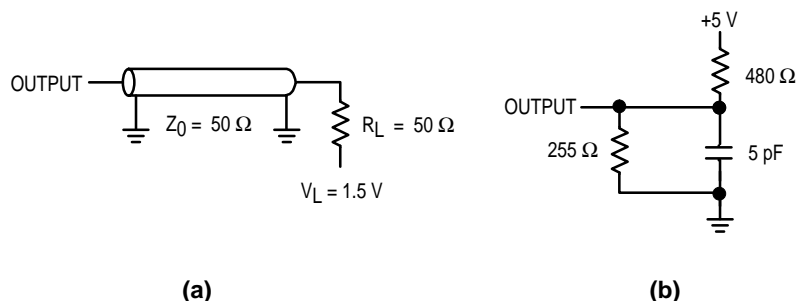
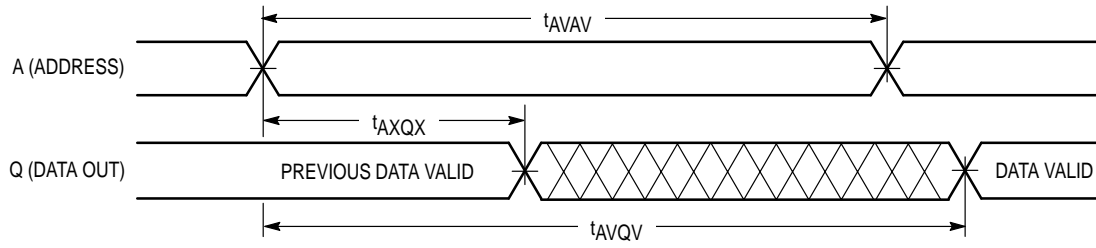


Figure 1. AC Test Loads

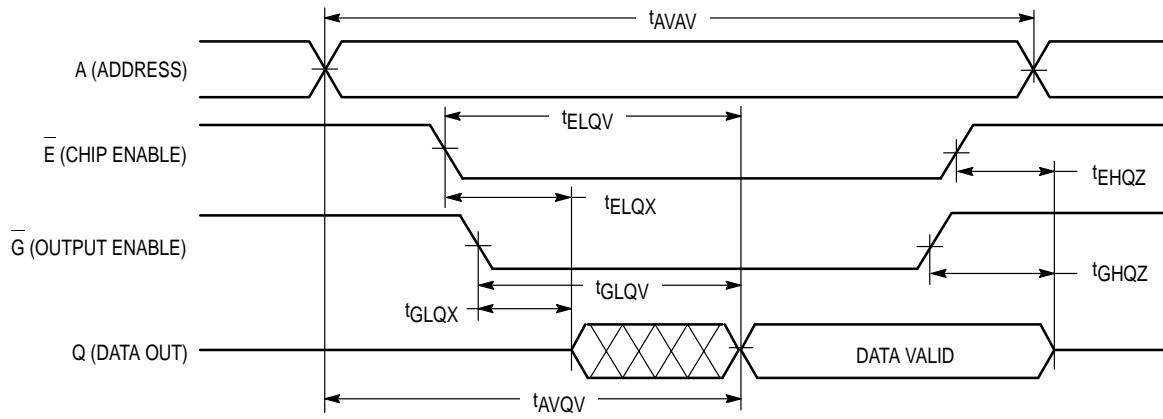
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)



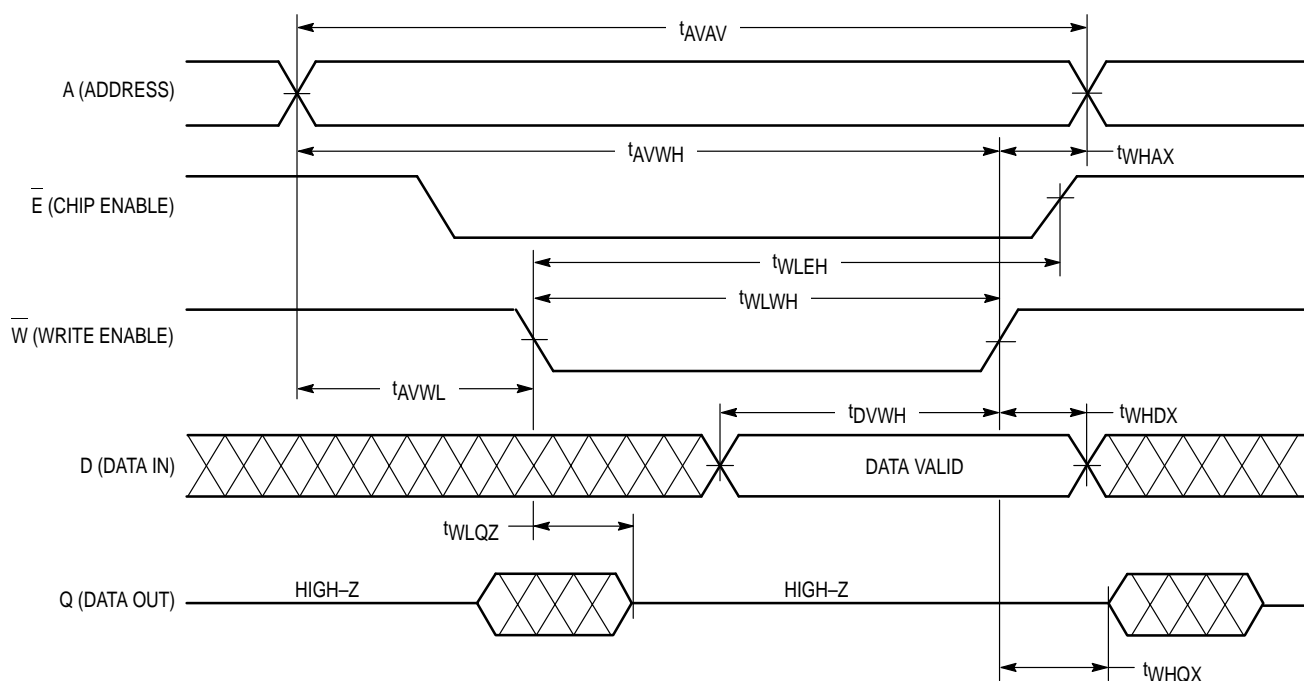
WRITE CYCLE 1 (\overline{W} Controlled, See Notes 1 and 2)

Parameter	Symbol	6706BR-6		6706BR-7		6706BR-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	6	—	7	—	8	—	ns	
Write Pulse Width	t_{WLWH} , t_{WLEH}	6	—	7	—	8	—	ns	
Data Valid to End of Write	t_{DVWH}	3	—	3.5	—	3.5	—	ns	
Data Hold Time	t_{WDHX}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	—	3.5	—	3.5	—	3.5	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of \overline{E} low and \overline{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady-state voltage with load of Figure 1b.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1



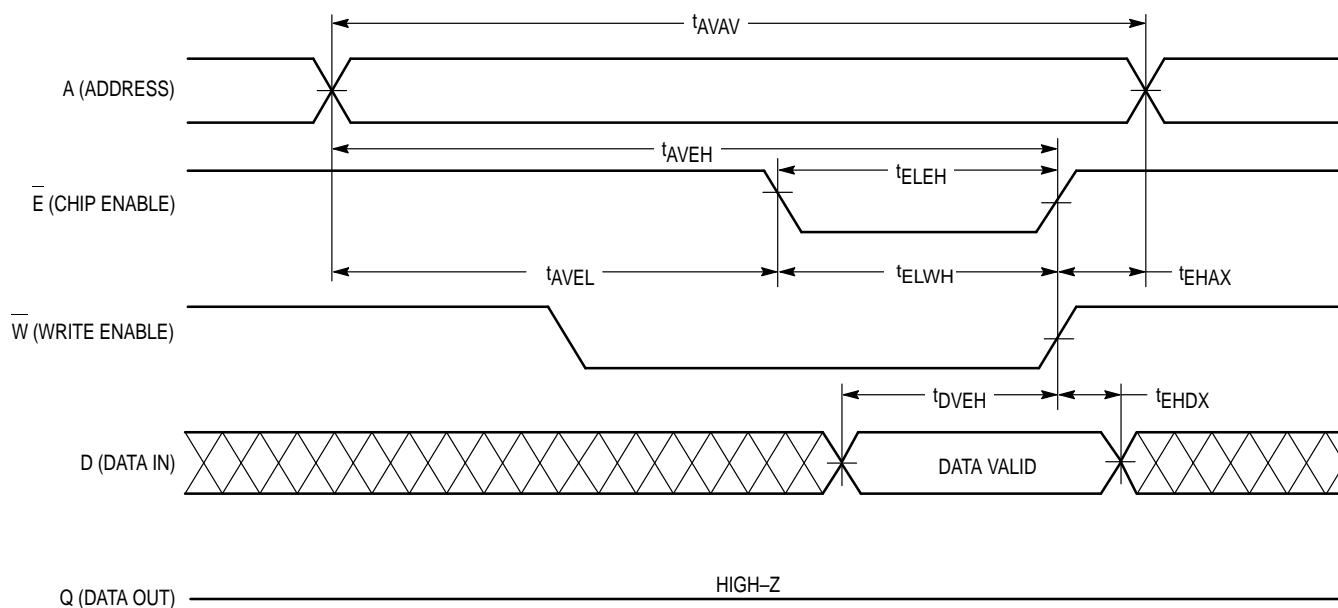
WRITE CYCLE 2 (\overline{E} Controlled, See Notes 1 and 2)

Parameter	Symbol	6706BR-6		6706BR-7		6706BR-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	6	—	7	—	8	—	ns	
Chip Enable to End of Write	t_{ELWH} , t_{ELEH}	5	—	6	—	6	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	3	—	3.5	—	3.5	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

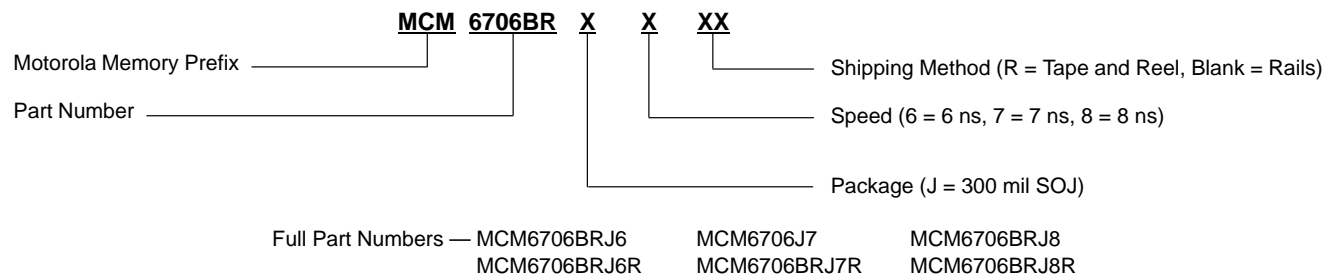
NOTES:

1. A write occurs during the overlap of \overline{E} low and \overline{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If \overline{E} goes low coincident with or after \overline{W} goes low, the output will remain in a high impedance condition.
5. If \overline{E} goes high coincident with or before \overline{W} goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2

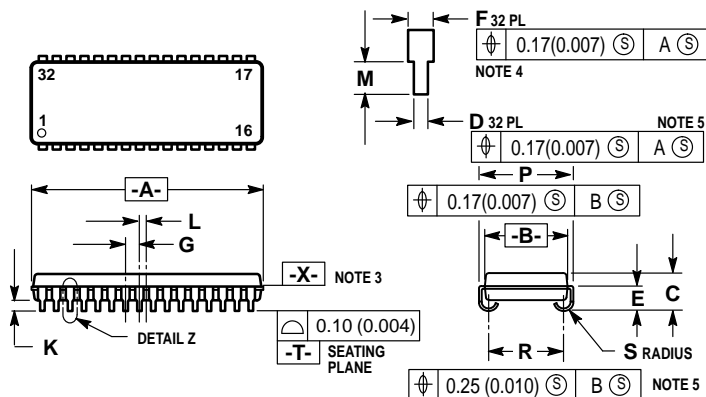


ORDERING INFORMATION (Order by Full Part Number)



PACKAGE DIMENSIONS


32-LEAD 300 MIL SOJ CASE 857-02



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DATUM PLANE -X- LOCATED AT TOP OF MOLD PARTING LINE AND COINCIDENT WITH TOP OF LEAD, WHERE LEAD EXITS BODY.
4. TO BE DETERMINED AT PLANE -X-.
5. TO BE DETERMINED AT PLANE -T-.
6. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
7. 857-01 IS OBSOLETE, NEW STANDARD 857-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.83	21.08	0.820	0.830
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.41	0.50	0.016	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
N	0.76	1.14	0.030	0.045
P	8.38	8.64	0.330	0.340
R	6.60	6.86	0.260	0.270
S	0.77	1.01	0.030	0.040

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