

Advance Information

512K Pipelined BurstRAM™ Secondary Cache Module for Pentium™

The MCM64PE64 (512KB) module is designed to provide a burstable, high performance, L2 cache for the Pentium microprocessor in conjunction with Intel's Triton II chip set. The MCM64PE64 is configured as 64K x 64 bits. It is packaged in a 160-pin card edge memory module. The module uses two 3.3 V, 64K x 32 BurstRAMs for the data RAMs and one 3.3 V, 32K x 8 FSRAM for the 8-bit tag RAM.

Bursts can be initiated with either address status processor (ADSP) or cache address status (CADS). Subsequent burst addresses are generated internal to the BurstRAM by the cache burst advance (CADV) input pin.

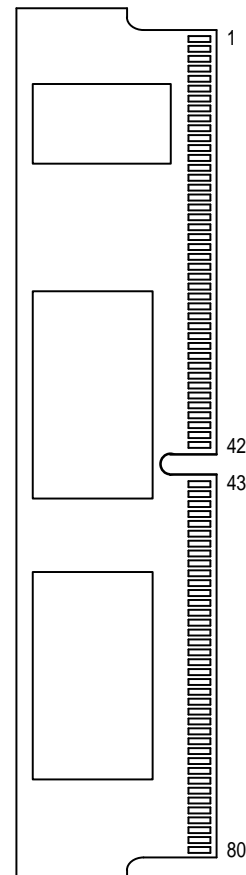
Write cycles are internally self timed and are initiated by the rising edge of the clock (CLK0) input. Eight write enables are provided for byte write control.

PD0 – PD3 map into the Triton II chip set for auto-configuration of the cache control.

- 8-Bit Cache Tag
- Pentium-Style Burst Counter on Chip
- Pipelined Data Out
- 160-Pin Card Edge Module
- Address Pipeline Supported by ADSP Disabled with Ex
- All Cache Data and Tag I/Os are TTL Compatible
- Three State Outputs
- Byte Write Capability
- Fast Module Clock Rate: 66, 75 MHz
- Fast SRAM Access Times: 12, 15 ns for Tag RAMs
7, 8 ns for Data RAMs
- One-Cycle Deselect Data RAMs
- Decoupling Capacitors for Each Fast Static RAM
- Single 3.3 V + 10%, – 5% Power Supply
- Burndy Connector, Part Number: CELP2X80SC3Z48
- Intel COAST 3.0 Option III Compliant

MCM64PE64


160-LEAD CARD EDGE
CASE TBD, TOP VIEW



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How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303-675-2140 or 1-800-441-2447

JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 4-32-1,
Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan. 81-3-5487-8488

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609
– US & Canada ONLY 1-800-774-1848

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

INTERNET: <http://motorola.com/sps>



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