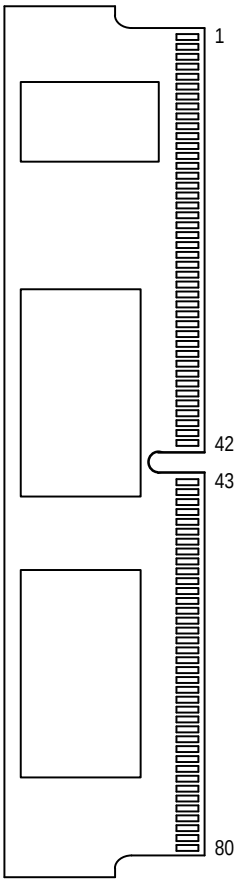
MCM64PE64

Advance Information

512K Pipelined BurstRAM™ Secondary Cache Module for Pentium™

160–LEAD CARD EDGE CASE TBD, TOP VIEW



The MCM64PE64 (512KB) module is designed to provide a burstable, high performance, L2 cache for the Pentium microprocessor in conjunction with Intel's Triton II chip set. The MCM64PE64 is configured as 64K x 64 bits. It is packaged in a 160–pin card edge memory module. The module uses two 3.3 V, 64K x 32 BurstRAMs for the data RAMs and one 3.3 V, 32K x 8 FSRAM for the 8–bit tag RAM.

Bursts can be initiated with either address status processor ($\overline{\text{ADSP}}$) or cache address status (CADS). Subsequent burst addresses are generated internal to the BurstRAM by the cache burst advance (CADV) input pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (CLK0) input. Eight write enables are provided for byte write control.

PD0 – PD3 map into the Triton II chip set for auto–configuration of the cache control.

- 8–Bit Cache Tag
- Pentium–Style Burst Counter on Chip
- Pipelined Data Out
- 160–Pin Card Edge Module
- Address Pipeline Supported by $\overline{\text{ADSP}}$ Disabled with $\overline{\text{Ex}}$
- All Cache Data and Tag I/Os are TTL Compatible
- Three State Outputs
- Byte Write Capability
- Fast Module Clock Rate: 66, 75 MHz
- Fast SRAM Access Times: 12, 15 ns for Tag RAMs
  7, 8 ns for Data RAMs
- One–Cycle Deselect Data RAMs
- Decoupling Capacitors for Each Fast Static RAM
- Single 3.3 V + 10%, – 5% Power Supply
- Burndy Connector, Part Number: CELP2X80SC3Z48
- Intel COAST 3.0 Option III Compliant

BurstRAM is a trademark of Motorola.
Pentium is a trademark of Intel Corp.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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