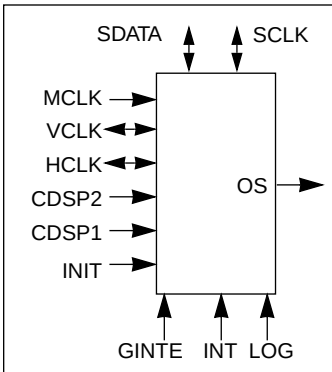
Order this document by MCM20007/D

MCM20007

Advance Information

1/4” Color CIF Image Sensor (A Series)

352 x 288 pixel progressive/interlace scan solid state image sensor



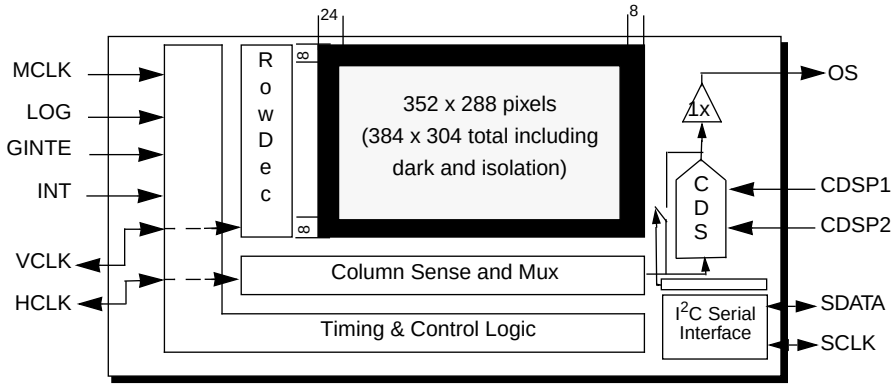
Features:

- CIF resolution, active CMOS image sensor with square pixel unit cells
- Patented pinned photodiode architecture
- Bayer-RGB color filter array with optional micro lenses
- High sensitivity and charge conversion efficiency
- High fill factor and quantum efficiency
- Low fixed pattern noise / Wide dynamic range
- Ultra low image lag and smear
- Antiblooming and continuous variable speed shutter (1/60sec to 1/15000sec)
- Integrated on-chip timing/logic circuitry
- On-chip CDS and scan mode selection
- Digitally programmable via I^2C serial interface
- Single 3.3V power supply
- 16 pin ceramic DIP package with glass window

Ordering Information	
Device	**Package**
MCM20007ID	16 CDIP

The MCM20007 is based on an active pixel design realized using sub-micron ImageMOS™ technology developed especially for imaging applications. The proprietary pinned photodiode process results in an excellent blue response. The quantum efficiency also exceeds that of comparable sensors in the red spectrum. Optional lenslet arrays can be added to improve the effective fill factor for higher sensitivity. Readout noise is minimized by using on-chip CDS. This, along with the low dark current of 0.2 nA/cm^2, optimizes the sensor dynamic range to 66 dB. The driver circuits for timing and control functions are integrated on-chip.

The sensor can be run by supplying a single Master Clock. The option for user supplied clocks is available. The sensor provides various user selectable options such as scan mode selection for full motion/still imaging, CDS on/off, and variable integration times. Either analog CDS or raw video signals are output via a 75Ω capable driver. Digitization can be done by Motorola’s MCM10005, among others. Given the excellent electro-optical performance, low power dissipation, and on-chip integration, Motorola’s image sensors and support devices are suitable for a variety of consumer applications including still/video imaging, scanners, security/ID systems, and automotive.



Feature	Value
Resolution	352 x 288 pixels
Pixel Size	7.8 µm x 7.8 µm
Image Size	2.7mm x 2.2mm
Readout Rate	10 MHz
Frame Rate	60 FPS
Vsat (w CDS)	1.0 V
Conv. Gain	13 µV/e
Fill Factor (max)	65%
Sensitivity	1.8 V/lux-sec
Avg. Col. FPN	0.17%
Dark Current	0.2 nA/cm^2
Dynamic Range	66 dB
Power Supply	3.3 V+/-10%

Figure 1. MCM20007 Simplified Block Diagram and Sensor Specifications.

This document contains information on a new product.
Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1] (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to 3.8	V
V_{in}	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	-0.5 to V_{DD} + 0.5	V
I	DC Current Drain per Pin, Any Single Input or Output	±50	mA
I	DC Current Drain, V_{DD} and V_{SS} Pins	±100	mA
T_{STG}	Storage Temperature Range	-65 to +150	˚C
T_L	Lead Temperature (10 second soldering)	300	˚C

[1] Maximum Ratings are those values beyond which damage to the device may occur.

$V_{SS} = AV_{SS} = DV_{SS} = V_{SSO}$ ($DV_{SS} = V_{SS}$ of Digital circuit, $AV_{SS} = V_{SS}$ of Analog Circuit)
$V_{DD} = AV_{DD} = DV_{DD} = V_{DDO}$ ($DV_{DD} = V_{DD}$ of Digital circuit, $AV_{DD} = V_{DD}$ of Analog Circuit)

RECOMMENDED OPERATING CONDITIONS (to guarantee functionality; voltage referenced to V_{SS})

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC Supply Voltage, V_{DD} = 3.3V (Nominal)	3.0	3.6	V
T_A	Commercial Operating Temperature	0	70	˚C
T_J	Junction Temperature	0	85	˚C

Notes:
- All parameters are characterized for DC conditions after thermal equilibrium has been established.
- Unused inputs must always be tied to an appropriate logic level, e.g., either V_{SS} or V_{DD}.
- This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than the maximum rated voltages to this high impedance circuit.
- For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V ± 0.3V; V_{DD} referenced to V_{SS}; T_a = 0˚C to 70˚C)

Symbol	Characteristic	Condition	T_A = 0˚C to 70˚C		Unit
			Min	Max	
V_{IH}	Input High Voltage		2.0	V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
I_{in}	Input Leakage Current, No Pull-up Resistor	$V_{in} = V_{DD}$ or V_{SS}	-5	5	µA
I_{OH}	Output High Current	V_{DD} = Min, V_{OH} Min = 0.8 * V_{DD}	-3		mA
I_{OL}	Output Low Current	V_{DD} = Min, V_{OL} Max = 0.4 V	3		mA
V_{OH}	Output High Voltage	V_{DD} = Min, I_{OH} = -100µA	V_{DD} - 0.2		V
V_{OL}	Output Low Voltage	V_{DD} = Min, I_{OL} = 100µA		0.2	V
I_{OZ}	3-State Output Leakage Current	Output = High Impedance, $V_{out} = V_{DD}$ or V_{SS}	-10	10	µA
I_{DD}	Maximum Quiescent Supply Current	I_{out} = 0mA, $V_{in} = V_{DD}$ or V_{SS}	0	15.0	mA

POWER DISSIPATION (V_{DD} = 3.0V, V_{DD} referenced to V_{SS}; T_a = 25˚C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
P_{DYN}	Dynamic Power	10 MHz MCLK Clock frequency		50		mW
P_{STDBY}	Standby Power	STDBY Pin Logic High		5		mW
P_{AVG}	Average Power	10 MHz Operation (using STDBY)		25		mW

MCM20007 MONOCHROME CMOS IMAGE SENSOR ELECTRO-OPTICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Notes
E_{sat}	Saturation Exposure		0.4		$\mu J/cm^2$	1
QE	Peak Quantum Efficiency (@550nm)		30		%	2
PRNU	Photoresponse Non-uniformity			0.3	% rms	3
PRNL	Photoresponse Non-linearity			1.0	%	
R_s	Photoresponsivity Shading			10	%	4

Notes:

1. For λ = 550 nm wavelength and N_{e^-sat} = 40 ke^-.
2. Refer to typical values from Figure 5, MCM20007 nominal spectral response.
3. For a 100 x 100 pixel region under uniform illumination with output signal equal to 80% of saturation signal.
4. This is the global variation in the chip output across the entire chip measured at 80% saturation and is expressed as a percentage ofthe mean pixel value.

MCM20007 COLOR CMOS IMAGE SENSOR ELECTRO-OPTICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Notes
E_{sat}	Saturation Exposure		0.6		$\mu J/cm^2$	1
QE_r	Red Peak Quantum Efficiency @ λ = 650 nm		12		%	2
QE_g	Green Peak Quantum Efficiency @ λ = 550 nm		20		%	2
QE_b	Blue Peak Quantum Efficiency @ λ = 450 nm		22		%	2
PRNU	Photoresponse Non-uniformity			1.0	% rms	3
PRNL	Photoresponse Non-linearity			1.0	%	
R_{gs}	Green Photoresponsivity Shading			10	%	4

Notes:

1. For λ = 550 nm wavelength and N_{e^-sat} = 40 ke^-.
2. Refer to typical values from Figure 5, MCM20007 nominal spectral response.
3. For a 100 x 100 pixel region under uniform illumination with output signal equal to 80% of saturation signal.
4. This is the global variation in the chip output across the entire chip measured at 80% saturation and is expressed as a percentage of the mean pixel value.

CMOS IMAGE SENSOR CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Notes
	Sensitivity	1000		1800	mV/lux-sec	
$N_{e\text{-}sat}$	Saturated Signal - V_{out}	35			ke^-	
V_{sat}	Output Saturation Voltage (w/o CDS gain)	350	450	550	mV	1, 2, 4
V_{sat}	Output Saturation Voltage (with CDS gain)	700	900	1100	mV	1, 2, 4
I_d	Photodiode Dark Current		0.2	0.5	nA/cm^2	
DS	Dark Signal				mV	
DSNU	Dark Signal Non-Uniformity (Entire Field)				mV	
CTE	Pixel Charge Transfer Efficiency		0.9995	0.9999	%	5
f_H	Horizontal Imager Frequency			10	MHz	
IL	Image Lag		negligible	0.25	%	
X_{ab}	Blooming Margin - shuttered light		200			3,4,6

Notes:
1. V_{sat} is the mean value at saturation as measured at the output of the device.
2. Measured at the sensor output.
3. X_{ab} represents the increase above the saturation-irradiance level (H_{sat}) that the device can be exposed to before blooming of the pixel will occur. It should also be noted that V_{out} rises above V_{sat} for irradiance levels above H_{sat}.
4. It should be noted that there is a trade-off between X_{ab} and V_{sat}.
5. Pixel transfer efficiency
6. No column streaking

Output Amplifier (V_{dd} = 3.3V, V_{ss} = 0V)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{odc}	Output DC Offset (Raw video mode)	0.5		1.1	V	1
V_{odc}	Output DC Offset (CDS video mode)	1.0		2.1	V	1
P_d	Power Dissipation	40	50	100	mW	
f_{3dB}	Output Amplifier Bandwidth	100			MHz	2
$\Delta V_o/\Delta N$	Sensitivity (at the Output)	10	13	15	$\mu V/e^-$	
OSNU	Output Signal Non-Uniformity @ 50% Saturation			0.5	%	
C_L	Off-chip Load		20	30	pF	3
	Latency			0.0	clock cycles	

Notes:
1. DC is between max to min of max output swing
2. With stray output load capacitance of 10 pF between output and AC ground
3. To meet max 10MHz video @ max 1.0p-p signal (CDS mode only)

GENERAL

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$n_{e^- total}$	Total Sensor Noise		TBD	30	e^- rms	1
DR	Dynamic Range	58	60	66	dB	2

Notes:
1. Includes amplifier noise, dark pattern noise and dark current shot noise at 20 MHz data rates.
2. Uses 20 log($N_{e^-sat}/n_{e^- total}$) where $N_{e\text{-}sat}$ refers to the vertical CMOS sensor saturation signal.

CMOS IMAGE SENSOR CHARACTERISTICS

Correlated Double Sampler (CDS)

Symbol	Parameter		Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		350	450	550	mV_{pp}
f_{max}	Maximum Input Pixel Frequency	MCLK is input			10	MHz
T_{pwCDS}	CDSP1 and CDSP2 Pulse Widths	Minimum	10		15/(16 x f_{MCLK})	ns
A_V	Amplifier Output Gain (fixed)				6.0 2.0	dB Voltage
C_{IN}	Input Capacitance	Includes Pad Capacitance			3.0	pF
	Latency				2.0	clock cycles

I^2C [6] SERIAL INTERFACE TIMING SPECIFICATIONS (see Figure 2)

Symbol	Characteristic	Min	Max	Unit
f_{max}	SCLK maximum frequency		100	KHz
M1	Start condition SCLK hold time	2	-	T_{MCLK}[7]
M2	SCLK low period	8	-	T_{MCLK}
M3	SCLK/SDATA rise time [from V_{IL} = (0.2)*VDD to V_{IH} = (.8)*VDD]	-	.3	µs[8]
M4	SDATA hold time	0	-	ns
M5	SCLK/SDATA fall time (from Vh = 2.4V to Vl = 0.5V)	-	.3	µs[8]
M6	SCLK high period	4	-	T_{MCLK}
M7	SDATA setup time	0	-	ns
M8	Start / Repeated Start condition SCLK setup time	2	-	T_{MCLK}
M9	Stop condition SCLK setup time	2	-	T_{MCLK}
C_I	Capacitive for each I/O pin	-	10	pF
Cbus	Capacitive bus load for SCLK and SDATA	-	200	pF
Rp	Pull-up Resistor on SCLK and SDATA	1.5	10	kΩ[9]

[6] I^2C is a proprietary Philips interface bus
[7] The unit T_{MCLK} is the period of the input master clock; The frequency of MCLK can vary between 3.125 MHz and 25 MHz
[8] The capacitive load is 200 pF
[9] A pull-up resistor to VDD is required on each of the SCLK and SDATA lines; for a maximum bus capacitive load of 200 pf, the minimum value of Rp should be selected in order to meet specifications

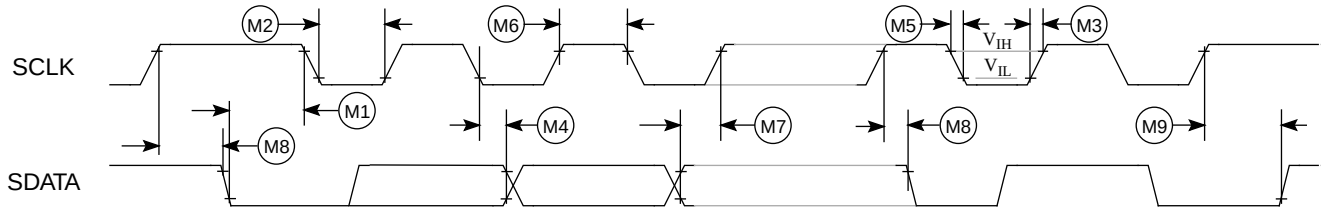


Figure 2. I^2C Bus Timing Diagram

Table 1. MCM20007 Pin Definitions

Pin No.	Pin Name	Description	Pin Type	Power
1	OS	Output Signal	O	
2	AVSS	Analog Ground	G	A
3	AVDD	Analog Power	P	A
4	CDSP1	CDS Reference Sample Pulse	I	
5	CDSP2	CDS Signal Sample Pulse	I	
6	INT	Pixel Integrate (SFCM)	I	
7	LOG	Lateral Overflow Gate	I	
8	GINTE	Global Integration Enable (SFCM)	I	

Pin No.	Pin Name	Description	Pin Type	Power
9	SCLK	Serial Clock	I/O	D
10	SDATA	Serial Data	I/O	D
11	INIT	Sensor Initialize	I	
12	HCLK/ SOF	Pixel Clock/Start of Frame	I/O	
13	VCLK	Vertical Clock	I/O	
14	MCLK	Master Clock	I	
15	DVSS	Digital Ground	P	D
16	DVDD	Digital Power	G	D

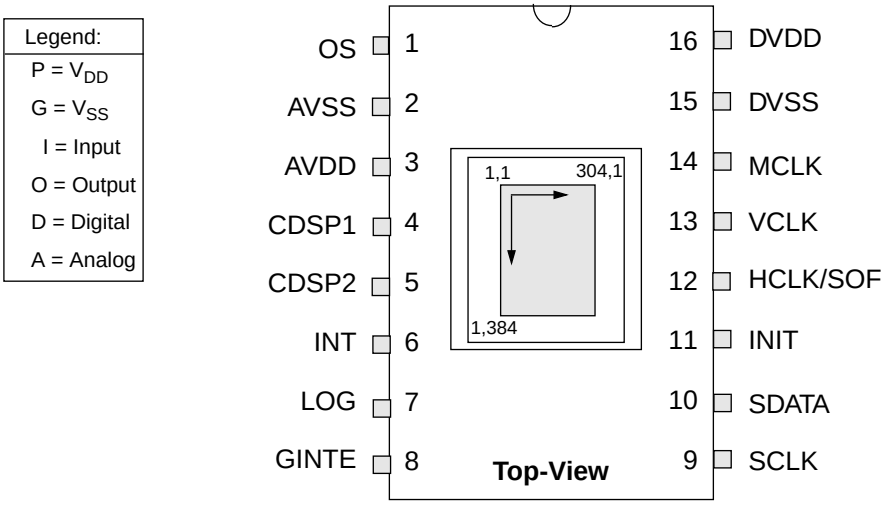


Figure 3. MCM20007 Pinout Diagram

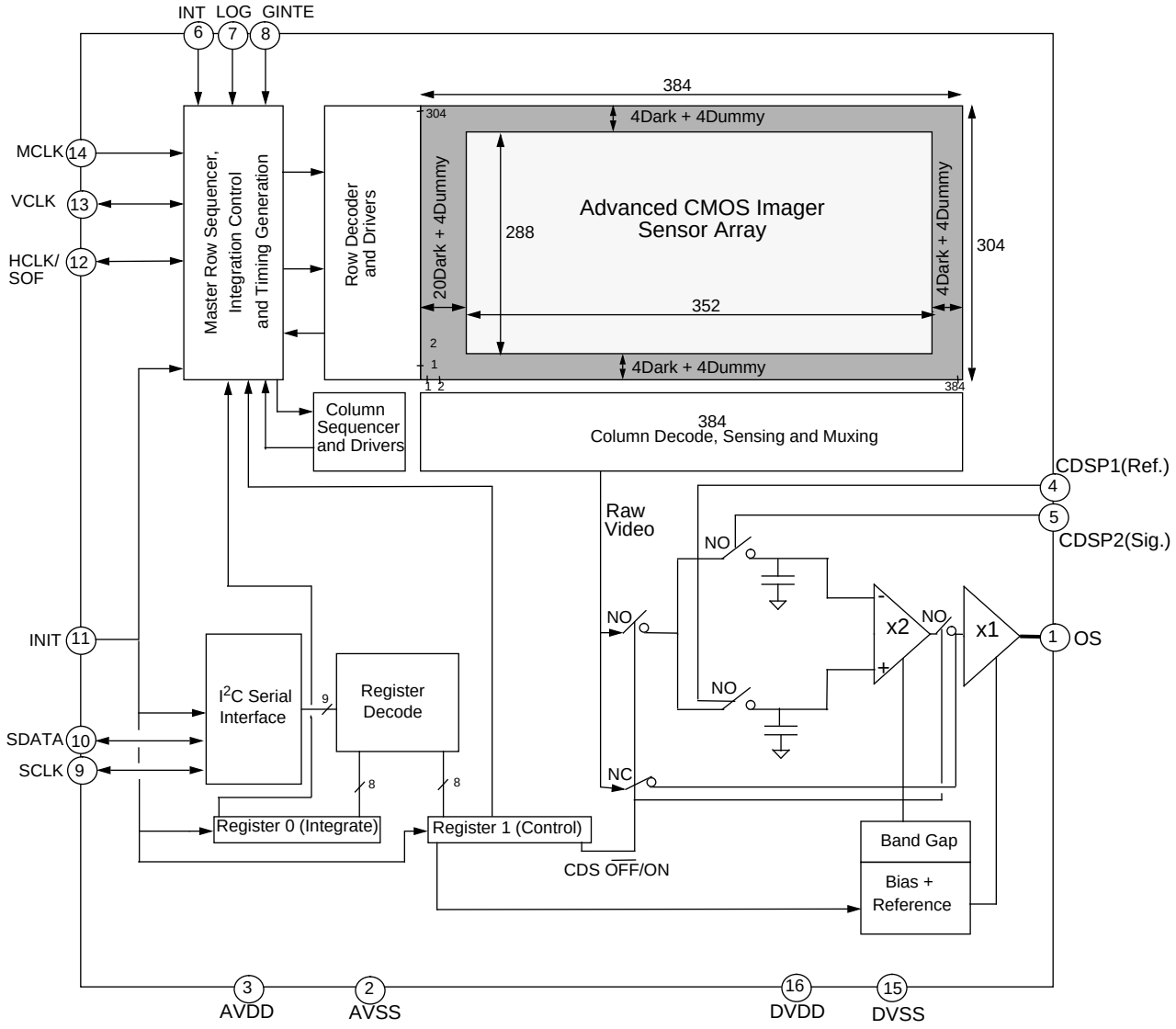


Figure 4. MCM20007 Detailed Block Diagram

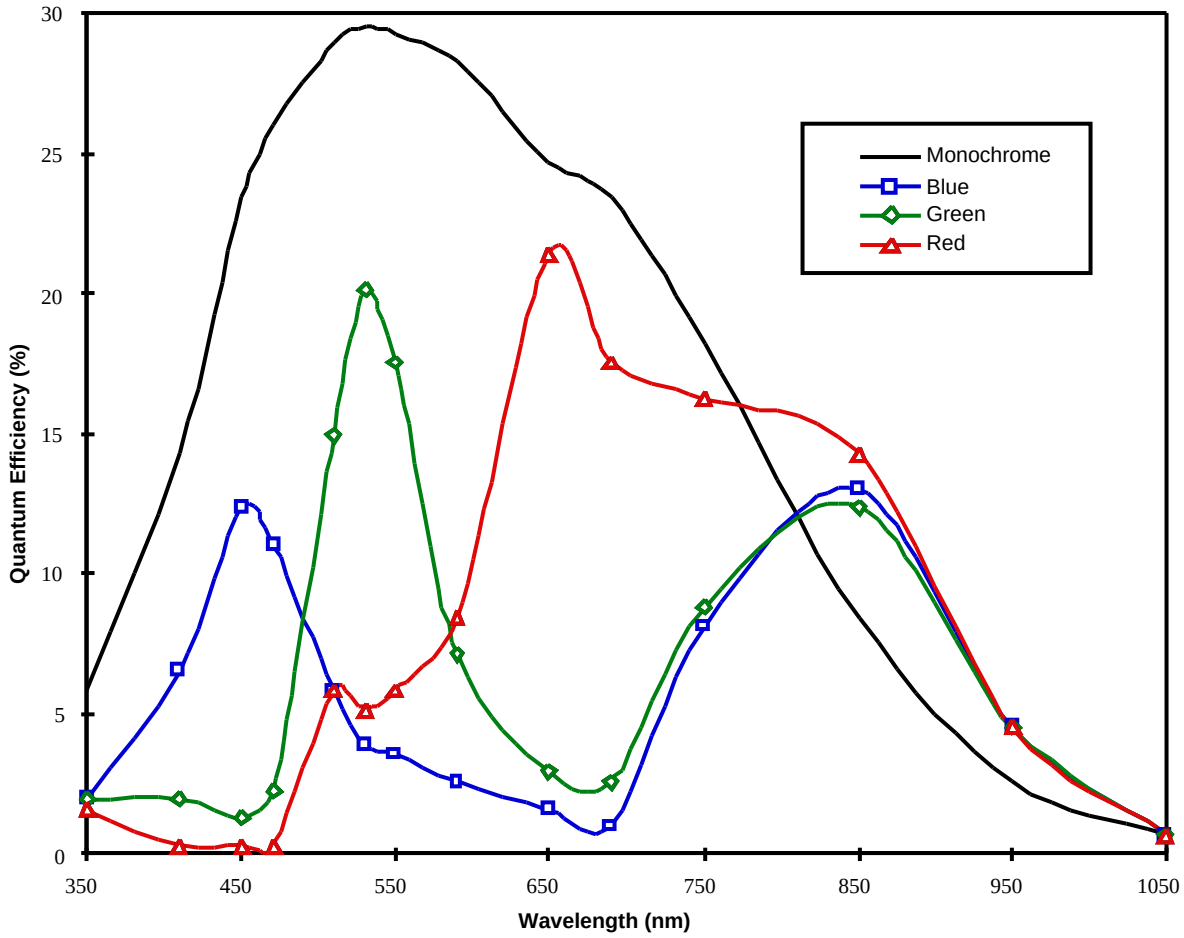


Figure 5. MCM20007 Nominal spectral response

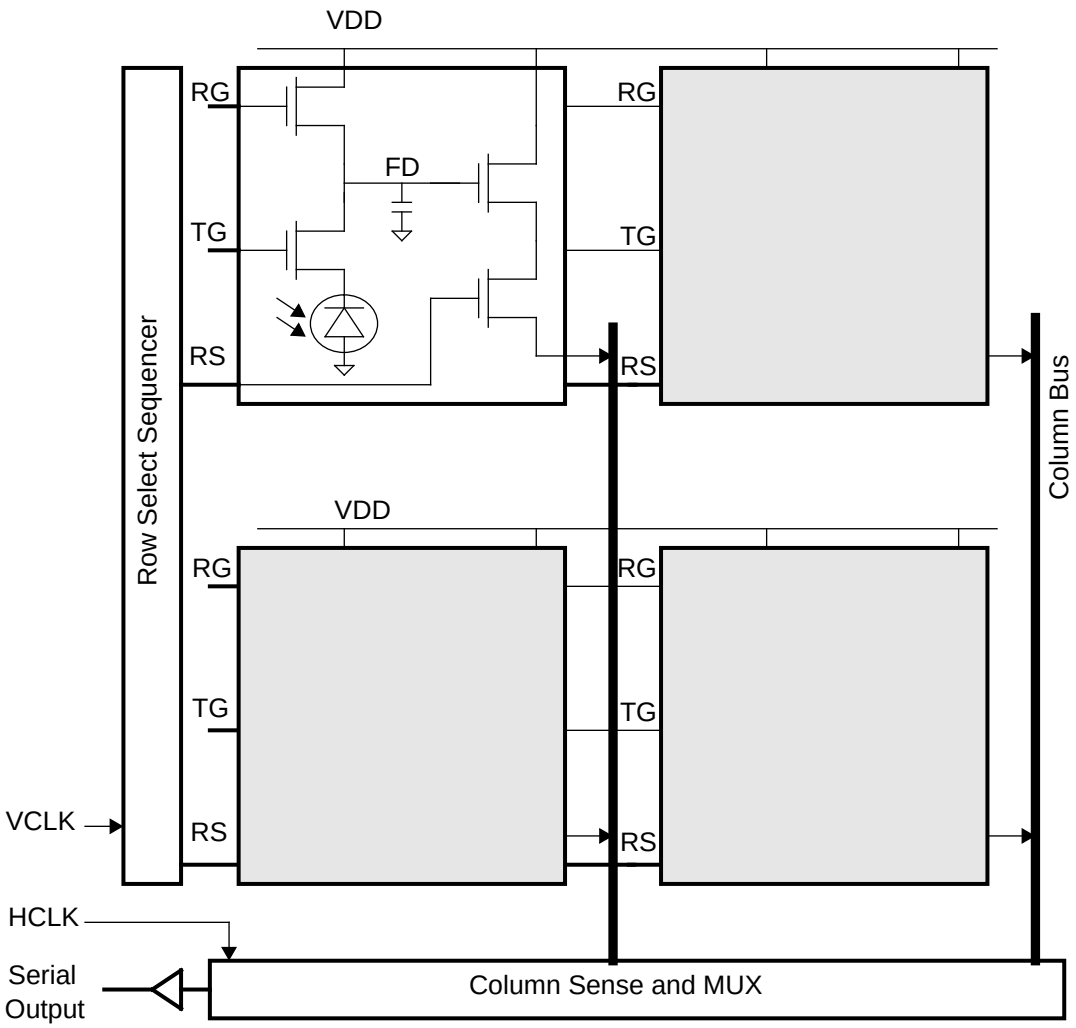


Figure 6. Pixel architecture, shown as an example a 2x2 array. The RG, TG, and RS signals are common per row. Each column shares a common column bus.

1.0 MCM20007 Sensor Family Overview

The MCM20007 sensor family comprises a 1/4" format CIF active pixel sensor which supports both progressive and interlaced scan readout modes. A user selectable on-board correlated double sampler (CDS) is available for noise suppression. The sensor family is available with optional Color Filter Arrays (CFAs) and/or micro lenses for enhanced sensitivity. This device is an ideal solution for monochrome and color consumer applications in still imaging or real time video which demand high sensitivity, low noise, wide dynamic range, low lag and smear. All with low power dissipation in a competitively priced solution.

The active pixel sensor array consists of a 352 x 288 array of pixels. In addition there are dark and dummy pixels bringing the total number of pixels to 384 x 304. Please refer to Figure 4 for placement of dark and dummy pixels. The dummy pixels are photoresponsive but are not a part of the active frame.

The output signal for a selected pixel can be processed through an analog signal processing pipeline to improve device sensitivity and performance. The resulting raw

analog or CDS analog video is directly compatible with 3.3V systems.

The sensor can be run by supplying a single master clock or the user can supply appropriate VCLK and HCLK sync signals. For a fully flexible operation the user may program the timing and control functions of the MCM20007 through a standard I^2C serial interface. This allows control over shuttering mechanisms, exposure time, CDS blocks, and scan readout type, i.e. progressive/interlaced.

The result is an extremely flexible, single chip solution to the digital image capture problem for imaging applications. It allows the system designer to achieve reduced component count, board space and system cost. Because the chip is designed for 3.3V operation, a wide variety of low power, portable applications may be addressed for consumer applications.

2.0 Pixel Architecture

The MCM20007 ImageMOS^{TM} (1) sensor comprises a 352x288 active pixel array and supports both progressive and interlaced scan readout modes. The basic operation of the pixel relies on the photoelectric effect where by due to its physical properties silicon is able to detect photons of light. The photons generate electron-hole pairs in direct proportion to the intensity and wavelength of the incident illumination. The application of an appropriate bias allows the user to collect the electrons and meter the charge in the form of a useful parameter such as voltage.

The pixel architecture is based on a four transistor (4T) Advanced CMOS Imager^{TM} (2) pixel which requires all pixels in a row to have common Reset, Transfer, and Row Select controls. In addition all pixels have common supply (V_{DD}) and ground (V_{SS}) connections. An optimized cell architecture provides enhancements such as noise reduction, fill factor maximizations, and anti-blooming. The use of pinned photodiodes (3) and proprietary transfer gate devices in the photoelements enables enhanced sensitivity in the entire visual spectral range and a lag free operation.

In its simplest mode of operation the process of acquiring an image can be described as follows. The start of an integration period is marked by the turning OFF of the Transfer Gate (TG). In order to enable antiblooming the Reset Gate (RG) is turned ON at the same instant or before. The photoelement which is a fully depleted pinned photodiode starts to collect electrons generated by the incident light. During this period if the photoelements' capacity is reached, any excess photo generated electrons will be removed by the means of an antiblooming structure. The end of the integration period is marked by the turning ON of the transfer gate whereby the charge collected is transferred to a floating diffusion (FD) node in preparation for conversion into a more useful quantity, namely voltage. However, prior to this transfer it is important to set the FD node level to a known reference. This is automatically achieved by leaving RG ON during integration to enable antiblooming. The FD node is set to the VDD potential and RG is turned OFF prior to pixel transfer into the FD node. Since RS is ON, the reset reference level is sampled and held in the horizontal readout circuit with a pulse on SHR (Sample and Hold Reset) refer to Figure 7 and Figure 12. Once TG is turned ON the signal level is sampled and held in the horizontal readout circuit by pulsing SHS (Sample and Hold Signal) refer to Figure 7 and Figure 12. The FD node is essentially a capacitor, once the photon generated electrons are transferred to this capacitor, the voltage across it drops from the reset level in proportion to the transferred charge ($dV=dQ/C_{FD}$). As can be inferred, the capacitance of this node is kept reasonably small (fF) to enable it to detect small charge packets. The change in the voltage across the floating diffusion capacitor is observed through a source follower buffer hence a voltage proportional to the charge transferred into the floating diffusion is produced. Applying the appropriate Row Select (RS) and Column Select (CS) signals, all pixels in the x-y array are addressed to reconstruct an electronic representation of the incident image. Once a pixel has been read out, preparation for the acquisition of the next frame can begin in the manner described above.

In addition to the imaging pixels, there are additional pixels called dark and dummy pixels at the periphery of the imaging section (see Figure 4). The dark pixels are covered by a light blocking shield rendering the pixels underneath insensitive to photons. These pixels provide the user means to measure the intrinsic pixel noise and dark current levels which should then be subtracted from the video measured in the imaging pixel.

The dummy pixels are provided at the array's periphery to eliminate inexact measurements due to light piping into the dark pixels adjacent to active pixels. The output of these pixels should be discarded.

1. ImageMOS is a Motorola trademark
2. Advanced CMOS Imager is a Kodak trademark
3. Patents held jointly by Motorola and Kodak

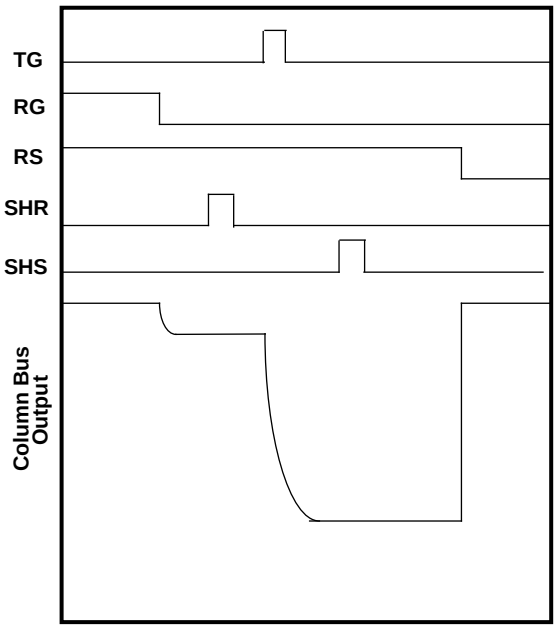


Figure 7. Pixel output as seen on the column bus when appropriate row (RS) is selected. Above timing is only an illustration. The pixel can be readout in other ways.

The MCM20007 family is offered with the option of monolithic polymer color filter arrays (CFAs). The combination of an extremely planarized process and proprietary Kodak color filter technology result in CFAs with superior spectral and transmission properties. The standard option is a primary (RGB) “Bayer” pattern (see Figure 8), however, facility to produce customized CFAs including complementary (CMYG) mosaics also exists. Depending on the application, the choice between primary or complementary filter mosaics should be made. In general, primary mosaics are used in still video while complementary are used in real time video applications.

Applications requiring higher sensitivity can benefit from the optional micro-lens arrays shown in Figure 9. The lenslet arrays can improve the fill factor (aperture ratio) of the sensor by 1.5-2x depending on the F number of the main lens used in the camera system. Microlenses yield greatest benefits when the main lens has a high F number. As a caution, unoptimized F numbers can lead to optical aberrations, hence care should be taken when incorporating microlens equipped imagers into camera systems/heads. The fill factor of the pixels without microlenses is 35%.

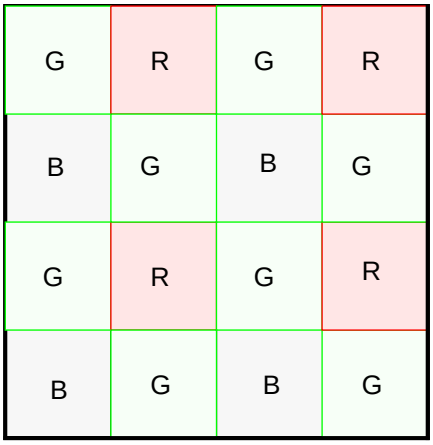


Figure 8. Optional on-chip Bayer CFA

Electronic shuttering, also known as electronic exposure timing in photographic terms, is a standard feature available on the sensor. The sensor frame rate and the image integration time (T_{int}) will both be multiples of the master clock frequency (MCLK). As an example, if the sensor MCLK is run at 7.6 MHz, the time required to read a full frame (1/MCLK*total #of columns*total # of rows) yields a frame rate of 60fps. The integration time of the sensor can now be varied from a maximum of 1/60sec to a minimum of 1/15360sec with T_{int} being controlled by an 8-bit register, hence 256 steps are available. A variable integration time will not effect the chosen frame rate which can only be varied by changing MCLK. This feature can be especially useful in situations such as imaging of fast moving objects where maximum available integration time is long enough to cause smear or blurring or when imaging a bright scene where there are enough photons to cause an early saturation of the pixel.

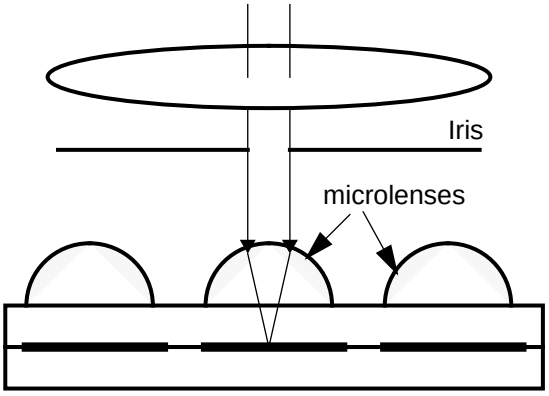


Figure 9. Improvement in pixel sensitivity results from focusing incident light on photo sensitive portions of the pixel by using microlenses.

3.0 Frame Capture Modes

Depending on the application the user may choose between the two available Frame Capture Modes (FCMs). An overview of the operation of the two modes and suggested guidelines for selection are given in this section.

By default the sensor starts up in the Continuous Frame Capture Mode (CFCM). This mode is most suitable for full motion video capture and will yield frame rates up to 80 fps at 10 MHz MCLK. In this mode the image integration and row readout take place in parallel. While a row of pixels is being integrated, another row is being readout. Since T_{int} is equal for all rows, the start of the integration periods for rows is staggered out. This mode relies on the integration periods of the rows being long enough to produce a reasonable overlap of the sequential rows. If this is not the case then image artifacts may be produced in instances where the target is moving very fast or the illumination is varying.

Antiblooming is controlled by on-chip logic in the CFCM and is always enabled. Electronic shuttering controls were explained in the previous section.

The second available capture mode is called Single Frame Capture Mode (SFCM). This mode consists of global integration of all pixels, next a simultaneous transfer to the FD node of all pixels followed by a sequential read out of all rows takes place. This mode is best suited for still or “single snap shot” capture of an image. In other situations this mode may be used for capturing moving pictures at very low frame rates. Examples also include random sampling of very fast moving video in web applications, conditions with varying illumination. A key point to remember is that SFCM is best used for snap shot imaging even though continuous motion capture is possible in this mode. The SFCM is completely controlled by the user who first selects the mode via the programmable serial interface. Inputs to the pins labelled Global Integrate Enable (GINTE), Lateral Overflow Gate (LOG), and Integrate (INT) also have to be provided (in CFCM these are generated on-chip). The GINTE is an active HIGH input, it prepares the sensor to start integration. LOG enables antiblooming, its bounds define the period antiblooming is in effect. The bounds of the INT pulse define the actual integration time i.e. the time the Transfer gate (TG) is OFF and photocharge is integrated in the photoelement. Pixel control signals in SFCM are illustrated in Figure 10. T_{EC} and T_{INT} represent the time exposure control and pixel integration are enabled. Again the user has complete flexibility in assigning values to these parameters however, recommended overlaps of T1 through T3 in Figure 10 should be followed for proper operation. The falling edge of GINTE represents the end of an integration/pixel transfer cycle. Another frame capture, however, cannot begin until all pixels have been scanned out. Once this cycle is complete, The GINTE pulse can be turned HIGH immediately or as when required.

Regardless of the frame capture mode the vertical transfer clock (VCLK) and the horizontal readout clocks (HCLK) can be generated on-chip or if desired supplied by the user via the VCLK and HCLK pins.

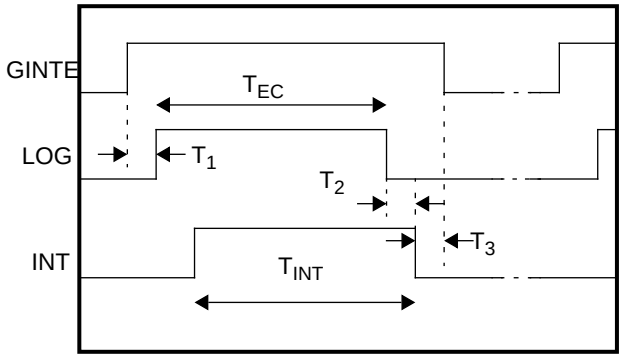


Figure 10. User supplied timing signals in SFCM. Minimum recommended timing parameters T1>1 ns, T2>1 ns, T3>1/f_{MCLK}. For synchronous applications to simplify timing, T1, T2, T3 may be made equal to 1/f_{MCLK}.

Selection of internally generated VCLK and HCLK or externally supplied clocks can be made through the serial interface. The default mode is to use internally generated clocks allowing the user to operate the chip by supplying a single MCLK. In this mode either the VCLK and HCLK or VCLK and Start of Frame (SOF) are available for monitoring by the user.

4.0 Column Readout and Mutiplexing

The ImageMOS image sensor relies on a modular circuit architecture (see the column schematic in Figure 12) to implement a novel column readout. Each column in the imaging array has an active load to provide the biasing current. In addition, each column has two sample and hold capacitors to store the reference and the signal outputs of individual pixels. These levels are subsequently used in the CDS block explained in the next section. The columns or “bit-line” are grouped in blocks of 64. The outputs of 6 such blocks are multiplexed and buffered before connecting to the CDS block. The MUX block reads out pixels of a given row serially, resembling the output format of a CCD.

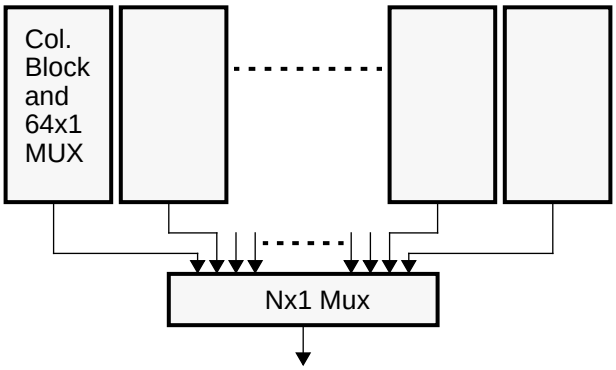


Figure 11. Conceptual illustration of multiplexing scheme for sensor readout.

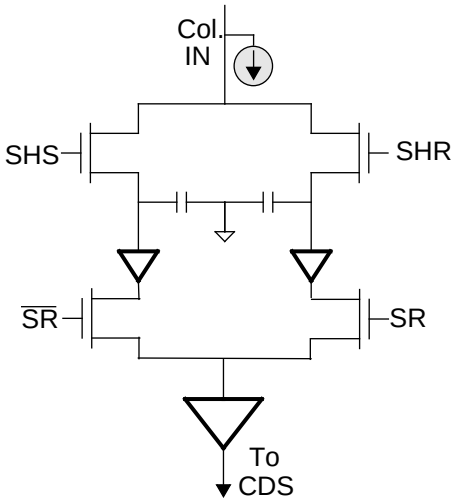


Figure 12. SHS, SHR, SR, and $\overline{SR}$ signals are generated internally on the chip.

5.0 High Speed Correlated Double Sampling

The uncertainty associated with the reset action of a capacitive node results in a reset noise which is equal to kTC; C being the capacitance of the node, T the temperature and k the Boltzmann constant. A common way of eliminating this noise source in all image sensors is to use Correlated Double Sampling. The output signal is sampled twice, once for its reset (reference) level and once for the actual video signal. These values are sampled and held and a difference amplifier subtracts the reference level from the signal output. Double sampling of the signal eliminates any noise sources which bear correlation.

In its default mode of operation the CDS block is bypassed by the video chain and the sensor output consists of raw analog video received via the unity gain buffer. In this mode the output signal contains both reset and signal levels per pixel period. The sensor output is 550mV p-p max.

In order to activate the CDS function the user must first set the CDS ON bit via the serial interface, next appropriate clocks at the pins labelled CDSP1 and CDSP2 must be supplied. With CDS selected, the sensor output will contain only the signal information. The CDS stage also incorporates a 2x gain stage hence its peak to peak output can reach a maximum of 1100 mV shown in Figure 14.

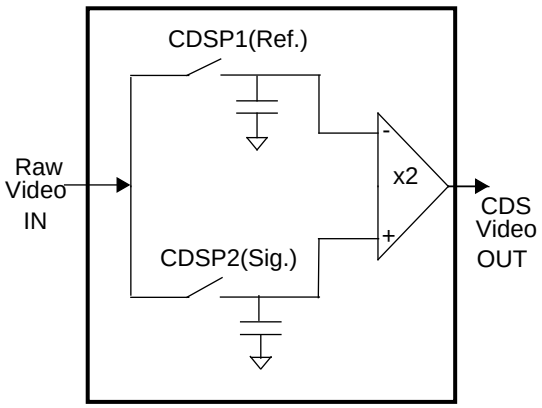


Figure 13. Conceptual block diagram of CDS implementation.

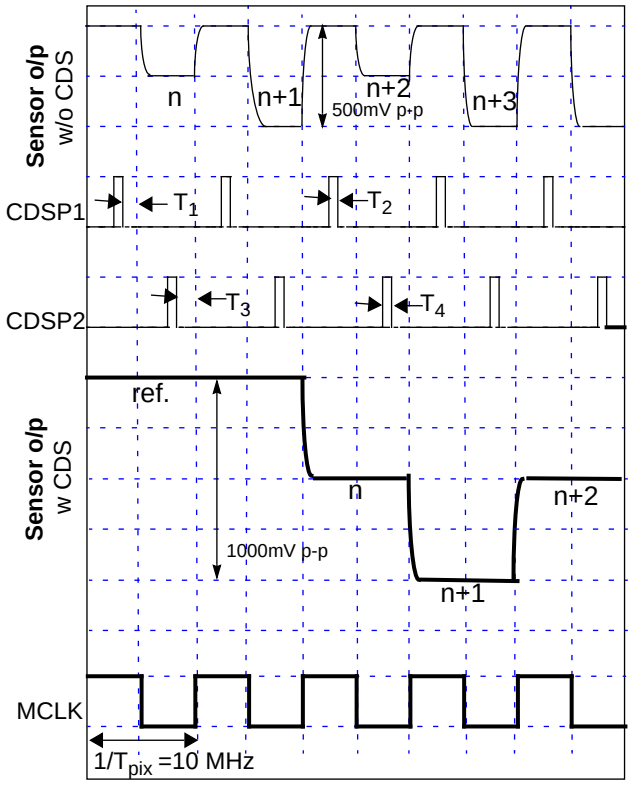


Figure 14. Sensor output with CDS and without (raw video) CDS. Minimum recommended overlaps: T1>2ns, T2=10ns, T3>2ns, T4=10ns. Note the different latency in the Raw and CDS video (Raw=0 clock cycles; CDS=2 clock cycles).

6.0 Output Buffer

The output amplifier is a unity gain buffer capable of driving an AC coupled 75Ω matched line or a 30 pF load. The amplifier employs feedback techniques to ensure accuracy of 1x gain. The drive level of the amplifier will not require the use of an external buffer(i.e. emitter follower) as in the case of many CCD imagers. Direct coupling is possible when interfacing to 3.3V level analog signal processors or ADCs. If not, AC coupling would be required.

7.0 Utility Register Programming

The MCM20007 utilizes an I^2C interface serial interface to program chip control codes for the utility registers. On chip selections that can be made via this interface include integration time duration, interlace/progressive scan mode, CFCM/SFCM frame capture modes, CDS on/off, user/on-chip timing clocks for VCLK and HCLK, and choice between clocks available to monitor.

All control data and addresses are programmed into the MCM20007 via the I^2C interface, MSB to LSB, with the address byte preceding the programming control data. Control data packet width may vary, but it is always input in byte-wide increments. Table 2 shows the memory map of the addresses for selecting the programmable registers. There are 8 bits of data associated with each register.

Table 2. Programmable Control Register Memory Map

Address	Register Function
00h	R(0): Integration Register
01h	R(1): Operation Mode Control Register

The INIT input pin is used to initialize the sensor to assure controlled chip and system startup. Control is asserted via a logic HIGH input. This should be held high for a minimum of eight MCLK cycles to insure all start up and initialization cyles are completed.

There are two programmable registers in the sensor. Register(0) allows the user to select the integration time (see Table 3). Register(1) allows control of all other parameters stated earlier (see Table 4). The image integration time of the sensor can be controlled in 256 steps from a minimum of 1/256 frame time to a maximum of 1 frame time. The frame time is controlled by the MCLK frequency and can be calculated as shown in the example in section 2.0. After selecting the appropriate register, the following eight inputs on the SDATA pin are used to set the integration period as shown in Table 3.

Table 3. Utility Register(0) programming addresses select integration time

Register Function (Integration time)	Register Address							
	D7	D6	D5	D4	D3	D2	D1	D0
1/256 T	0	0	0	0	0	0	0	1
2/256 T	0	0	0	0	0	0	1	0
255/256 T	1	1	1	1	1	1	1	1
256/256 T	0	0	0	0	0	0	0	0

Note that 1/256 T is equivalent to 2*Line Time, where the time required to readout a line (row) is ($1/f_{M\text{-}CLK}$*424). The longest integration time a sensor can have is equal to the time required to readout all rows (304) hence a register address equivalent to 152/256 T

yields the maximum integration time available at given MCLK frequency. Programming addresses beyond 152 through 256 will not result in any further increase of Tint.

Programming for Register(1) which controls the various operation modes of the sensor can be done by selecting programming addresses shown in Table 4. The clock monitor function (D1) allows the user to monitor the on-chip clocks generated. It is a convenient way of synchronizing signals for frame grabbing. The vertical clock (VCLK) is always available at the sensor VCLK pin, however, the data selection on the D1 bit gives the user the choice to monitor either the horizontal clock (HCLK) or the Start Of Frame (SOF) on the sensor's HCLK pin. The clock monitor is active only if the appropriate input is given to the register's D0 address bit. The scan mode selection can be done by addressing bit D4. The two most widely used scanning modes are interlaced scanning and progressive scanning. Solid state sensors designs are dedicated to specific scanning modes, although with progressive scan sensors it is possible to deliver interlaced information. Interlacing is a technique used in TV systems used to enhance the vertical resolution of the picture without increasing the bandwidth of the transmission system. A spatial offset is introduced on the display system between the odd and even fields. An odd field consists of rows 1,3,5,7,9.... while an even field comprises rows 2,4,6,8..... Since the spatial offset is exactly half the vertical pitch of the sensor, the even and odd fields appear interdigitated when displayed on top of one another, thus appearing to improve the sensor's vertical resolution. By definition two interlaced fields comprise a frame. The other scanning mode is called progressive scanning. It refers to non-interlaced or sequential row by row scanning of the entire sensor in a single pass. The image capture happens at one instant of time. In contrast, interlaced video captures fields sequentially in time. Any nominal movement between fields in interlaced video can cause smear and/or serrations to appear in the image in interlaced mode.

Table 4. Utility Register(1) programming addresses

Register Address	Value	Function Select
D7	0	Reserved for future use
	1	Invalid input
D6	0	Reserved for future use
	1	Invalid input
D5	0	Power ON
	1	STDBY/Power save mode
D4	0	Progressive scan mode
	1	Interlace scan mode
D3	0	Continuous Frame Capture Mode (CFCM)
	1	Single Frame Capture Mode (SFCM)
D2	0	CDS OFF
	1	CDS ON
D1	0	Clock monitor: VCLK and SOF
	1	Clock monitor: VCLK and HCLK
D0	0	On chip clock generation enabled
	1	User generated timing for VCLK and HCLK

The serial interface may be used to reprogram the integration register (R(0)) at any time during the sensor operation. However, the changes take effect only at the beginning of the next frame. The contents of the operations register (R(1)) should not be changed while a frame integration/readout is in progress.

8.0 Detailed Sensor Clocking

The sensor can be operated in a total of eight modes in both interlaced and progressive scan modes. These are outlined in Table 5. All input clocks are 3.3V digital inputs. Maximum input pin loading is 10pF.

A number of timing blocks and clock relationships have been illustrated in previous sections. This section begins with an illustration of OPT1 i.e. Continuous Frame Capture Mode (CFCM) with user supplied VCLK and HCLK and no CDS selected.

Table 5. Various available timing options

OPT	Image Capture Mode	VCLK, HCLK Timing Generation	CDS
1	CFCM	User supplied	OFF
2	CFCM	User supplied	ON
3	SFCM	User supplied	OFF
4	SFCM	User supplied	ON
5	CFCM	on-chip	OFF
6	CFCM	on-chip	ON
7	SFCM	on-chip	OFF
8	SFCM	on-chip	ON

The VCLK enables the transfer of the integrated photocharge to a floating diffusion node by triggering in sequence the in-pixel control signals explained in section 2.0. The charge transfer to the FD node and storage of the reference/signal levels on the column circuitry is initiated by the rising edge of the VCLK pulse. The entire process is completed in 39 MCLK cycles at which time the readout via the HCLK clocks starts. This is accomplished by 385 HCLK pulses to read the 384 columns of the CIF sensor (one additional clock used to reset internal chip counters during readout). The readout scheme is similar in operation to a CCD which has a parallel to serial transfer from the imaging pixels followed by a horizontal CCD readout.

Once the entire row has been transferred and sample and held in the column circuitry, the pixel will be left in reset state (TG/ RG HIGH - see section 2.0 for details). Since the sensor is operating in the continuous frame capture mode, the sensor will have started integrating on another row while the present row is being read. The offsets governing which row starts integration will be internally set by the sensor once the appropriate integration time has been selected through the serial interface. A point to note is that the user supplies the next VCLK. In case the arrival of this pulse is not optimized with respect to the pixel integration time, the pixel may reach its saturation capacity early on. Any further charge will be drained away by the antiblooming structure of the pixel.

Since CDS is OFF in this option, the inputs to the CDSP1 and CDSP2 pins should be driven LOW and the sensor output will be raw video with no inherent clock latency.

GINTE, LOG, and INT inputs are needed only in the single frame capture mode, hence the inputs to the respective pins should also be driven LOW.

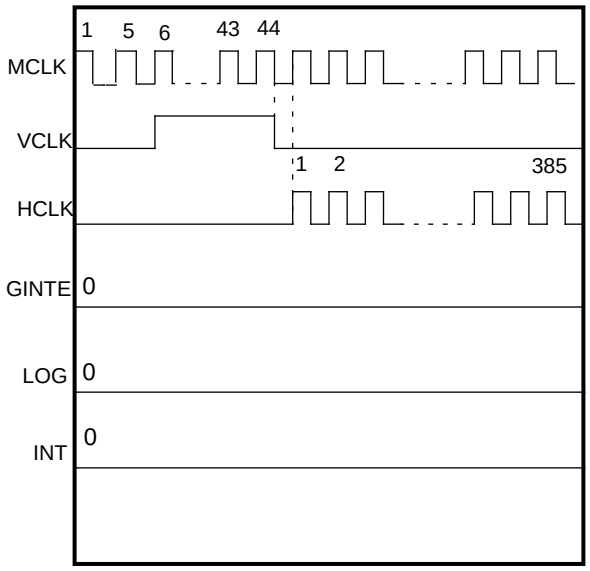


Figure 15. Input clocks for OPT1 mode (Table 5)

For this frame capture mode if a CDS output is desired, then the CDSP1 and CDSP2 should be supplied. Details are given in section 5.0. All other clocks will remain as shown in Figure 15. Note that the introduction of this additional signal processing chain produces a latency of 2 MCLK time periods in arrival of the output video. This will be true for all CDS outputs regardless of the frame capture modes (CFCM or SFCM).

The single frame capture mode (SFCM) relies completely on the user to supply the control signals for start and end of integration periods. In addition, as in the modes discussed before, the user has the choice of supplying the vertical and horizontal readout clocks or use those generated on-chip.

The relationship between GINTE, LOG, and INT was explained in section 3.0 and illustrated in Figure 16. For the sensor operation outlined in OPT3 once GINTE (refer to Figure 10) goes LOW, the normal readout cycles of VCLK and HCLK can begin. However, all pixels have to be read out before another frame integration can begin. Hence there will be 304 VCLK/HCLK cycles to readout a frame.

After a frame has been read out all pixels will remain in a reset state until the next GINTE triggers another frame integration. Once again, to obtain a CDS output (OPT4) follow instructions given in section 5.0 relating to the CDSP1 and CDSP2 input clocks.

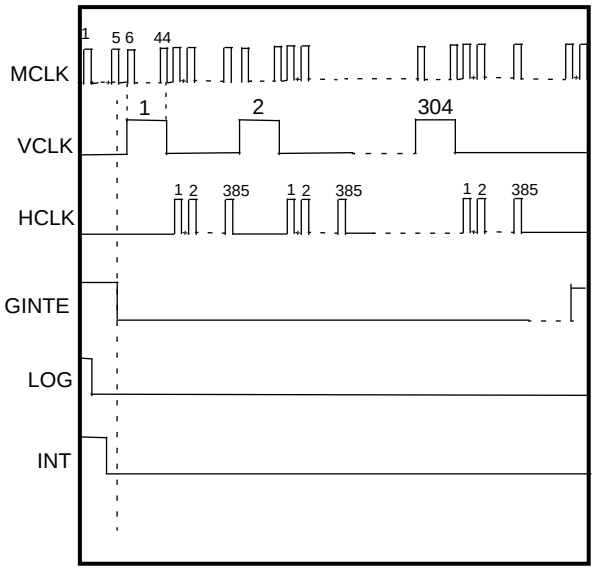


Figure 16. Input clocks for OPT3 mode (Table 5)

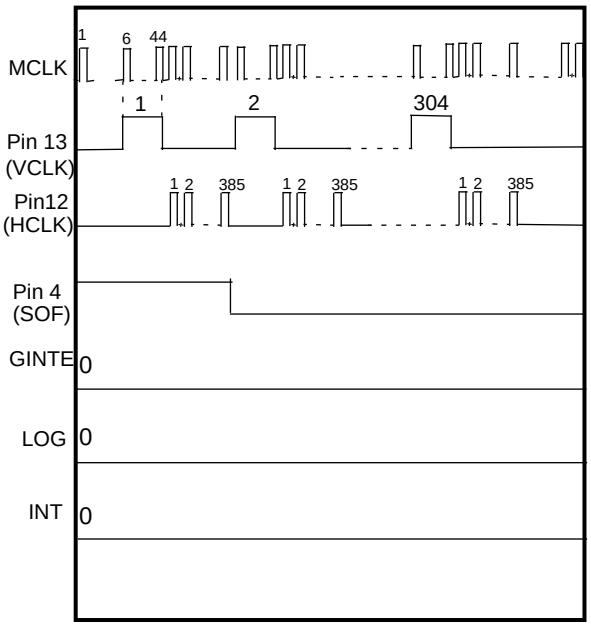


Figure 17. Only MCLK input is required for OPT5 mode. Clock monitor outputs on pins 12 and 13 are shown.

If the user selects the on-chip timing generation option for VCLK and HCLK, the timing becomes further simplified. The sensor can be made to operate with a single MCLK and output raw video signals. Such a mode of operation makes the MCM20007 especially attractive compared to various other imaging sensors (including CCDs) that are commercially available.

The user selects the clocks that are available to monitor by programming the serial interface. In this mode the VCLK and HCLK pins become output pins instead of inputs.

The OPT5 mode of operation requires only an MCLK input, all other timing and control signals are generated on-chip. The outputs on the VCLK and HCLK clock monitors are shown in Figure 17. Sensor output frame rates are determined by the MCLK frequency and the pixel integration time is controlled by the integration register (R0).

In order to obtain a CDS output while in the CFCM/on-chip clock mode (OPT6) the appropriate inputs to the CDSP1 and CDSP2 should be supplied.

The SFCM capture mode with on-chip clocks will generate monitoring clocks similar to those shown in Figure 16. The user supplies the integration clocks (GINTE, LOG, INT). The falling edge of the GINTE clock input, triggers a readout cycle. As before a CDS output is obtained with required inputs of CDSP1 and CDSP2 clocks.

9.0 I^{2}C Register Programming

The I^{2}C is an industry standard which is also compatible with the Motorola bus (called M-Bus) that is available on many microprocessor products. The I^{2}C contains a serial two-wire half-duplex interface that features bidirectional operation, master or slave modes, and multi-master environment support. The clock frequency on the system is governed by the slowest device on the board. The SDATA and SCLK are the bidirectional data and clock pins, respectively. These pins are open drain and will require a pull-up resistor to VDD of 1.5 KΩ to 10 KΩ (see page 5).

The I^{2}C is used to write the required user system data into the Program Control Registers in the MCM20007. The I^{2}C bus can also read the data in the Program Control Register for verification or test considerations. The MCM20007 is a slave only device that supports a maximum clock rate (SCLK) of 100 kHz while reading or writing only one register address per I^{2}C start/stop cycle. The following sections will be limited to the methods for writing and reading data into the MCM20007 register.

For a complete reference to I2C, see “The I2C Bus from Theory to Practice” by Dominique Paret and Carl Fenger, published by John Wiley & Sons, ISBN 0471962686.

9.1 MCM20007 I2C Bus Protocol

The MCM20007 uses the I2C bus to write or read one register byte per start/stop I2C cycle as shown in Figure 18 and Figure 19. These figures will be used to describe the various parts of the I2C protocol communications as it applies to the MCM20007.

MCM20007 I2C bus communication is basically composed of following parts: START signal, MCM20007 slave address (0110011) transmission followed by a R/$\overline{W}$ bit, an acknowledgment signal from the slave, 8 bit data transfer followed by another acknowledgment signal, STOP signal, Repeated START signal, and clock synchronization.

9.1.1 START Signal

When the bus is free, i.e. no master device is engaging the bus (both SCLK and SDATA lines are at logical “1”), a master may initiate communication by sending a START signal. As shown in Figure 18, a START signal is defined as a high-to-low transition of SDATA while SCLK is high. This signal denotes the beginning of a new data transfer and wakes up all the slaves on the bus.

9.1.2 Slave Address Transmission

The first byte of a data transfer, immediately after the START signal, is the slave address transmitted by the master. This is a 7-bit calling address followed by a R/$\overline{W}$ bit. The seven-bit address for the MCM20007, starting with the MSB (AD7) is 0110011. The transmitted calling address on the SDATA line may only be changed while SCLK is low as shown in Figure 18. The data on the SDATA line is valid on the High to Low signal transition on the SCLK line. The R/$\overline{W}$ bit following the 7-bit tells the slave the desired direction of data transfer:

- 1 = Read transfer, the slave transitions to a slave transmitter and sends the data to the master
- 0 = Write transfer, the master transmits data to the slave

9.1.3 Acknowledgment

Only the slave with a calling address that matches the one transmitted by the master will respond by sending back an acknowledge bit. This is done by pulling the SDATA line low at the 9th clock (see Figure 18). If a transmitted slave address is acknowledged, successful slave addressing is said to have been achieved. No two slaves in the system may have the same address. The MCM20007 is configured to be a slave only.

9.1.4 Data Transfer

Once successful slave addressing is achieved, data transfer can proceed between the master and the selected slave in a direction specified by the R/$\overline{W}$ bit sent by the calling master. Note that for the first byte after a start signal (in Figure 18 and Figure 19), the R/$\overline{W}$ bit is always a “0” designating a write transfer. This is required since the next data transfer will contain the register address to be read or written.

All transfers that come after a calling address cycle are referred to as data transfers, even if they carry sub-address information for the slave device.

Each data byte is 8 bits long. Data may be changed only while SCLK is low and must be held stable while SCLK is high as shown in Figure 18. There is one clock pulse on SCLK for each data bit, the MSB being transferred first.

Each data byte has to be followed by an acknowledge bit, which is signalled from the receiving device by pulling the SDATA low at the ninth clock. So one complete data byte transfer needs nine clock pulses.

If the slave receiver does not acknowledge the master, the SDATA line must be left high by the slave. The master can then generate a stop signal to abort the data transfer or a start signal (repeated start) to commence a new calling.

If the master receiver does not acknowledge the slave transmitter after a byte transmission, it means 'end of data' to the slave, so the slave releases the SDATA line for the master to generate STOP or START signal.

9.1.5 Stop Signal

The master can terminate the communication by generating a STOP signal to free the bus. However, the master may generate a START signal followed by a calling command without generating a STOP signal first. This is called a Repeated START. A STOP signal is defined as a low-to-high transition of SDATA while SCLK is at logical “1” (see Figure 18).

The master can generate a STOP even if the slave has generated an acknowledge bit at which point the slave must release the bus.

9.1.6 Repeated START Signal

A Repeated START signal is a START signal generated without first generating a STOP signal to terminate the communication. This is used by the master to communicate with another slave or with the same slave in different mode (transmit/receive mode) without releasing the bus.

As shown in Figure 19, a Repeated START signal is shown being used during the read cycle. It is used to redirect the data transfer from a write cycle (master transmits the register address to the slave) to a read cycle (slave transmits the data from the designated register to the slave).

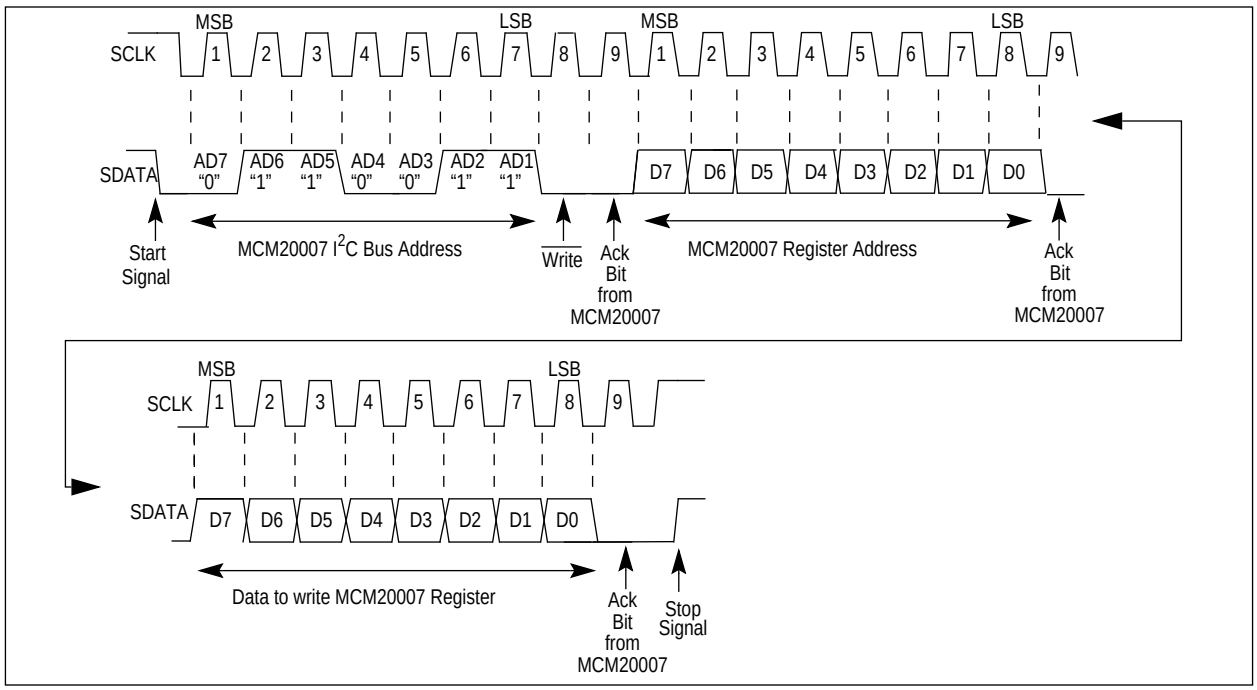


Figure 18. WRITE Cycle using I2C Bus

9.1.7 I2C Bus Clocking and Synchronization

Open drain outputs are used on the SCLK outputs of all master and slave devices so that the clock can be synchronized and stretched using wire-AND logic. This means that the slowest device will keep the bus from going faster than it is capable of receiving or transmitting data.

After the master has driven SCLK from High to Low, all the slaves drive SCLK Low for the required period that is needed by each slave device and then releases the SCLK bus. If the slave SCLK Low period is greater than the master SCLK Low period, the resulting SCLK bus signal Low period is stretched. Therefore, synchronized clocking occurs since the SCLK is held low by the device with the longest Low period. Also, this method can be used by the slaves to slow down the bit rate of a transfer. The master controls the length of time that the SCLK line is in the High state. The data on the SDATA line is valid when the master switches the SCLK line from a High to a Low.

Slave devices may hold the SCLK low after completion of one byte transfer (9 bits). In such case, it halts the bus clock and forces the master clock into wait states until the slave releases the SCLK line.

9.2 Register Write

Writing the MCM20007 registers is accomplished with the following I2C transactions (see Figure 18):

- Master transmits a START
- Master transmits the MCM20007 Slave Calling Address with "WRITE" indicated (BYTE=66_{hex}, 102_{dec}, 01100110_{bin})
- MCM20007 slave sends acknowledgment by forcing the SDATA Low during the 9th clock, if the Calling Address was received
- Master transmits the MCM20007 Register Address

- MCM20007 slave sends acknowledgment by forcing the SDATA Low during the 9th clock after receiving the Register Address
- Master transmits the data to be written into the register at the previously received Register Address
- MCM20007 slave sends acknowledgment by forcing the SDATA Low during the 9th clock after receiving the data to be written into the Register Address
- Master transmits STOP to end the write cycle

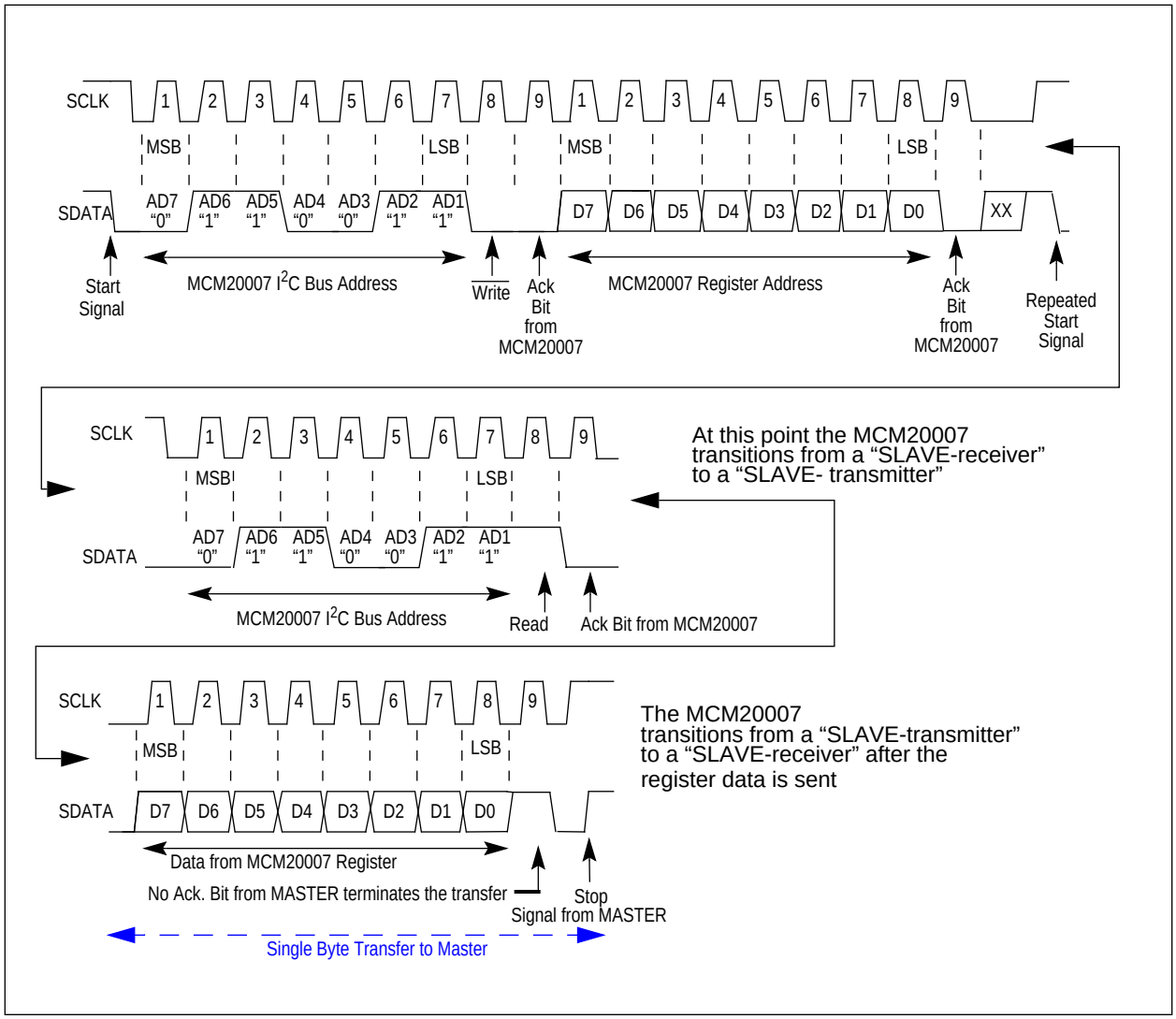
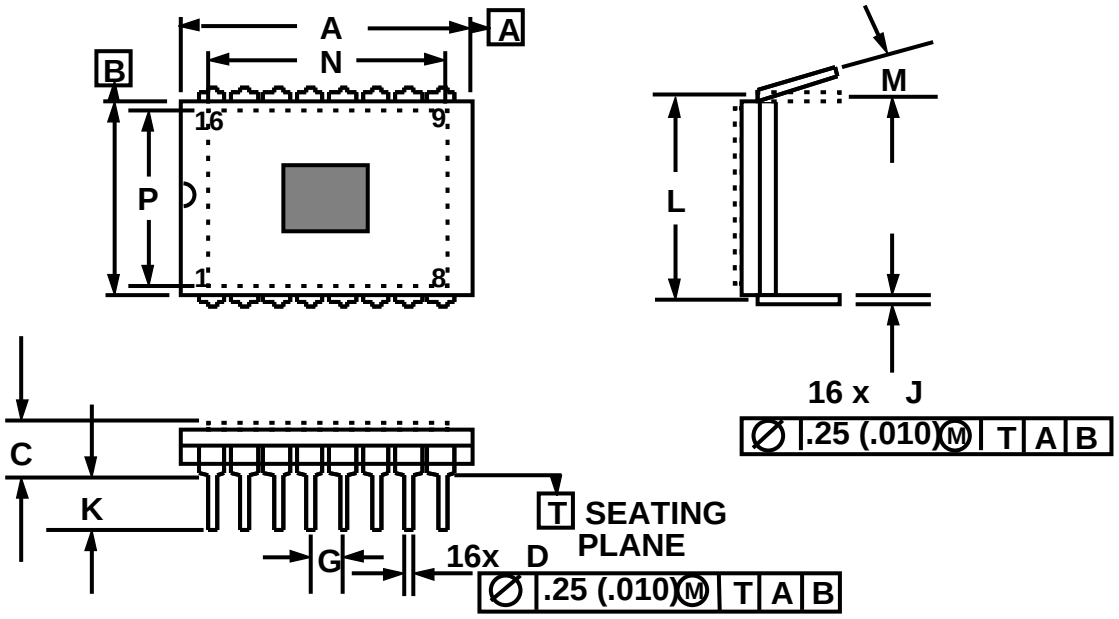


Figure 19. READ Cycle using I2C Bus

9.3 Register Read

Reading the Programmable Timing Generator registers is accomplished with the following I^2C transactions (see Figure 19):

- Master transmits a START
- Master transmits the MCM20007 Slave Calling Address with “WRITE” indicated (BYTE=66_{hex}, 102_{dec}, 01100110_{bin})
- MCM20007 slave sends acknowledgment by forcing the SData Low during the 9th clock, if the Calling Address was received
- Master transmits the MCM20007 Register Address
- MCM20007 slave sends acknowledgment by forcing the SData Low during the 9th clock after receiving the Register Address
- Master transmits a Repeated START
- Master transmits the MCM20007 Slave Calling Address with “READ” indicated (BYTE = 67_{hex}, 103_{dec},01100111)
- MCM20007 slave sends acknowledgment by forcing the SDATA Low during the 9th clock, if the Calling Address was received
- At this point, the MCM20007 transitions from a “Slave-Receiver” to a “Slave-Transmitter”
- MCM20007 sends the SCLK and the Register Data contained in the Register Address that was previously received from the master; MCM20007 transitions to slave-receiver
- Master does not send an acknowledgment (NAK)
- Master transmits STOP to end the read cycle



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	21.1	21.5	0.831	0.847
B	14.85	15.15	0.584	0.596
C	3.62	5.14	0.131	0.189
D	0.36	0.56	0.014	0.022
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	15.24 BSC		0.600 BSC	
M	0°	5°	0°	5°
N	18.3	18.5	0.722	0.730
P	13.5	13.7	0.530	0.538

NOTES
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: METRIC
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

Figure 20. 16 pin CDIP Package (Preliminary Drawing)

Notes:

Note: For the most current information regarding this product, contact Motorola on the World Wide Web at http://sps.motorola.com/consumer-solutions/

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver Colorado 80217. 1-800-441-2447 or 303-675-2140

MFax™: RMFAX0@email.sps.mot.com -TOUCHTONE (602) 244-6609
HOME PAGE:http://motorola.com/sps/

JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 141, 4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan. 81-3-5487-8488

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

MOTOROLA