18-Bit Switchable Active SCSI Bus Terminator (110Ω)

MCCS142235

18–BIT ACTIVE SCSI TERMINATOR (110Ω)

The MCCS142235™ is a precision 18–bit switchable active SCSI bus terminator. It is used in conjunction with a 2.85V regulator (MC34268). Also provided is a Local–V_{CC} (LV_{CC}) low voltage sense circuit to latch the enable state when a peripheral is shut down or loses power. When the device is enabled according to the truth table below, the MCCS142235 provides 110Ω precision resistor pull–ups to a 2.85V reference for termination of 18–bits in a SCSI standard bus system interface. When the switch is disabled, the device is in a High Impedance State on all 18 bits.

The low voltage sense circuit gives the device the ability to latch the current output state when power is removed from the LV_{CC} pin. As long as TERMPWR remains, there is no interruption to the SCSI bus when powering down a SCSI peripheral, because the proper termination condition remains.

In 8–bit SCSI applications (“A” cable), only one ‘2235 is needed at each end of the SCSI cable in order to terminate the 18 active signal lines. In 16–bit WIDE SCSI applications (“P” cable), one ‘2235 and one ‘2234 (or two ‘2235s) would be needed at each end of the SCSI cable in order to terminate the 27 active signal lines.

For information on “Power Dissipation for Active SCSI Terminators,” refer to Motorola Application Note AN1408/D, available through the Motorola Design–NET Fax System, or through the Motorola Literature Distribution Center.

- Complies With SCSI and SCSI–2 Standards
- 18 Switchable 110Ω Terminating Resistors
- Operating Temperature Range: 0°C to 70°C
- Operating Voltage Range: 2.75 to 2.95V
- Resistor Tolerance ±5.0% (Over Temperature and Supply Voltage Ranges)
- Local–V_{CC} (LV_{CC}) Low Voltage Sense Circuit

DW SUFFIX
24–LEAD WIDE SOIC PACKAGE
CASE 751E–04

FA SUFFIX
32–LEAD PLASTIC FQFP PACKAGE
CASE 873A–02

TRUTH TABLE

	Test	Enable	Output
Active Mode	0	0	Z
	0	1	Terminated
Test Mode	1	X	Test Mode

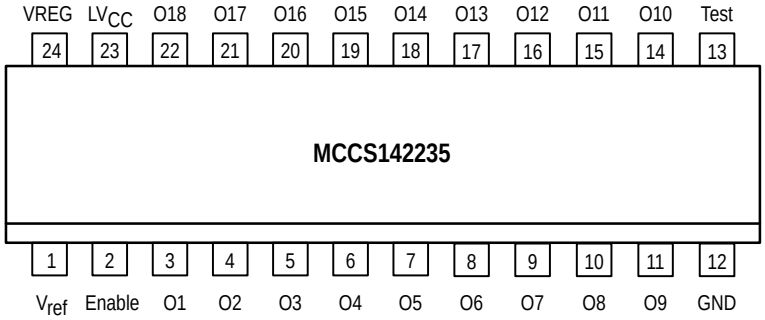

Figure 1. 24–Lead Pinout (Top View)

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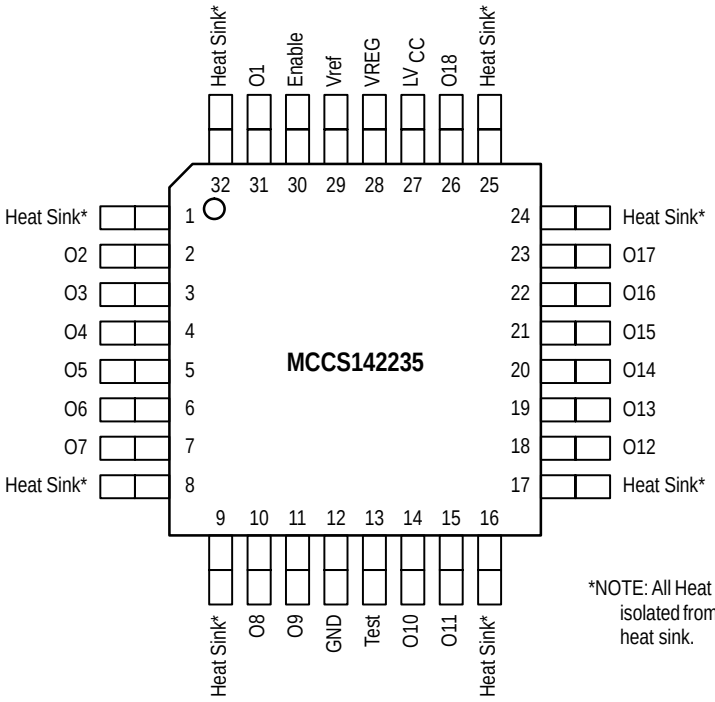


Figure 2. 32–Lead Pinout (Top View)

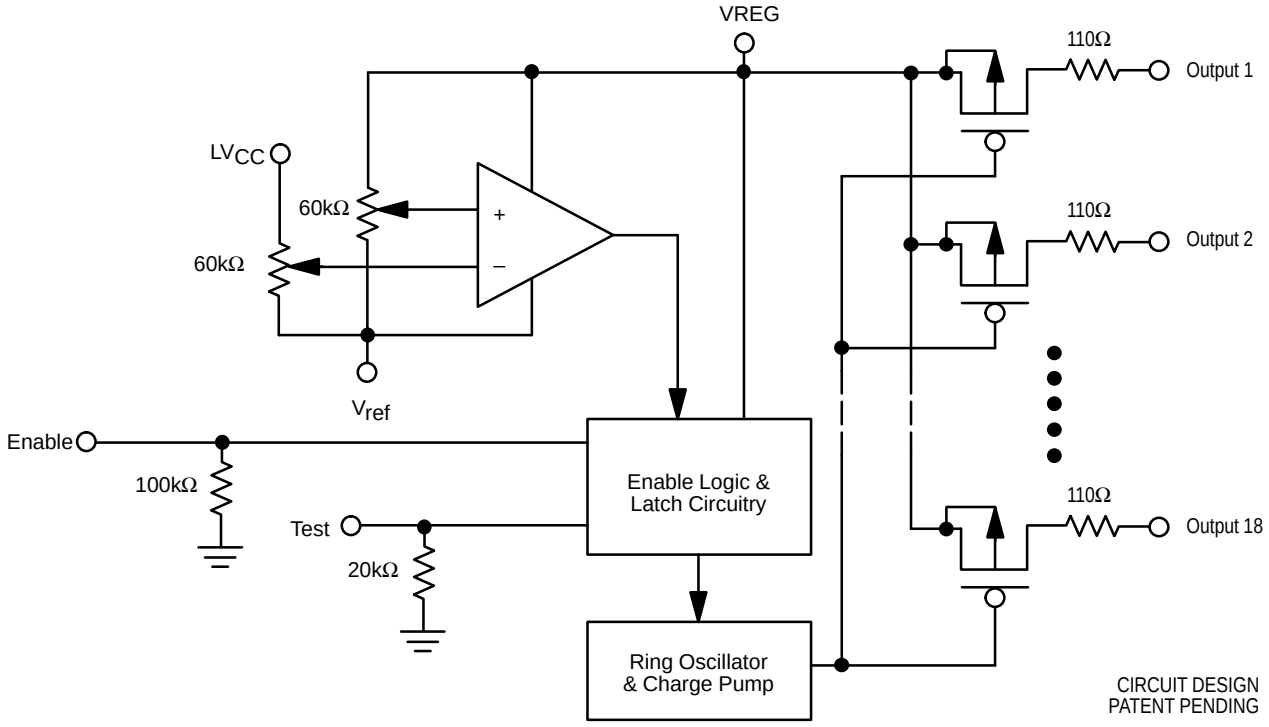
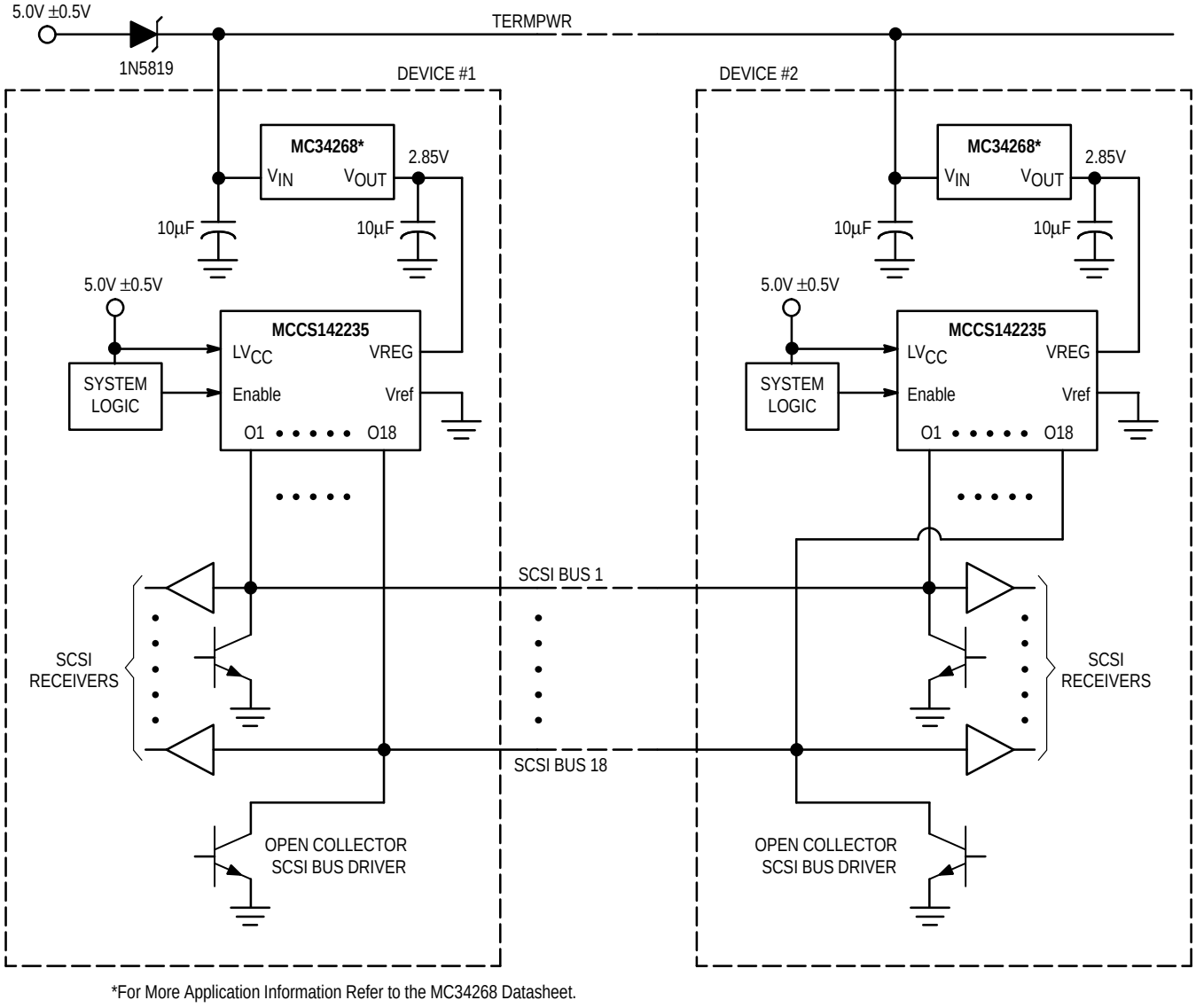


Figure 3. MCCS142235 Block Diagram



*For More Application Information Refer to the MC34268 Datasheet.

Figure 4. Typical SCSI Bus Configuration Using the MCCS142235

MAXIMUM RATINGS*

Symbol	Parameter	Value	Units
VREG	DC Regulated Power Voltage (Referenced to GND)	–0.5 to 3.0	V
V_{in}	DC Input Voltage (Referenced to GND) for Test/V_{ref} pins	– 0.5 to VREG + 0.5	V
V_{in}	DC Input Voltage (Referenced to GND) for LV_{CC}/Enable pins	– 0.5 to + 6.0	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to VREG +0.5	V
I_{in}	DC Input Current, per pin	± 20	mA
I_{out}	DC Output Current, per pin	± 35	mA
I_{CC}	DC Supply Current, VREG and GND pins	± 500	mA
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1mm from case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
VREG	DC Regulated Power Voltage (Referenced to GND)	2.75	2.95	V
V_{in}, V_{out}	DC Input Voltage (Test/V_{ref} Inputs)	0	VREG	V
V_{in}	DC Input Voltage (Enable, LV_{CC} Inputs)	0	5.5	V
T_A	Operating Temperature	0	70	°C
t_r, t_f	Input Rise and Fall Time (All inputs but LV_{CC})	0	500	ns
t_r, t_f	Input Rise and Fall Time (LV_{CC})	0	no limit	ns

DC CHARACTERISTICS

Symbol	Parameters	VREG (V)	25°C		0°C to + 70°C		Unit	Condition
			Min	Max	Min	Max		
V_{IH}	Min High–Level Input Voltage	2.85	2.0		2.0		V	Per Truth Table
V_{IL}	Max Low–Level Input Voltage	2.85		0.8		0.8	V	Per Truth Table
I_{in}	Max Input Leakage Current (Enable Input)	2.85		±0.10		±1.0	µA	V_{in} = GND
	Max Input Leakage Current (Test Input)	2.85		±0.10		±1.0	µA	V_{in} = GND
	Max Input Leakage Current (LV_{CC} Input)	2.85		±0.10		±1.0	µA	V_{in} = GND V_{ref} = GND
		2.85		±100		±200	µA	V_{in} = 5.5V V_{ref} = GND
	Max Input Leakage Current (V_{ref} Input)	2.85		±0.10		±1.0	µA	V_{in} = VREG LV_{CC} = VREG
I_{OZ}	Max Output Leakage Current	2.85		±0.50		±5.0	µA	Per Truth Table V_{out} = GND or VREG
I_{CC}	Max Quiescent Supply Current	2.85		1.0		10	µA	V_{ref}/LV_{CC} = VREG Enable/Test = GND
	Max Quiescent Supply Current (Comparator Active)	2.85		100		200	µA	Enable/V_{ref}/Test = GND LV_{CC} = 5.0V
	Max Quiescent Supply Current (Comparator Active/ Termination Active)	2.85		800		1000	µA	Test/V_{ref} = GND Enable/LV_{CC} = 5.0V I_{out} = 0µA

TERMINATION RESISTOR CHARACTERISTICS

Symbol	Parameters	VREG (V)		35°C		0°C to + 70°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
R110	Output Termination Impedance (Note 1.)	2.75	2.95	108.9 (Note 1.)	111.1 (Note 1.)	104.5	115.5	Ω	Per Truth Table

1. See Figure 5, Termination resistance versus regulated supply voltage and temperature. 110Ω Resistor Target Is at 35°C. Temperature coefficient of resistance T_C = 0.135Ω/°C typical.

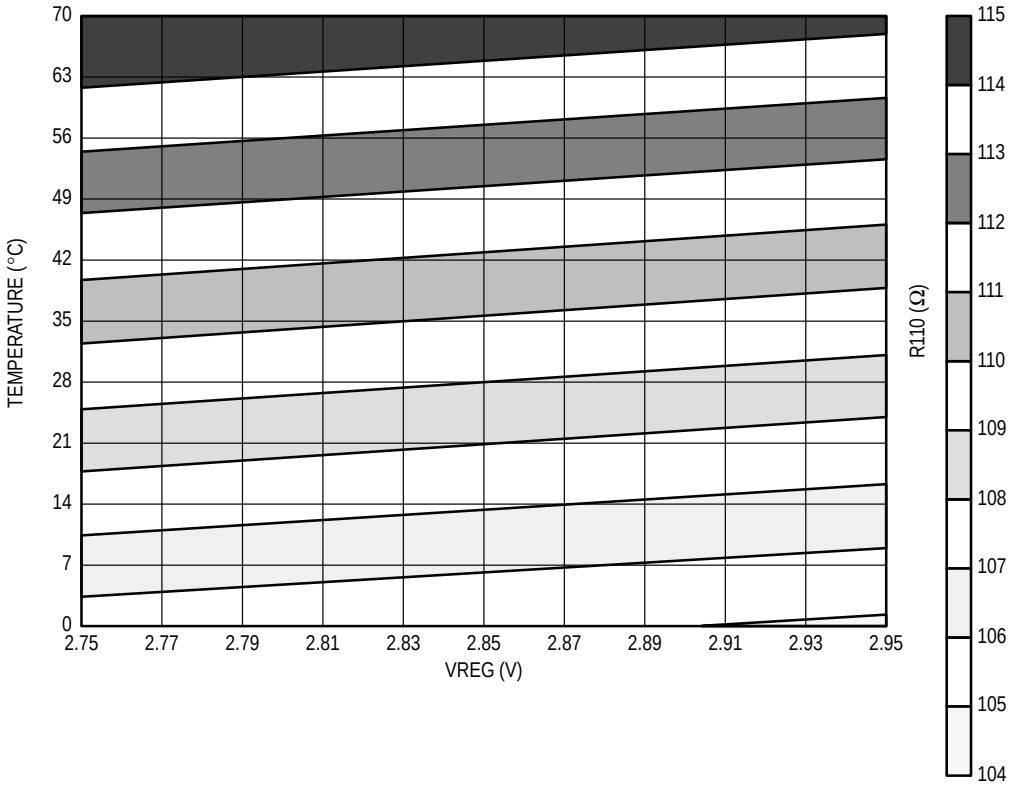


Figure 5. Termination Resistance R110 (Ω) versus Regulated Supply Voltage VREG (V) and Temperature (°C)
(Model Adj R–Sq = 0.9995)

DC CHARACTERISTICS

Symbol	Parameter	VREG (V)	Typical @ +25°C	Unit	Condition
V_T	Latch Voltage (LV_{CC} Input)	2.85	3.70	V	Per Truth Table
C_{out}	Output Capacitance High Impedance	2.85	8.0	pF	Per Truth Table, Output = 0V

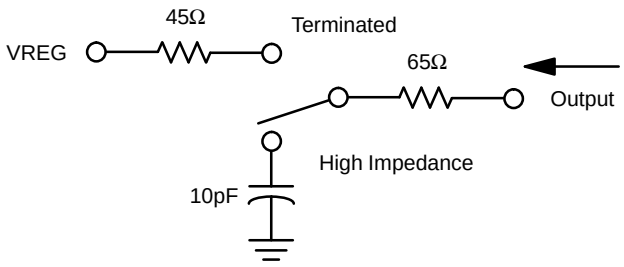


Figure 6. Output Impedance Model

AC CHARACTERISTICS (VREG = 2.85, C_L = 50 pF, $t_r = t_f$ = 6 ns)

Symbol	Parameters	0°C to + 70°C	Unit	Condition
$t_{(Enable)}$	Max Propagation Delay, High Impedance to Termination, Enable to Outputs	100	µs	Per Truth Table
$t_{(Disable)}$	Max Propagation Delay, Termination to High Impedance, Enable to Outputs	1.0	µs	Per Truth Table

TIMING REQUIREMENTS (VREG = 2.85, C_L = 50 pF, $t_r = t_f$ = 6 ns)

Symbol	Parameters	25°C	0°C to + 70°C	Unit	Condition
t_{setup}	Min Setup Time, LV_{CC} to Enable	200	500	ns	(See Figure 7)
t_{hold}	Min Hold Time, LV_{CC} to Enable	50	100	ns	(See Figure 7)

* If LV_{CC} Enable is grounded then the LV_{CC} feature is disabled.

Figure 7. Timing Requirements

MCCS142235 Applications Information

Proper Use of the LV_{CC} Feature

The Motorola Active SCSI Terminator chip incorporates features not available in competitor designs. A primary feature, known as "Local V_{CC} sensing", facilitates future migration to reliable software control of the termination state (either terminated or high impedance). When the Enable pin is driven by internal logic within the SCSI peripheral, it is essential that the peripheral be powered up. Otherwise the enable signal to the termination chip may be invalid causing system bus failure due to improper termination. Imagine a SCSI system with a disk drive at one end of the bus which is providing termination to the bus via the MCCS142235 device. A "smart" drive will be providing an enable signal to the termination chip through internal logic circuitry to ensure termination is present. In the event this same disk drive is powered down by a user while the bus is active, what becomes of the termination located within that drive? Does it remain terminated? Does it change state causing the system to crash? Or does it go into an undetermined state?

The termination power supply is always present on an operating SCSI bus through the dedicated TERMPWR line. But the "Local V_{CC}" power supply within each peripheral may be powered down at any time while the SCSI bus is in operation. It is this local supply which powers the peripheral's logic chips and provides the enable signal to the SCSI terminator chip. Therefore, it is essential to maintain the proper enable signal to the switchable terminator even during peripheral power down.

To avoid rendering the system inoperable while powering down a terminating peripheral, Motorola has an exclusive "Local V_{CC} sensing" circuit on the MCCS142235 which latches the enable state of the termination permanently during peripheral power loss. A comparator within the MCCS142235 can be connected to the local power supply via the LV_{CC} input. The LV_{CC} level is monitored against an internal reference, and the current enable state is latched should LV_{CC} drop below a predetermined value (≈3.70V). This comparator threshold is set sufficiently high to ensure that a valid logic state still exists on the TTL–level Enable pin prior to latching. Upon return of the local power supply, the enable path automatically becomes transparent, and the termination state returns to system control!

The Local V_{CC} sensing feature has been designed to draw as little DC current as possible. Flexibility has been designed into the MCCS142235 to allow the Local V_{CC} sensing feature to be disabled when not required. In this disabled state, the DC bias current is completely removed and the enable latch remains transparent at all times.

Figure 8 shows the recommended connection scheme to utilize the LV_{CC} latch feature. Figure 9 shows the recommended connection scheme for applications in which the LV_{CC} feature is not required – the LV_{CC} and V_{ref} pins are shorted to VREG and the enable path remains permanently transparent.

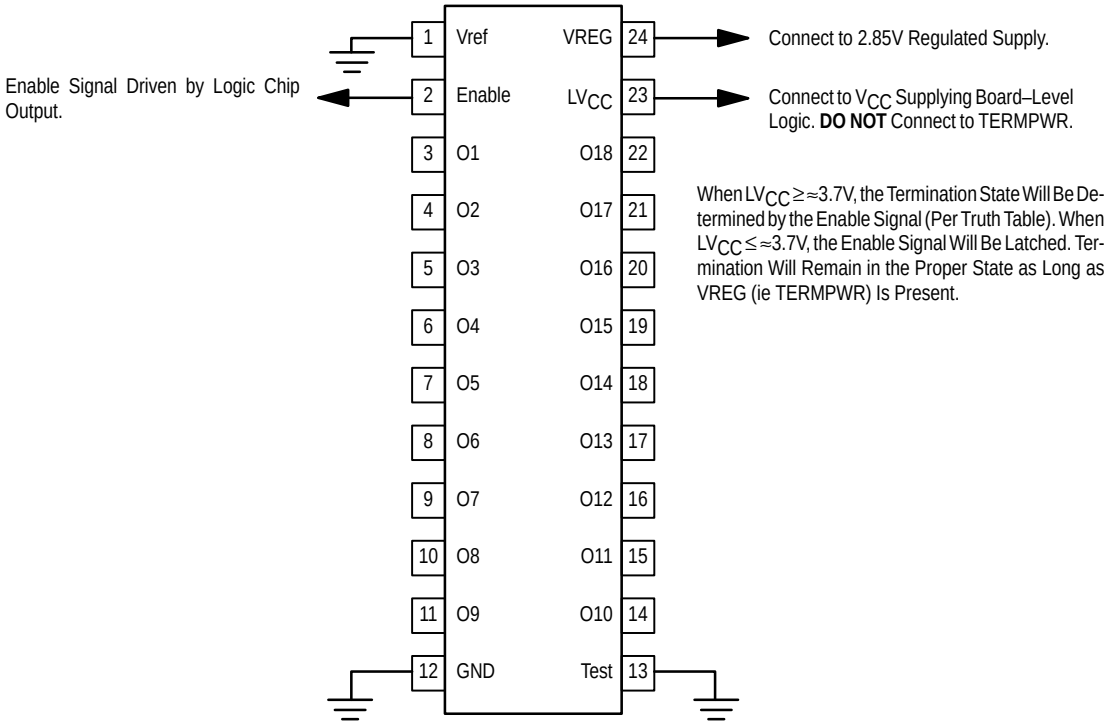


Figure 8. Recommended Connection Scheme to Utilize LV_{CC} Feature

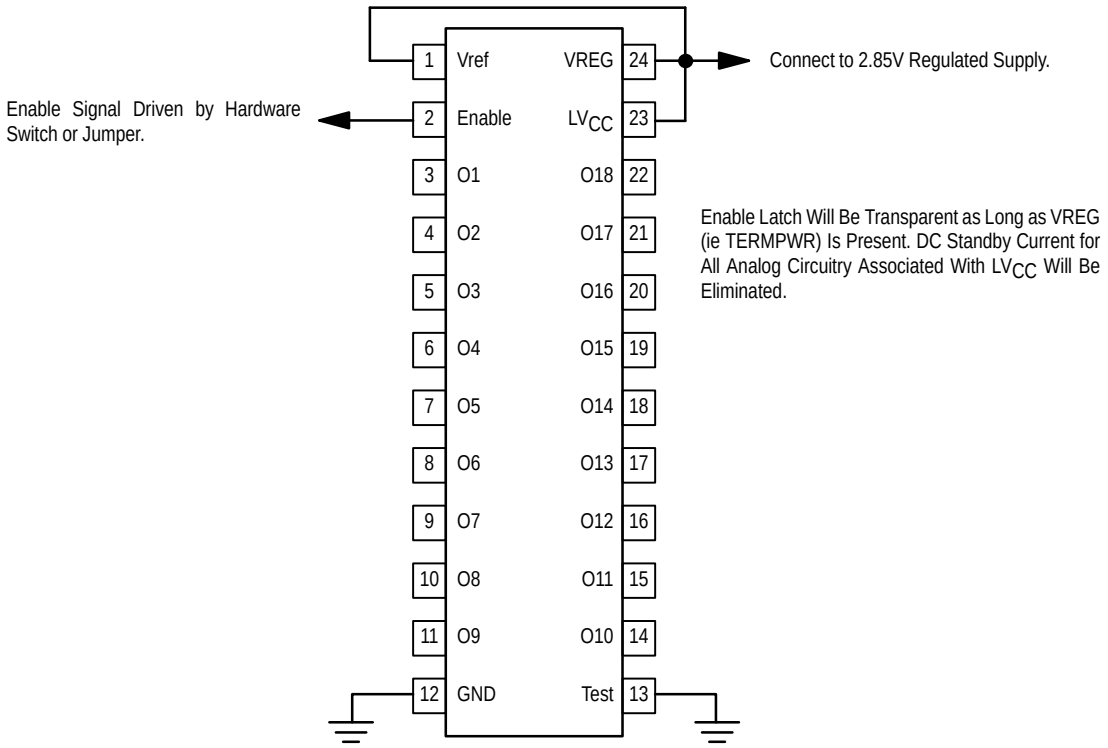
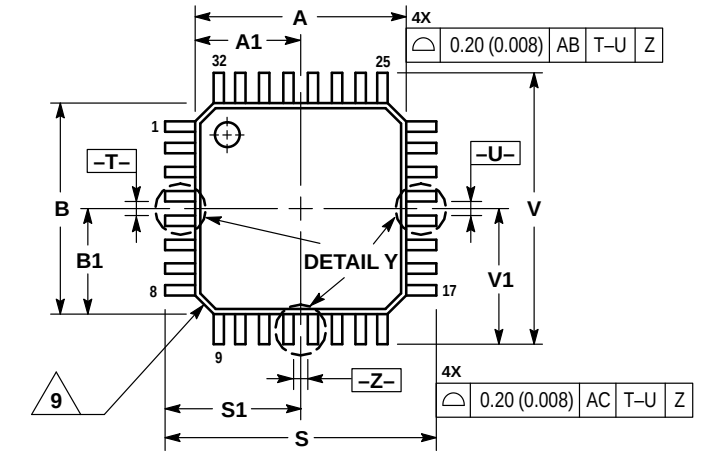


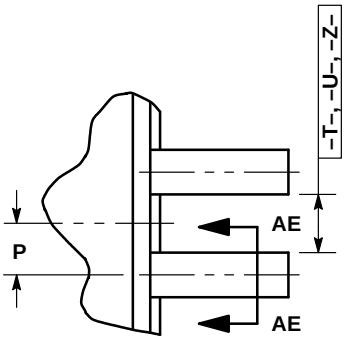
Figure 9. Recommended Connection Scheme to Disable LV_{CC} Feature

Enable Input Application	Result
A. No Connection to Enable	Enable input will be pulled “LOW” internally. Termination will be disabled causing all outputs to be high impedance.
B. Single Pole Switch to Supply	Enable input will be pulled “LOW” internally when the switch is open. Enable input will be held “HIGH” when the switch is closed. The supply source in this case could be TERMPWR, VREG or V_{CC}.
C. Double Pole Switch Between Supply and GND	This is a more expensive way to accomplish application B. above. It is more economical to allow the internal pulldown to provide the “LOW” input level. The Supply Source in this case could be TERMPWR, VREG or V_{CC}.
D. Hardwired “Low”	The MCCS142235 will be permanently disabled causing all outputs to be high impedance.
E. Hardwired “High”	The MCCS142235 will be permanently enabled providing 110Ω nominal impedance to each bus line.
F. External Logic Driven	With LV_{CC} input connected to the local power supply and V_{ref} connected to GND, the Local–V_{CC} sensing and Enable latching feature will be active. If this feature is not desired, tie LV_{CC} and V_{ref} to VREG (per Figure 9), and the Enable state will follow the Truth Table.

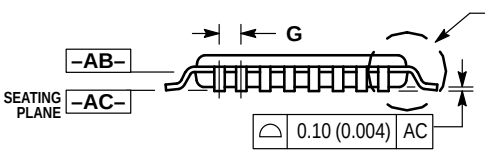
OUTLINE DIMENSIONS

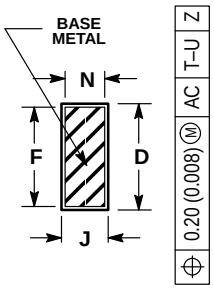
FA SUFFIX
FQFP PACKAGE
CASE 873A–02
ISSUE A



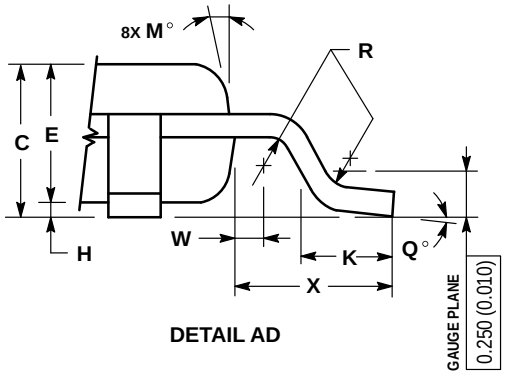


DETAIL Y





SECTION AE–AE



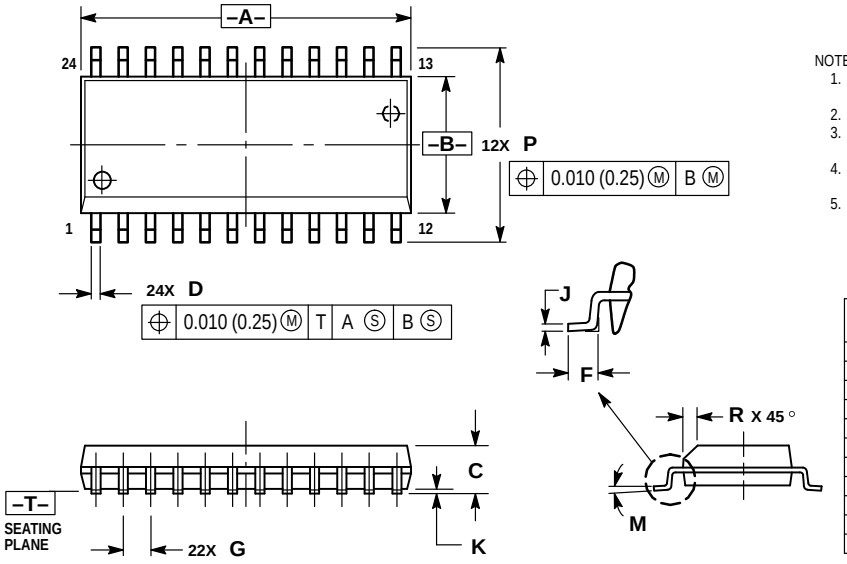
DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

OUTLINE DIMENSIONS

DW SUFFIX
SOIC PACKAGE
CASE 751E–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0 °	8 °	0 °	8 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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