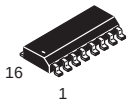
MCCS142234

9-Bit Switchable Active SCSI Bus Terminator (110 Ω)

The MCCS142234™ is a precision 9-bit switchable active SCSI bus terminator with a Local-V_{CC} (LV_{CC}) low voltage sense circuit to latch the Enable state. When the switch is enabled according to the truth table the device provides a 110Ω resistance between regulated supply and each line output for SCSI termination of 9 bits. When the switch is disabled according to the truth table, the device is in a High Impedance State on all 9 bits.

The low voltage sense circuit gives the device the ability to latch the current output state when power is removed from the LV_{CC} pin. As long as VREG remains, there is no interruption to the SCSI bus when powering down a SCSI peripheral.



D SUFFIX
SOIC PACKAGE
CASE 751B-03

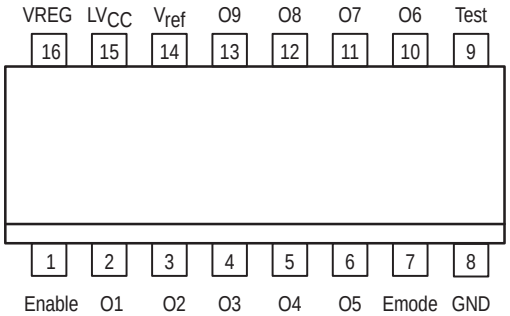
FEATURES

- Complies With SCSI and SCSI-2 Standards
- 9 Switchable 110 Ω Terminating Resistors
- Operating Temperature Range: 0°C to 70°C
- Operating Voltage Range: 2.75 to 2.95V
- Resistor Tolerance ±5.0% (Over Temperature and Supply Voltage Ranges)
- Local-V_{CC} (LV_{CC}) Low Voltage Sense Circuit
- Active HIGH or Active LOW Enable Input

TRUTH TABLE

	Test	Emode	Enable	Output
Active Mode	0	0	0	Terminated
	0	0	1	Z
	0	1	0	Z
	0	1	1	Terminated
Test Mode	1	X	X	220Ω to VREG

PIN ASSIGNMENT



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MOTOROLA

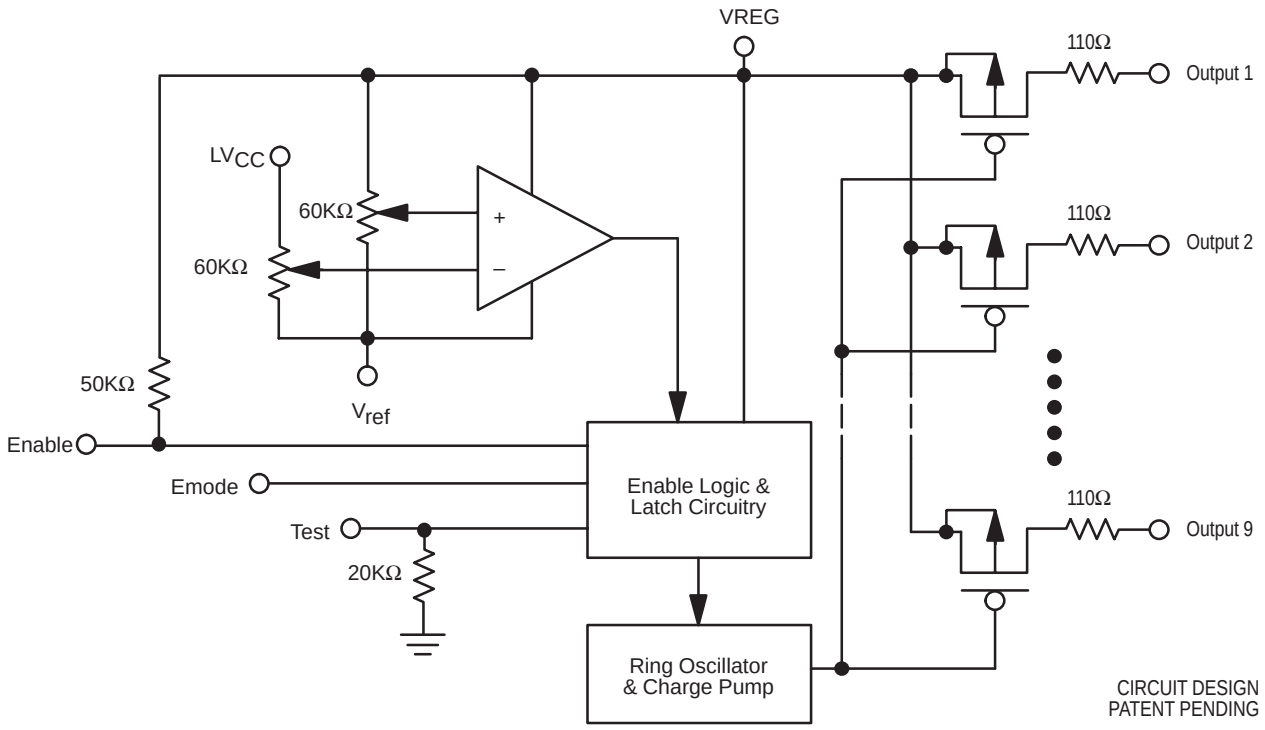


Figure 1. MCCS142234 Block Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Units
VREG	DC Regulated Power Voltage (Referenced to GND)	–0.5 to 3.0	V
V_{in}	DC Input Voltage (Referenced to GND) for Emode/Test/V_{ref} pins	– 0.5 to VREG + 0.5	V
V_{in}	DC Input Voltage (Referenced to GND) for LV_{CC}/Enable pins	– 0.5 to + 6.0	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to VREG +0.5	V
I_{in}	DC Input Current, per pin	± 20	mA
I_{out}	DC Output Current, per pin	± 35	mA
I_{CC}	DC Supply Current, VREG and GND pins	± 250	mA
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1mm from case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

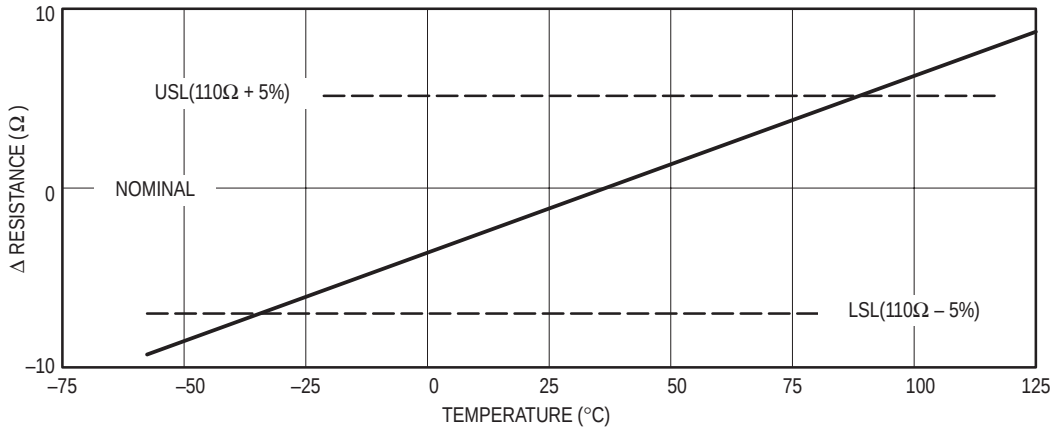
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
VREG	DC Regulated Power Voltage (Referenced to GND)	2.75	2.95	V
V_{in}, V_{out}	DC Input Voltage (Emode/Test/V_{ref} Inputs)	0	VREG	V
V_{in}	DC Input Voltage (Enable, LV_{CC} Inputs)	0	5.5	V
T_A	Operating Temperature	0	70	°C
t_r, t_f	Input Rise and Fall Time (All inputs but LV_{CC})	0	500	ns
t_r, t_f	Input Rise and Fall Time (LV_{CC})	0	no limit	ns

DC CHARACTERISTICS

Symbol	Parameters	VREG (V)	25°C Min	25°C Max	0°C to + 70°C Min	0°C to + 70°C Max	Unit	Condition
V_{IH}	Min High-Level Input Voltage	2.85	2.0		2.0		V	Per Truth Table
V_{IL}	Max Low-Level Input Voltage	2.85		0.8		0.8	V	Per Truth Table
I_{in}	Max Input Leakage Current (Emode Input)	2.85		±0.10		±1.0	µA	V_{in} = VREG or GND
	Max Input Leakage Current (Enable Input)	2.85		±0.10		±1.0	µA	V_{in} = VREG
	Max Input Leakage Current (Test Input)	2.85		±0.10		±1.0	µA	V_{in} = GND
	Max Input Leakage Current (LV_{CC} Input)	2.85		±0.10		±1.0	µA	V_{in} = 0V V_{ref} = GND
		2.85		±100		±200	µA	V_{in} = 5.5V V_{ref} = GND
	Max Input Leakage Current (V_{ref} Input)	2.85		±0.10		±1.0	µA	V_{in} = VREG LV_{CC} = VREG
I_{OZ}	Max Output Leakage Current	2.85		±0.50		±5.0	µA	Per Truth Table V_{out} = GND or VREG
I_{CC}	Max Quiescent Supply Current	2.85		1.0		10	µA	Enable/V_{ref}/LV_{CC} = VREG Test/Emode = GND (See Figure 2)
	Max Quiescent Supply Current (Comparator Active)	2.85		100		200	µA	Emode/V_{ref}/Test = GND Enable/LV_{CC} = 5.0V (See Figure 3)
	Max Quiescent Supply Current (Comparator Active/ Termination Active)	2.85		800		1000	µA	Enable/Emode/Test/ V_{ref} = GND LV_{CC} = 5.0V I_{out} = 0µA (See Figure 4)
R110	Output Termination Impedance[1]	2.75 2.95	Note[1]	Note[1]	104.5	115.5	Ω	Per Truth Table

1 See Graph 1, Temperature Characteristic of 110Ω Resistor. 110Ω Resistor Target Is at 35°C.



Graph 1. Temperature Characteristic of 110Ω Resistor

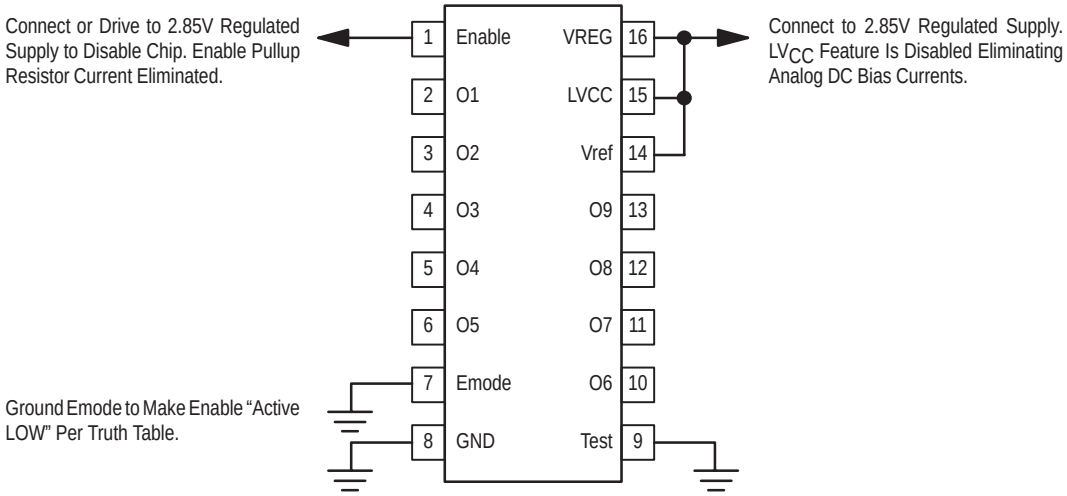


Figure 2. Best Case Static Power Dissipation
(LV_{CC} Feature Disabled; Termination Disabled – High Impedance; Enable "Active LOW")

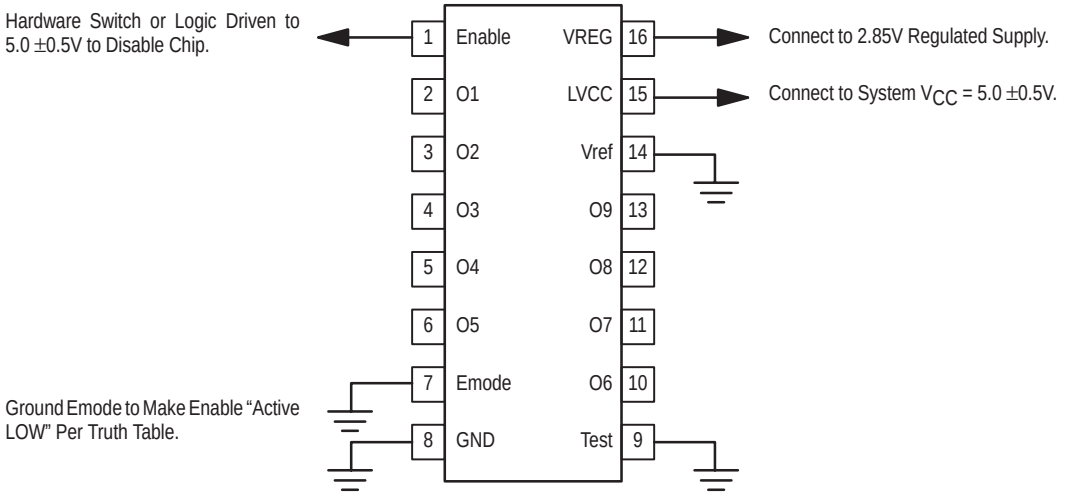


Figure 3. LV_{CC} Comparator Power Dissipation
(LV_{CC} Feature Active; Termination Disabled – High Impedance; Enable "Active LOW")

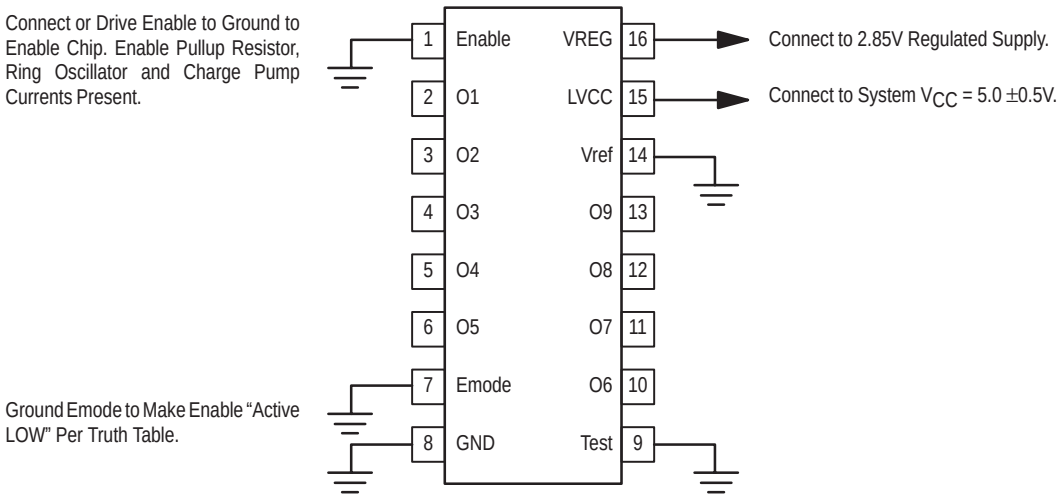


Figure 4. Worst Case Static Power Dissipation
(LV_{CC} Feature Active; Termination Enabled; Enable "Active LOW"; *No Outputs Asserted LOW*)

Symbol	Parameter	VREG (V)	Typical @ +25°C	Unit	Condition
V_T	Latch Voltage (LV_{CC} Input)	2.85	3.70	V	Per Truth Table
C_{out}	Output Capacitance High Impedance	2.85	8.0	pF	Per Truth Table Output = 0V (See Figure 5)

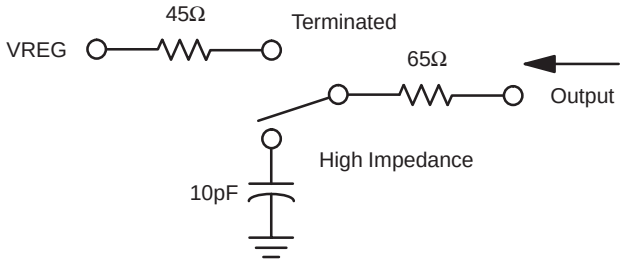


Figure 5. Output Impedance Model

AC CHARACTERISTICS (VREG = 2.85, C_L = 50 pF, $t_r = t_f$ = 6 ns)

Symbol	Parameters	0°C to + 70°C	Unit	Condition
$t_{(Enable)}$	Max Propagation Delay, High Impedance to Termination, Enable or Emode to Outputs	100	µs	Per Truth Table
$t_{(Disable)}$	Max Propagation Delay, Termination to High Impedance, Enable or Emode to Outputs	1.0	µs	Per Truth Table

TIMING REQUIREMENTS (VREG = 2.85, C_L = 50 pF, $t_r = t_f$ = 6 ns)

Symbol	Parameters	25°C	0°C to + 70°C	Unit	Condition
t_{setup}	Min Setup Time, LV_{CC} to Enable	200	500	ns	(See Figure 6)
t_{hold}	Min Hold Time, LV_{CC} to Enable	50	100	ns	(See Figure 6)

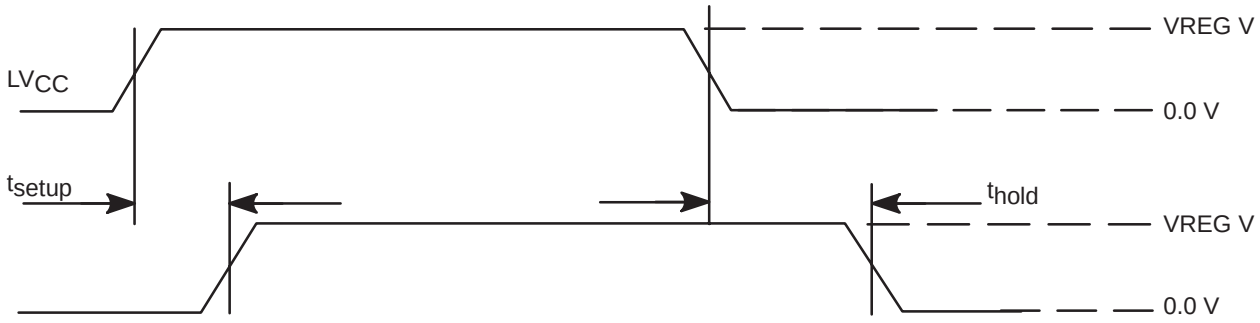


Figure 6. Timing Requirements

Applications Information

The Motorola Active SCSI Terminator chip incorporates several features not available in competitor designs. A primary feature, known as "Local V_{CC} sensing", facilitates future migration to reliable software control of the termination state (either terminated or high impedance). When the Enable pin is driven by internal logic within the SCSI peripheral, it is essential that the peripheral be powered up. Otherwise the Enable signal to the termination chip may be invalid causing system bus failure. Imagine a SCSI system with a disk drive at one end of the bus which is providing termination to the bus via the MCCS142234 device. A "smart" drive will be providing an Enable signal to the termination chip through internal logic circuitry to ensure termination is present. In the event this same disk drive is powered down by a user while the bus is active, what becomes of the termination located within that drive? Does it remain terminated? Does it change state causing the system to crash? Or does it go into an undetermined state?

The termination power supply is always present on an operating SCSI bus through the dedicated TERMPWR line. But the "Local V_{CC}" power supply within each peripheral may be powered down at any time while the SCSI bus is in operation. It is this local supply which powers the peripheral's logic chips and provides the enable signal to the SCSI terminator chip. Therefore, it is essential to maintain the proper enable signal to the switchable terminator even during peripheral power down.

To avoid rendering the system inoperable while powering down a terminating peripheral, Motorola has included a "Local V_{CC} sensing" circuit on the MCCS142234 which latches the enable state of the termination permanently during peripheral power loss. A comparator within the MCCS142234 can be connected to the local power supply via the LV_{CC} input. The LV_{CC} level is monitored against an internal reference, and the current Enable state is latched should LV_{CC} drop below a predetermined value (≈3.70V). This comparator threshold is set sufficiently high to ensure that a valid logic state still exists on the TTL–level Enable pin prior to latching. Upon return of the local power supply, the Enable path automatically becomes transparent, and the termination state returns to system control!

The Enable and LV_{CC} inputs are not diode connected to the regulated power supply (2.85V) of the MCCS142234. They may be directly interfaced to 5.0V logic without conducting current through their inputs or disturbing the regulated level.

The Local V_{CC} sensing feature has been designed to draw as little DC current as possible. Analog circuitry always requires some DC bias current in order to function. This may represent a concern, especially for battery backup or portable applications. Flexibility has been designed into the MCCS142234 to allow the Local V_{CC} sensing feature to be disabled when not required. In this disabled state, the DC bias current is completely removed and the Enable latch remains transparent at all times.

Figure 7 shows the recommended connection scheme to utilize the LV_{CC} latch feature. Per Figure 1, V_{ref} is the analog ground for the resistor divider and comparator circuit, and must be grounded for LV_{CC} operation. Figure 8 shows the recommended connection scheme for applications in which the LV_{CC} feature is not required, and the user wishes to obtain the absolute lowest static power dissipation. V_{ref} and LV_{CC} pins are shorted to VREG and the Enable path remains permanently transparent.

A second unique feature of the MCCS142234 is the user-selectable logic polarity of the Enable input. The Enable and Emode input pins work together to determine the state of the termination resistors; either terminated (Enabled) or high impedance (Disabled). Enable and Emode allow the user to select the polarity of of the Enable signal to match the system logic signal used to drive the Enable input. If Emode is hardwired "HIGH" (to VREG), the Enable input becomes active "HIGH" per the Truth Table. Conversely, with Emode tied "LOW" (to GND), the Enable input becomes active "LOW". This feature eliminates the need to add external inversion to the Enable signal regardless of the polarity of the system signal provided to the MCCS142234.

Emode can be used as an alternate for the Enable input. But, the Emode input has ESD protection which causes it to be diode connected internally to VREG. Therefore Emode should never be driven above the VREG potential. The Enable input is not diode connected to VREG, and may be driven by 5.0V logic.

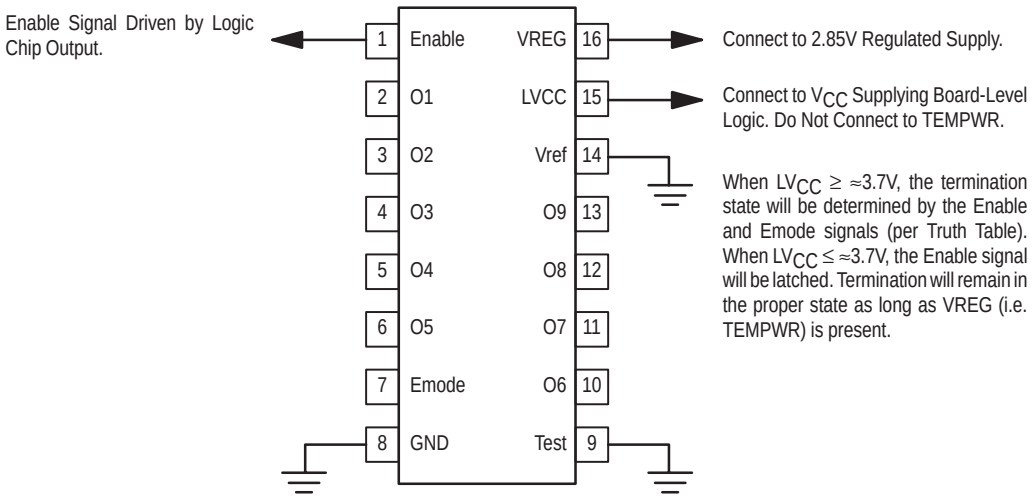


Figure 7. Recommended Connection Scheme to Utilize LV_{CC} Feature

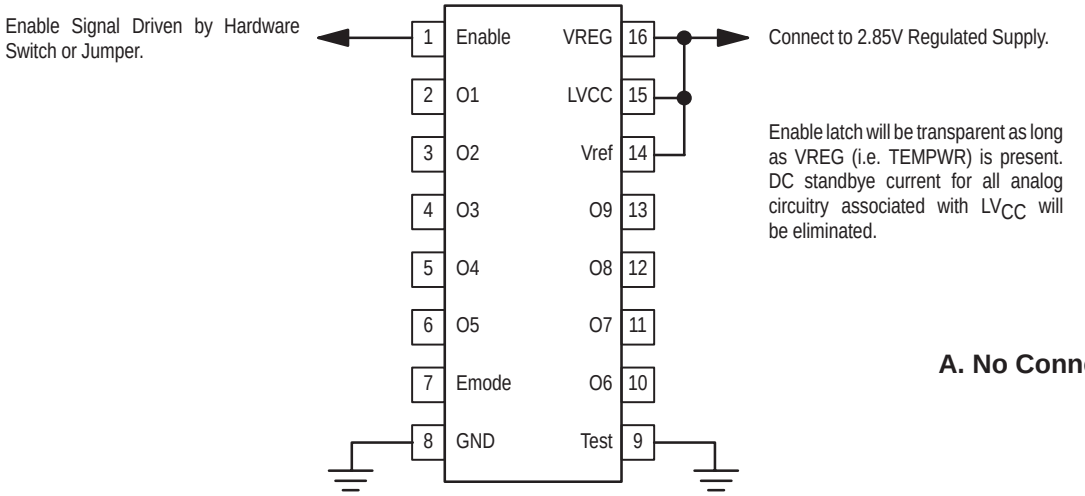


Figure 8. Recommended Connection Scheme to Disable LV_{CC} Feature

Enable Input Application	Result
A. No Connection to Enable	Enable input will be pulled “HIGH” internally. Termination state will depend upon the level of the Emode input. Emode should be hardwired “HIGH” to VREG or the termination will be permanently disabled.
B. Single Pole Switch to GND	Enable input will be pulled “HIGH” internally when the switch is open. Enable input will be held “LOW” when the switch is closed. Termination state will depend upon the level of the Emode input.
C. Double Pole Switch Between Supply and GND	This is a more expensive way to accomplish application B. above. It is more economical to allow the internal pullup to provide the “HIGH” input level. The Supply Source in this case could be TERMPWR, VREG or V_{CC}.
D. Hardwired “High”	
E. Hardwired “Low”	
F. External Logic Driven	

With Emode also hardwired “HIGH”, the MCCS142234 will be permanently enabled and provide termination on all outputs. With Emode hardwired “LOW”, the chip will be permanently disabled.

With Emode also hardwired “LOW”, the MCCS142234 will be permanently enabled and provide termination on all outputs. With Emode hardwired “HIGH” the chip will be permanently disabled. Application D. above is preferred over E. since D. does not draw current through the Enable input pull-up resistor.

With LV_{CC} input connected to the local power supply and V_{ref} connected to GND, the Local-V_{CC} sensing and Enable latching feature will be active. If this feature is not desired, hardwire LV_{CC} and V_{ref} to VREG (per Figure 8), and the Enable state will follow the Truth Table.

Thermal Considerations for Active SCSI Termination

The following formula can be used to determine the operating junction temperature of the MCCS142234, 16-lead SOIC package. However, the assumptions made in this calculationgreatly affect the predicted long-term reliability/lifetime of the device.

$T_j = (P_{diss})(\theta_{ja}) + T_a$

T_j = junction temperature
T_a = ambient temperature
P_{diss} = (V_diss) (ICC_diss) (# lines low) OR (ICC_diss)^2 (R) (# lines low)
V_diss = (VREG – V_{out})
ICC_diss = V_diss/R
R = 110Ω ±5.0%
θ_{ja} = thermal resistance of package from junction to ambient (16-pin SOIC)
= 130°C/W still air OR
= 75°C/W 500 lfpm

The junction temperature will depend on the data transfer rate and the data being transferred. If all 9 MCCS142234 bus lines are low, data equals “0”, maximum power is consumed and the junction temperature will rise accordingly. The information below details the failure mechanism caused by higher temperatures.

Optimizing the Long Term Reliability of Plastic Packages

Today’s plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However when the ultimate in system reliability is required, thermal management must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold (Au) wire bonded to aluminum (Al) bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time, an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperatures are consistent with system reliability goals.

Predicting Bond Failure Time

Based on the results of almost ten (10) years of +125°C operating life testing, a special Arrhenius equation for Au to Al integrity has been developed to show the relationship between junction temperature and reliability. Table I shows the relationship between junction temperature, and continuous operating time to 0.1% wire bond failure, (1 failure per 1000 bonds).

Table I. Device Junction Temperature versus Time to 0.1% Bond Failures

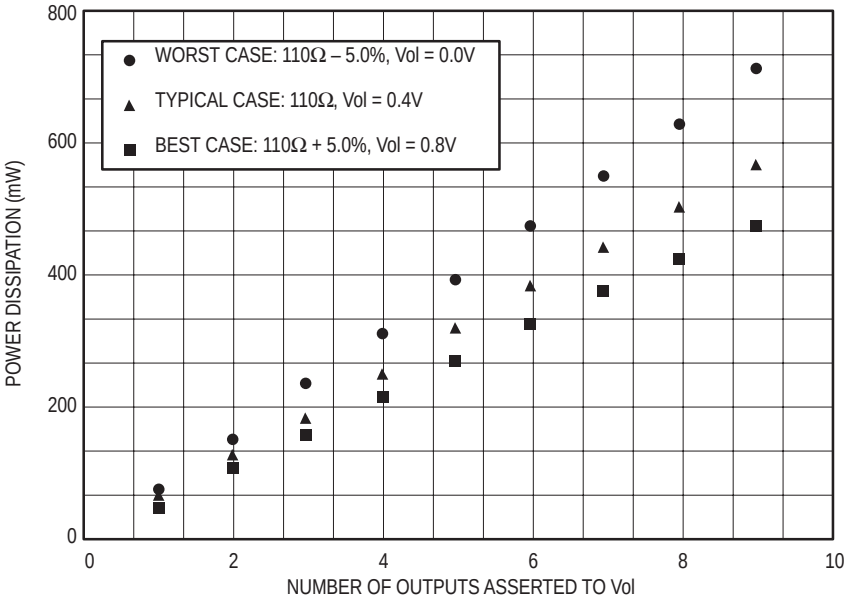
Junction Temperature °C	Time (Hours)	Time (Years)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Worst, Worst Case

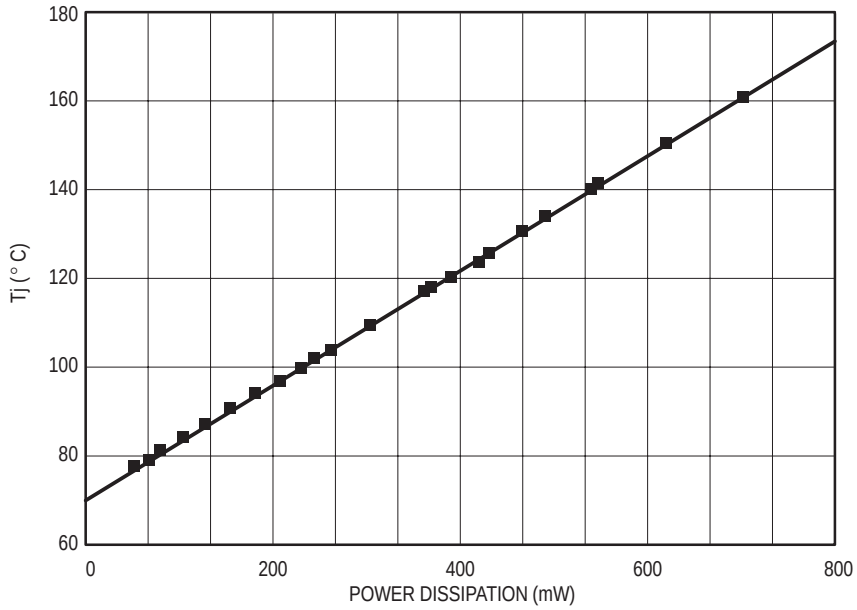
In calculating Tj, the following worst case assumptions were made:

Application: 2 MCCS142234 devices could be used in terminating a SCSI bus.

1) Number of lines low: all 18 lines could be asserted low
2) Duty cycle: signals held low indefinitely (100%)
3) Output low state: signal line is pulled to 0.0V
4) Ambient temperature: Ta could be as high as 70°C



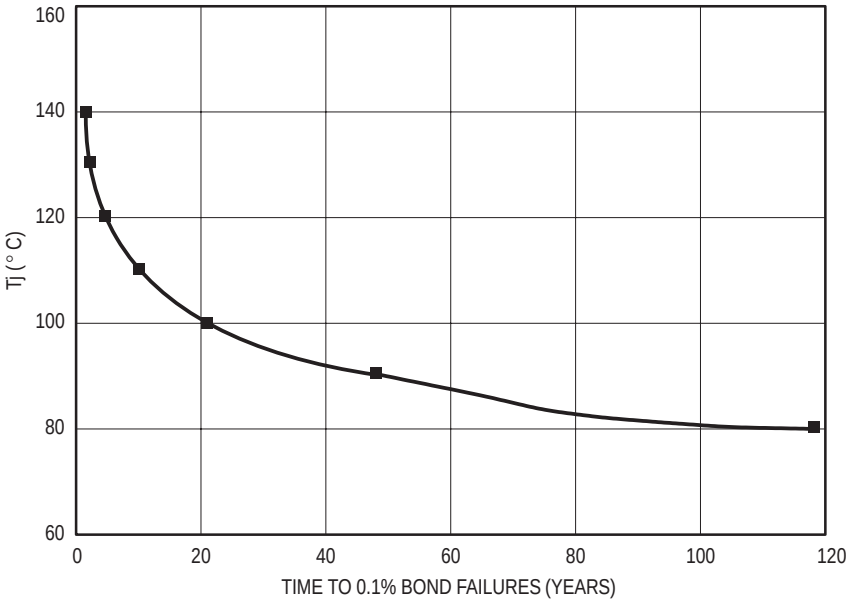
Graph 2. Power versus Number of Outputs Asserted to Vol



Graph 3. Junction Temperature versus Power

Using these assumptions, a spreadsheet was generated to tabulate the power dissipation as the number of lines asserted low increased (see Graph 2). These results, along with Graphs 3 and 4, can be used to show the relationship between “Power Dissipation” and “Time to 0.1% Bond Failures”. With 9 lines low, Tj is calculated to be 156°C which would indicate a time to 0.1% bond failures of less than 1 year (Graph 4). This is **unacceptable**.

Thus, the worst case assumptions were re-examined and tested for validity. Obviously, these assumptions were very gross and leads one to believe the SCSI bus is always active and being driven low. This represents a hard bus short to ground on all lines; a non-functional system condition. The SCSI bus between a workstation and disk drive may in fact be idle most of its operating life.



Graph 4. Junction Temperature versus Time to 0.1% Bond Failures (Years)

A More Realistic Worst Case

New assumptions were proposed to give a more realistic Tj calculation. A discussion of these appears below.

Table 2 shows specific pin states during different phases of operation. Of all the phases, the 9 data bits will be driven low more frequently in the DATA IN phases. Typically, during these phases an average of 3 control signals will be asserted low, along with 9 data bits. Therefore, in actual application usage the SCSI bus will have at most 12 bits asserted low. Only during a bus error will the possibility of all 18 lines being asserted low occur. Even if this condition lasted up to a month, it would not come close to the effect of being indefinitely driven low. Table 2 illustrates the gross nature of the original assumption of all 18 bus lines driven low.

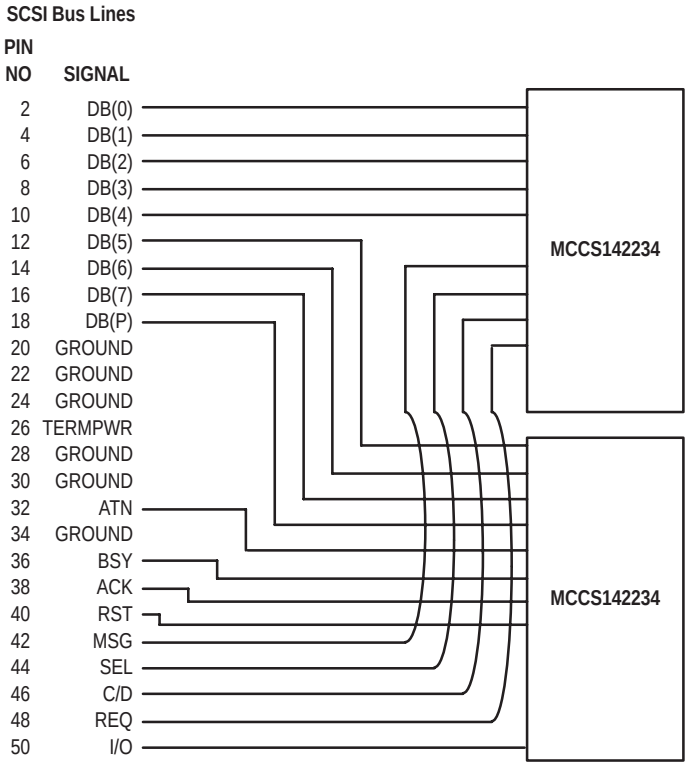


Figure 9. Example of Distributing Most Frequently Asserted Signal Lines

To take the new assumption further, we assume that 2 MCCS142234 are used to terminate a SCSI bus. One now could take additional steps with this information and distribute the 12 signal lines (data 0–8, BSY, I/O, REQ, & ACK) between the 2 devices (see Figure 9). In this way, 6 of the 12 most frequently asserted lines would be routed to each package through prudent board layout. Now the maximum number of lines per package asserted low is 6!

Once again, taking the above assumption a step further and reducing the duty cycle to 50%. The number of lines held low for a lifetime of the device can be approximated to 3 equating to 6 lines per package driven low at a 50% duty cycle. This takes into consideration that data will not always consist of “0” and that the bus at times may not be in use. One could even go further and propose a lower duty cycle so long as they have a thorough understanding of system utilization.

Table 2. SCSI Bus Phases (Source: SCSI Bench Reference – ENDL Publications)

BSY	SEL	MSG	C/D	I/O	REQ	ACK	ATN	RST	Data (0–8)	Bus Phase or Condition
1	0	X	X	X	0	0	X	0	X’s	Between Information Transfer Phases
1	0	0	0	0	1	0	X	0	X’s	Beginning of DATA OUT Phase
1	0	0	0	0	1	1	X	0	X’s	State During DATA OUT Phase
1	0	0	0	0	0	1	X	0	X’s	State During DATA OUT Phase
1	0	0	0	0	0	0	X	0	X’s	State During DATA OUT Phase
1	**0**	**0**	**0**	**1**	**1**	**0**	**X**	**0**	**X’s**	**Beginning of DATA IN Phase } Worst**
1	**0**	**0**	**0**	**1**	**1**	**1**	**X**	**0**	**X’s**	**State During DATA IN Phase } Case**
1	**0**	**0**	**0**	**1**	**0**	**1**	**X**	**0**	**X’s**	**State During DATA IN Phase } Number Lines**
1	**0**	**0**	**0**	**1**	**0**	**0**	**X**	**0**	**X’s**	**State During DATA IN Phase } Asserted**
1	0	0	1	0	1	0	X	0	X’s	Beginning of COMMAND Phase
1	0	0	1	0	1	1	X	0	X’s	State During COMMAND Phase
1	0	0	1	0	0	1	X	0	X’s	State During COMMAND Phase
1	0	0	1	1	1	0	X	0	X’s	Beginning of STATUS Phase
1	0	0	1	1	1	1	X	0	X’s	State During STATUS Phase
1	0	0	1	1	0	1	X	0	X’s	State During STATUS Phase
1	0	1	1	0	1	0	X	0	X’s	Beginning of MESSAGE OUT Phase
1	0	1	1	0	1	1	X	0	X’s	State During MESSAGE OUT Phase
1	0	1	1	0	0	1	X	0	X’s	State During MESSAGE OUT Phase
1	0	1	1	1	1	0	X	0	X’s	Beginning of MESSAGE IN Phase
1	0	1	1	1	1	1	X	0	X’s	State During MESSAGE IN Phase
1	0	1	1	1	0	1	X	0	X’s	State During MESSAGE IN Phase
1	0	1	0	0	1	0	X	0	X’s	Reserved Phase
1	0	1	0	1	1	0	X	0	X’s	Reserved Phase
1	0	X	X	X	X	X	1	0	X’s	ATTENTION CONDITION
0	0	X	X	X	X	X	X	0	0’s	BUS FREE
0	0	X	X	X	X	X	X	1	0’s	RESET CONDITION
1	0	0	0	0	0	0	0	0	X’s	ARBITRATION
1	1	0	0	X	0	0	X	0	X’s	Bus Winner Takes Bus
0	1	0	0	0	0	0	1	0	X’s	SELECTION
1	1	0	0	0	0	0	1	0	X’s	Target Responds to Selection
1	0	0	0	0	0	0	1	0	X’s	Initiator Responds to Target
0	1	0	0	1	0	0	0	0	X’s	RESELECTION
1	1	0	0	1	0	0	0	0	X’s	Target Responds to Reselection
1	0	0	0	1	0	0	0	0	X’s	Initiator Responds to Initiator
1	0	X	X	X	0	0	X	0	X’s	Between Information Transfers Phases
1	0	X	X	X	X	X	1	X	X’s	ATTENTION CONDITION

0 = Negated or Released; 1 = Asserted; X = Can Be Either State

Lastly, an erroneous assumption is that signal lines asserted low are driven to a true 0 Volts. The VIL specification in the SCSI standard permits the VIL signal to be anywhere from 0 to 0.8 Volts. Hence, this low state value will largely depend on the driver used in the system. For example, TTL drivers (FAST — 24mA) and CMOS drivers (FACT — 24mA) will typically drive to 0.4V.

To summarize, the new set of assumptions are:

1) A maximum of 12 of 18 lines can be asserted low at one time during normal operation.

2) Data lines (0–8) and control lines (BSY, I/O, REQ, & ACK) can be separated with prudent board layout therefore splitting 6 lines per package.

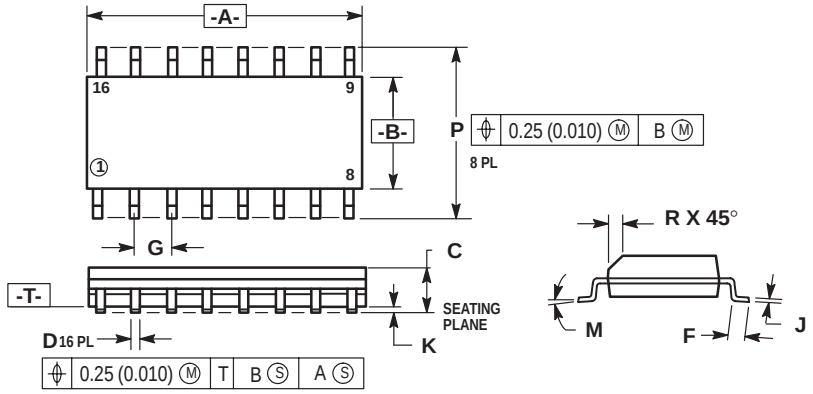
3) These lines are asserted with a 50% duty cycle.

4) Lines are not driven to 0 Volts, more realistically this value is 0.4 Volts.

Graphs 2, 3, and 4 give a new perspective on the power calculation when you compare the worst case to the best and typical case. The typical case value for Tj is now 91°C, which will translate to a lifetime of over 40 years.

OUTLINE DIMENSIONS

D SUFFIX
SOIC PACKAGE
CASE 751B-03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES

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