

MC74VHCT595A

Product Preview

8-Bit Shift Register with Output Storage Register (3-State)

The MC74VHCT595A is an advanced high speed 8-bit shift register with an output storage register fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation. The MC74VHCT595A contains an 8-bit static shift register which feeds an 8-bit storage register.

The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS to 5.0 V CMOS logic, or from 1.8 V CMOS logic to 3.0 V CMOS logic, while operating at the high-voltage power supply.

Shift operation is accomplished on the positive going transition of the Shift Clock input (SCK). The output register is loaded with the contents of the shift register on the positive going transition of the Register Clock input (RCK). Since the RCK and SCK signals are independent, parallel outputs can be held stable during the shift operation. And, since the parallel outputs are 3-state, the VHC595 can be directly connected to an 8-bit bus. This register can be used in serial-to-parallel conversion, data receivers, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the device to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage—input/output voltage mismatch, battery backup, hot insertion, etc.

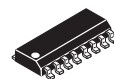
- High Speed: $f_{max} = 185\text{MHz}$ (Typ) at $V_{CC} = 5\text{V}$
- Low Power Dissipation: $I_{CC} = 4\mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- TTL-Compatible Inputs: $V_{IL} = 0.8\text{V}$; $V_{IH} = 2.0\text{V}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 3 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 1.0\text{V}$ (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.



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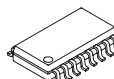
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SOIC-16
D SUFFIX
CASE 751B

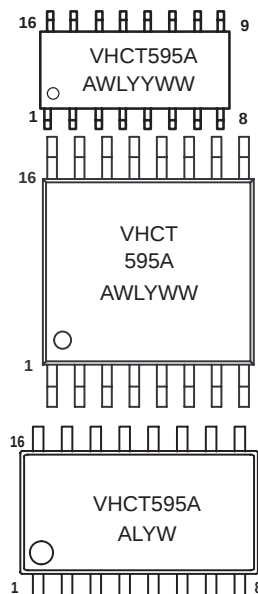


TSSOP-16
DT SUFFIX
CASE 948F



SOIC EIAJ-16
M SUFFIX
CASE 966

MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

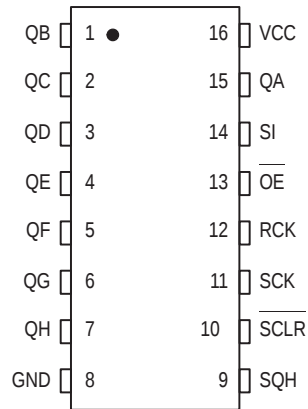
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

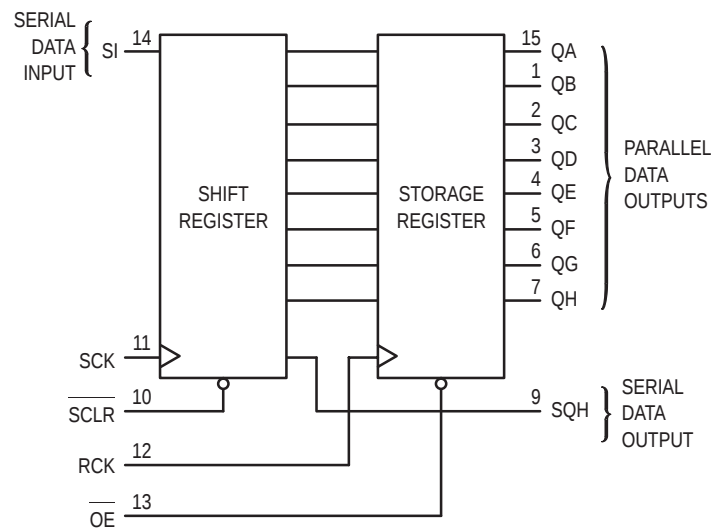
Device	Package	Shipping
MC74VHCT595AD	SOIC-16	48 Units/Rail
MC74VHCT595ADR2	SOIC-16	2500 Units/Reel
MC74VHCT595ADT	TSSOP-16	96 Units/Rail
MC74VHCT595ADTEL	TSSOP-16	2000 Units/Reel
MC74VHCT595ADTR2	TSSOP-16	2500 Units/Reel
MC74VHCT595AM	SOIC EIAJ-16	50 Units/Rail
MC74VHCT595AMEL	SOIC EIAJ-16	2000 Units/Reel

MC74VHCT595A

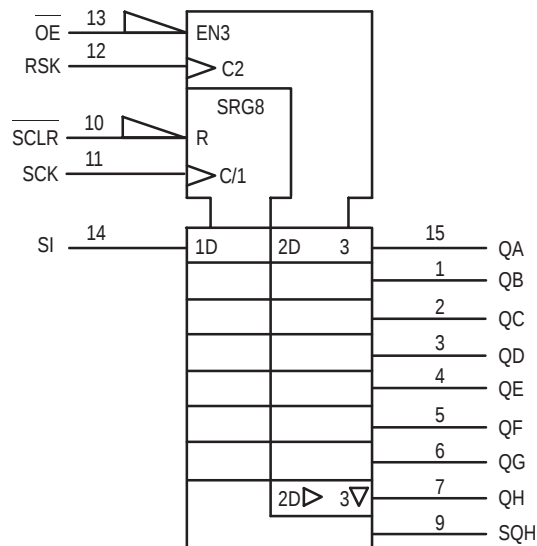
PIN ASSIGNMENT



LOGIC DIAGRAM

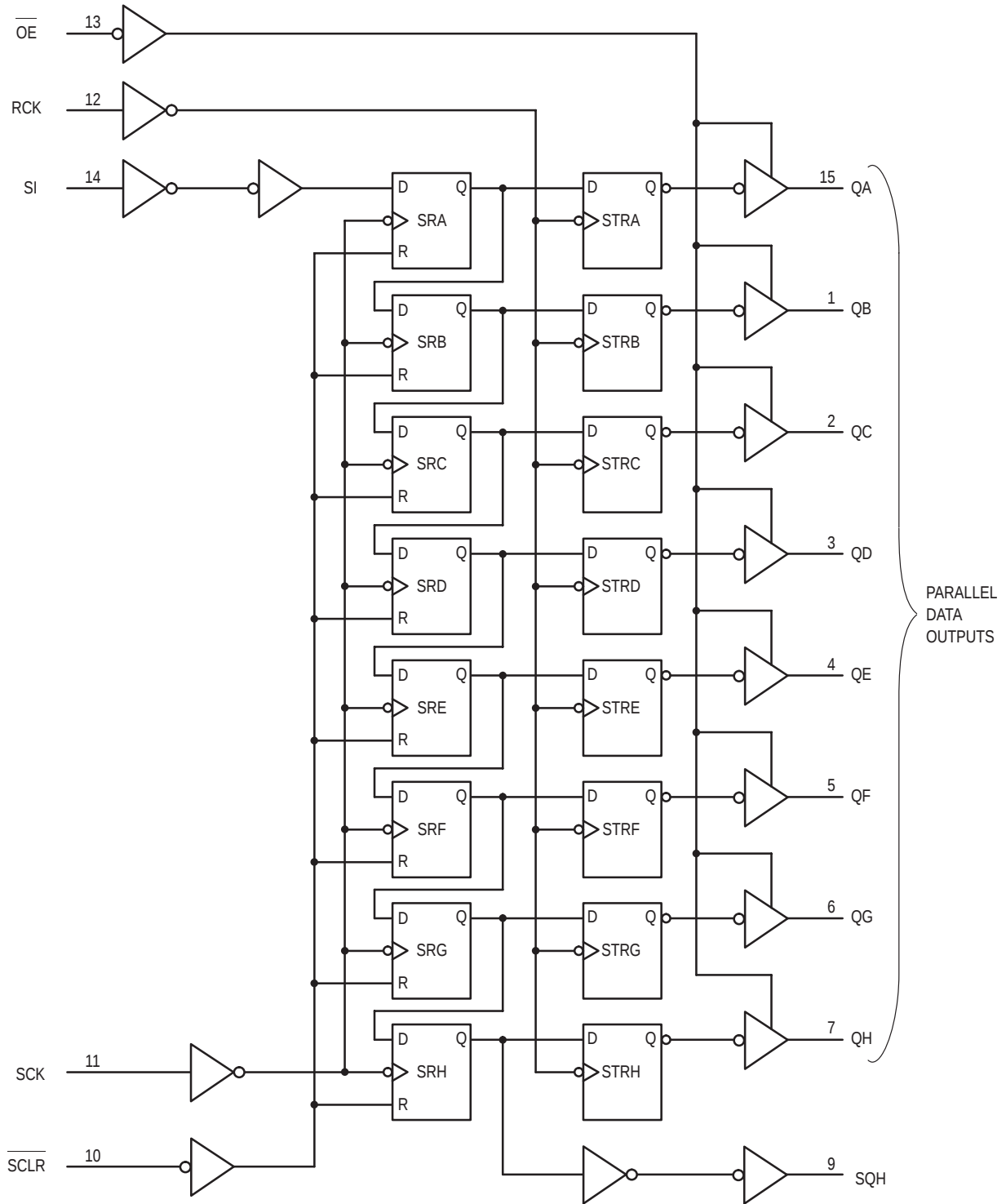


IEC LOGIC SYMBOL



MC74VHCT595A

EXPANDED LOGIC DIAGRAM



MC74VHCT595A

FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset (SCLR)	Serial Input (SI)	Shift Clock (SCK)	Reg Clock (RCK)	Output Enable (OE)	Shift Register Contents	Storage Register Contents	Serial Output (SQH)	Parallel Outputs (QA – QH)
Clear shift register	L	X	X	L, H, ↓	L	L	U	L	U
Shift data into shift register	H	D	↑	L, H, ↓	L	D SR _A ; SR _N SR _{N+1}	U	SR _G SR _H	U
Registers remains unchanged	H	X	L, H, ↓	X	L	U	**	U	**
Transfer shift register contents to storage register	H	X	L, H, ↓	↑	L	U	SR _N →STR _N	*	SR _N
Storage register remains unchanged	X	X	X	L, H, ↓	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents D = data (L, H) logic level ↓ = High-to-Low * = depends on Reset and Shift Clock inputs

STR = storage register contents U = remains unchanged ↑ = Low-to-High ** = depends on Register Clock input

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V _{IN}	DC Input Voltage	– 0.5 to + 7.0	V
V _{OUT}	DC Output Voltage V _{CC} = 0 High or Low State	– 0.5 to + 7.0 – 0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current	– 20	mA
I _{OK}	Output Diode Current (V _{OUT} <GND; V _{OUT} >V _{CC})	± 20	mA
I _{OUT}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 75	mA
P _D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

† Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	3.0	5.5	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage V _{CC} = 0 High or Low State	0 0	5.5 V _{CC}	V
T _A	Operating Temperature	– 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time V _{CC} = 5.0V ± 0.5V	0	20	ns/V

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The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

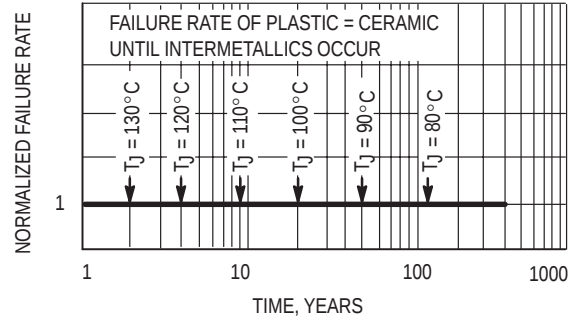


Figure 1. Failure Rate vs. Time
Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			T _A = ≤ 85°C		T _A = ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0		V
V _{IL}	Maximum Low-Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0		± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			4.0		40.0		40.0	μA
I _{CCT}	Quiescent Supply Current	Input: V _{IN} = 3.4 V	5.5			1.35		1.50		1.5	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0.0			0.5		5.0		5.0	mA
I _{OZ}	Three-State Output Off-State Current	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5			± 0.25		± 2.5		± 2.5	μA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = \leq 85^\circ\text{C}$		$T_A = \leq 125^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 3.3 \pm 0.3\text{ V}$ $C_L = 15\text{pF}$ $R_L = 1\text{ k}\Omega$ $C_L = 50\text{pF}$	80 55	150 130		70 50		70 50		MHz
		$V_{CC} = 5.0 \pm 0.5\text{ V}$ $C_L = 15\text{pF}$ $R_L = 1\text{ k}\Omega$ $C_L = 50\text{pF}$	135 95	185 155		115 85		115 85		
$t_{\text{PLH}}, t_{\text{PHL}}$	Propagation Delay, SCK to SQH	$V_{CC} = 3.3 \pm 0.3\text{ V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		8.8 11.3	13.0 16.5	1.0 1.0	15.0 18.5	1.0 1.0	15.0 18.5	ns
		$V_{CC} = 5.0 \pm 0.5\text{ V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		6.2 7.7	8.2 10.2	1.0 1.0	9.4 11.4	1.0 1.0	9.4 11.4	
t_{PHL}	Propagation Delay, CPLR to SQH	$V_{CC} = 3.3 \pm 0.3\text{ V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		8.4 10.9	12.8 16.3	1.0 1.0	13.7 17.2	1.0 1.0	13.7 17.2	ns
		$V_{CC} = 5.0 \pm 0.5\text{ V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		5.9 7.4	8.0 10.0	1.0 1.0	9.1 11.1	1.0 1.0	9.1 11.1	
$t_{\text{PLH}}, t_{\text{PHL}}$	Propagation Delay, RCK to QA–QH	$V_{CC} = 3.3 \pm 0.3\text{ V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		7.7 10.2	11.9 15.4	1.0 1.0	13.5 17.0	1.0 1.0	13.5 17.0	ns
		$V_{CC} = 5.0 \pm 0.5\text{ V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		5.4 6.9	7.4 9.4	1.0 1.0	8.5 10.5	1.0 1.0	8.5 10.5	
$t_{\text{PZL}}, t_{\text{PZH}}$	Output Enable Time, OE to QA–QH	$V_{CC} = 3.3 \pm 0.3\text{ V}$ $C_L = 15\text{pF}$ $R_L = 1\text{ k}\Omega$ $C_L = 50\text{pF}$		7.5 9.0	11.5 15.0	1.0 1.0	13.5 17.0	1.0 1.0	13.5 17.0	ns
		$V_{CC} = 5.0 \pm 0.5\text{ V}$ $C_L = 15\text{pF}$ $R_L = 1\text{ k}\Omega$ $C_L = 50\text{pF}$		4.8 8.3	8.6 10.6	1.0 1.0	10.0 12.0	1.0 1.0	10.0 12.0	
$t_{\text{PLZ}}, t_{\text{PHZ}}$	Output Disable Time, OE to QA–QH	$V_{CC} = 3.3 \pm 0.3\text{ V}$ $C_L = 50\text{pF}$ $R_L = 1\text{ k}\Omega$		12.1	15.7	1.0	16.2	1.0	16.2	ns
		$V_{CC} = 5.0 \pm 0.5\text{ V}$ $C_L = 50\text{pF}$ $R_L = 1\text{ k}\Omega$		7.6	10.3	1.0	11.0	1.0	11.0	
C_{IN}	Input Capacitance			4	10		10		10	pF
C_{OUT}	Three-State Output Capacitance (Output in High-Impedance State), QA–QH			6			10		10	pF

C_{PD}	Power Dissipation Capacitance (Note 1.)	Typical @ 25°C , $V_{CC} = 5.0\text{V}$	pF
		87	

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{\text{CC(OPR)}} = C_{\text{PD}} \cdot V_{CC} \cdot f_{\text{in}} + I_{\text{CC}}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{\text{PD}} \cdot V_{CC}^2 \cdot f_{\text{in}} + I_{\text{CC}} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$, $C_L = 50\text{pF}$, $V_{CC} = 5.0\text{V}$)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.8	1.0	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.8	– 1.0	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.2	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.7	V

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TIMING REQUIREMENTS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	V _{CC} V	T _A = 25°C		T _A = – 40 to 85°C	T _A = – 55 to 125°C	Unit
			Typ	Limit	Limit	Limit	
t _{su}	Setup Time, SI to SCK	3.3 5.0		3.5 3.0	3.5 3.0	3.5 3.0	ns
t _{su(H)}	Setup Time, SCK to RCK	3.3 5.0		8.0 5.0	8.5 5.0	8.5 5.0	ns
t _{su(L)}	Setup Time, SCLR to RCK	3.3 5.0		8.0 5.0	9.0 5.0	9.0 5.0	ns
t _h	Hold Time, SI to SCK	3.3 5.0		1.5 2.0	1.5 2.0	1.5 2.0	ns
t _{h(L)}	Hold Time, SCLR to RCK	3.3 5.0		0 0	0 0	1.0 1.0	ns
t _{rec}	Recovery Time, SCLR to SCK	3.3 5.0		3.0 2.5	3.0 2.5	3.0 2.5	ns
t _w	Pulse Width, SCK or RCK	3.3 5.0		5.0 5.0	5.0 5.0	5.0 5.0	ns
t _{w(L)}	Pulse Width, SCLR	3.3 5.0		5.0 5.0	5.0 5.0	5.0 5.0	ns

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SWITCHING WAVEFORMS

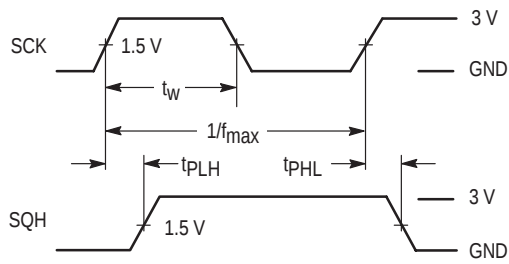


Figure 2.

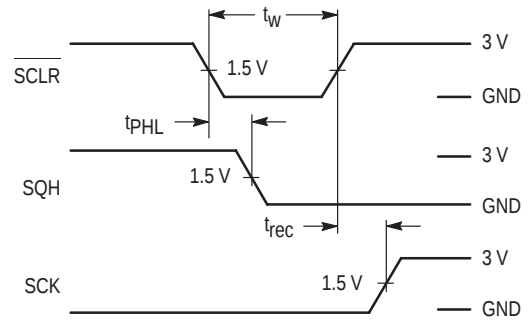


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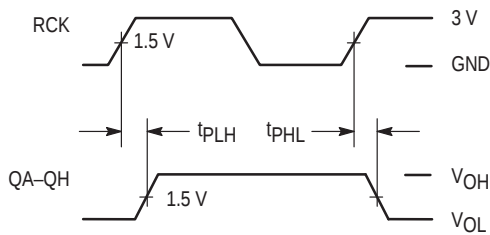


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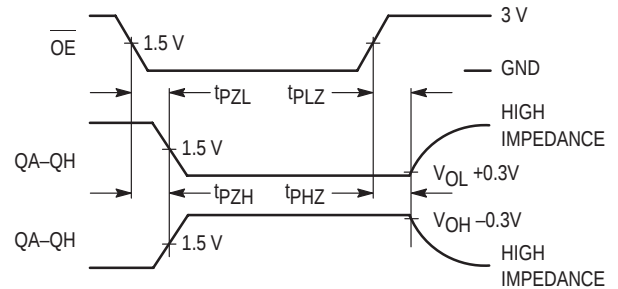


Figure 5.

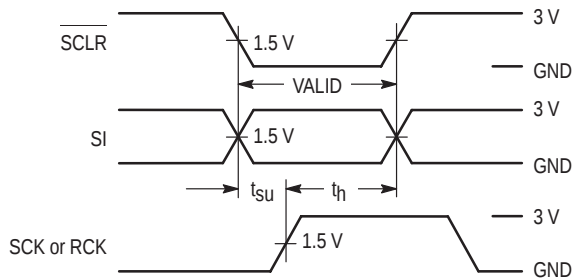


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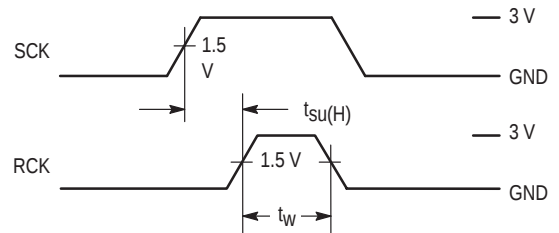
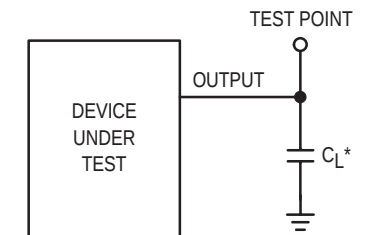


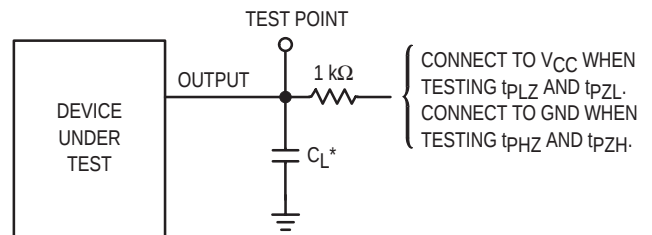
Figure 7.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 8.

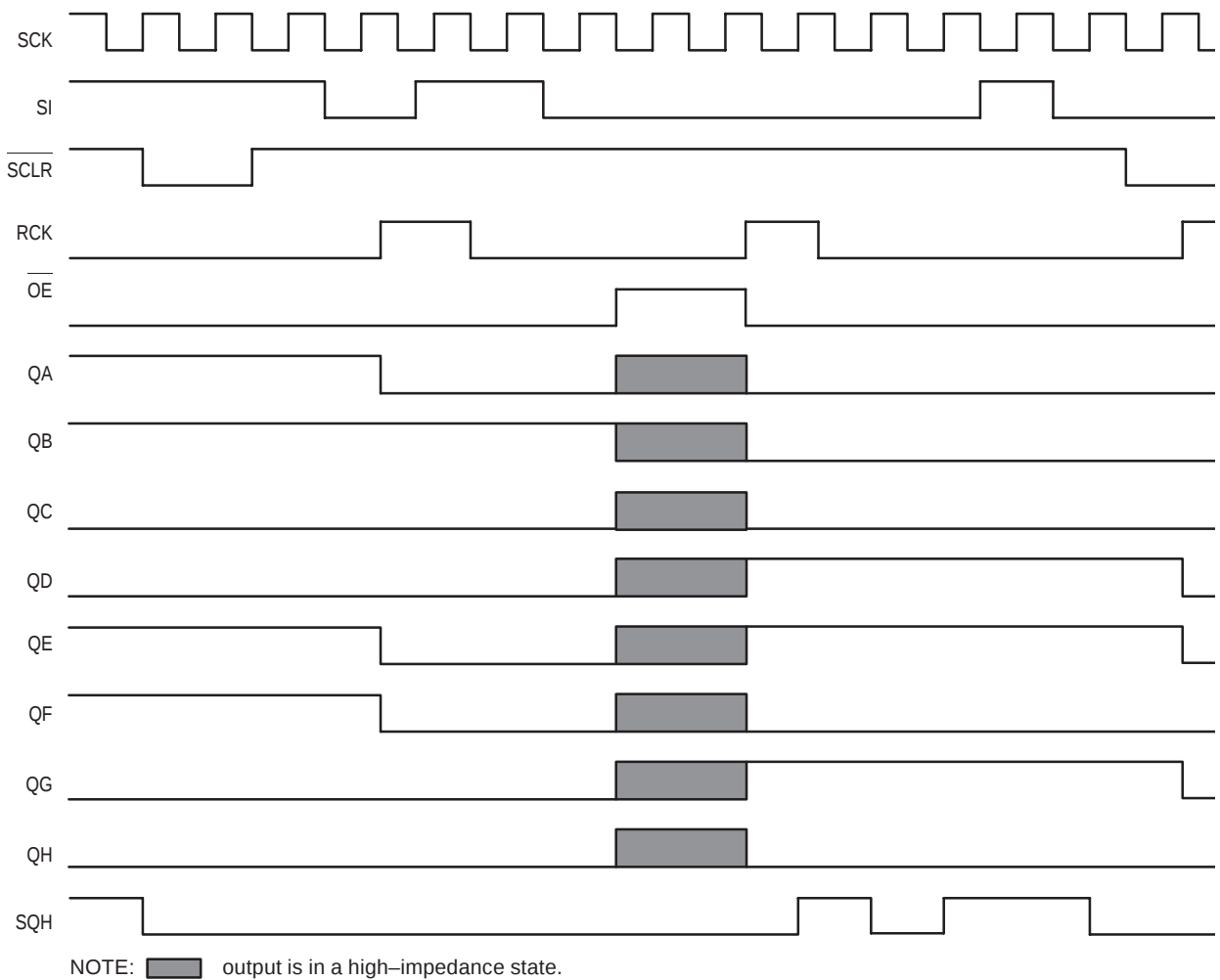


*Includes all probe and jig capacitance

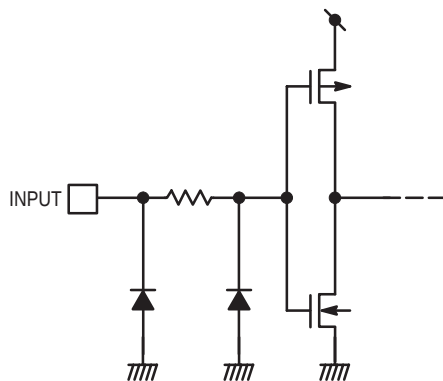
Figure 9.

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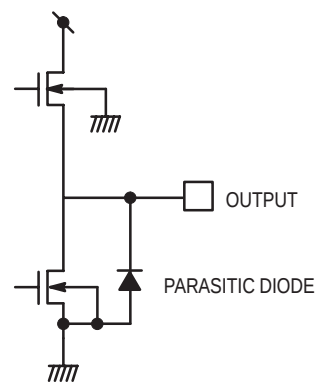
TIMING DIAGRAM



INPUT EQUIVALENT CIRCUIT



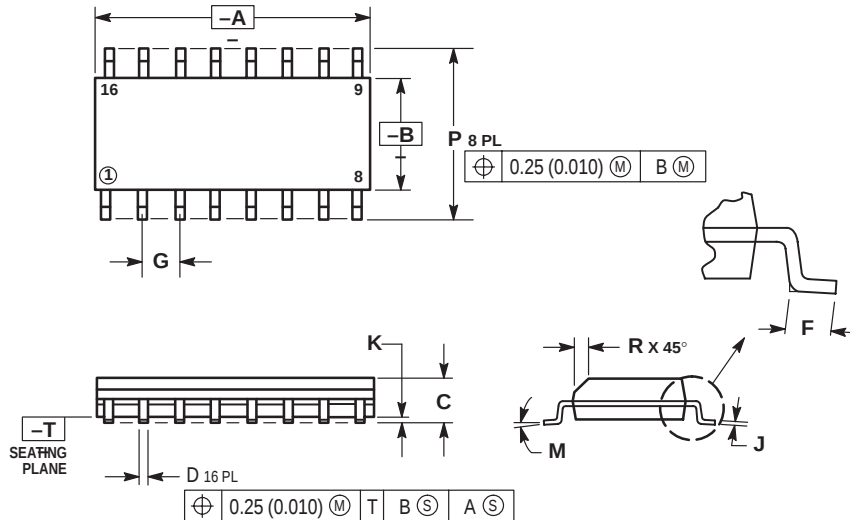
OUTPUT EQUIVALENT CIRCUIT



MC74VHCT595A

PACKAGE DIMENSIONS

SOIC-16 D SUFFIX CASE 751B-05 ISSUE J

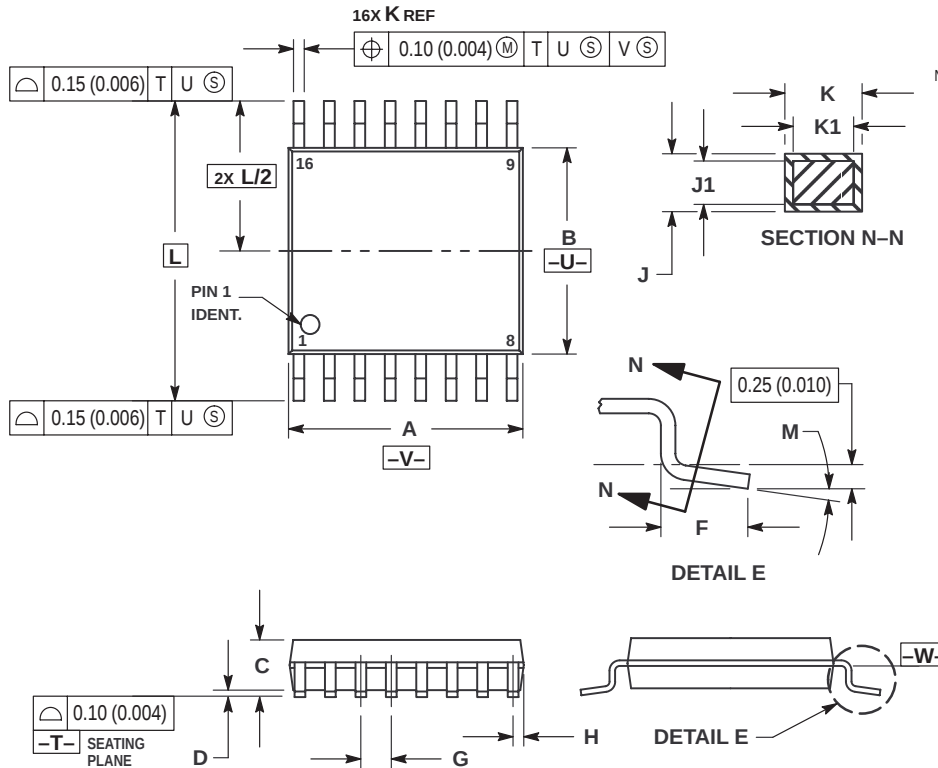


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

TSSOP-16 DT SUFFIX CASE 948F-01 ISSUE O



NOTES:

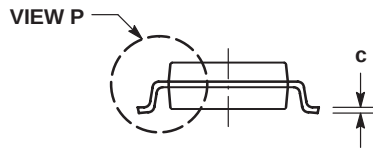
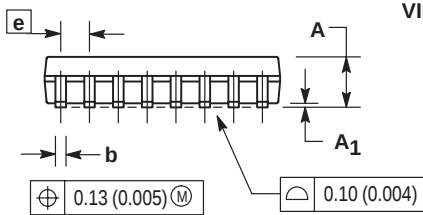
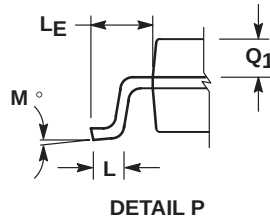
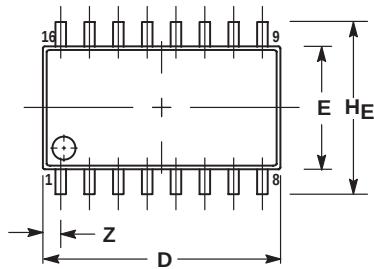
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74VHCT595A

PACKAGE DIMENSIONS

SOIC EIAJ-16
M SUFFIX
CASE 966-01
ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	—	0.78	—	0.031

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