MC74VHCT259A

Product Preview

8-Bit Addressable Latch/1-of-8 Decoder CMOS Logic Level Shifter

with LSTTL–Compatible Inputs

The MC74VHCT259 is an 8–bit Addressable Latch fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The VHC259 is designed for general purpose storage applications in digital systems. The device has four modes of operation as shown in the mode selection table.. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non–addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one–of–eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode, all outputs are LOW and unaffected by the address and data inputs. When operating the VHCT259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V because it has full 5 V CMOS level output swings.

The VHCT259A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when V_{CC} = 0 V. These input and output structures help prevent device destruction caused by supply voltage—input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: t_{PD} = 7.6 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2.0 V
- Power Down Protection Provided on Inputs and Outputs
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V

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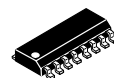
http://onsemi.com

MARKING DIAGRAMS

SOIC–16
D SUFFIX
CASE 751B

VHCT259A
AWLYYWW

TSSOP–16
DT SUFFIX
CASE 948F

VHCT
259A
AWLYWW
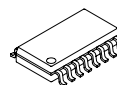
SOIC EIAJ–16
M SUFFIX
CASE 966
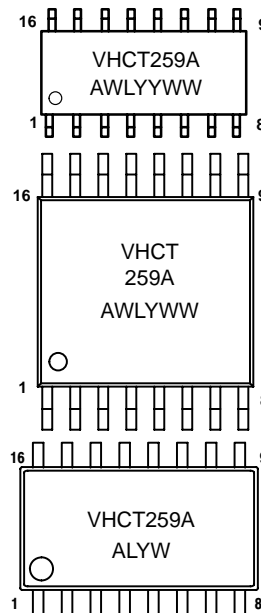
VHCT259A
ALYW

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week

A	= Assembly Location	A	= Assembly Location
WL	= Wafer Lot	L	= Wafer Lot
Y	= Year	Y	= Year
WW	= Work Week	W	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74VHCT259AD	SOIC–16	48 Units/Rail
MC74VHCT259ADR2	SOIC–16	2500 Units/Reel
MC74VHCT259ADT	TSSOP–16	96 Units/Rail
MC74VHCT259ADTEL	TSSOP–16	2000 Units/Reel
MC74VHCT259ADTR2	TSSOP–16	2500 Units/Reel
MC74VHCT259AM	SOIC EIAJ–16	50 Units/Rail
MC74VHCT259AMEL	SOIC EIAJ–16	2000 Units/Reel

MC74VHCT259A

PIN ASSIGNMENT

A0	1 ●	16	V$_{CC}$
A1	2	15	RESET
A2	3	14	ENABLE
Q0	4	13	DATA IN
Q1	5	12	Q7
Q2	6	11	Q6
Q3	7	10	Q5
GND	8	9	Q4

LOGIC DIAGRAM

ADDRESS INPUTS
A0 1
A1 2
A2 3

DATA IN 13

RESET 15
ENABLE 14

4 Q0
5 Q1
6 Q2
7 Q3
9 Q4
10 Q5
11 Q6
12 Q7

NONINVERTING OUTPUTS

PIN 16 = V$_{CC}$
PIN 8 = GND
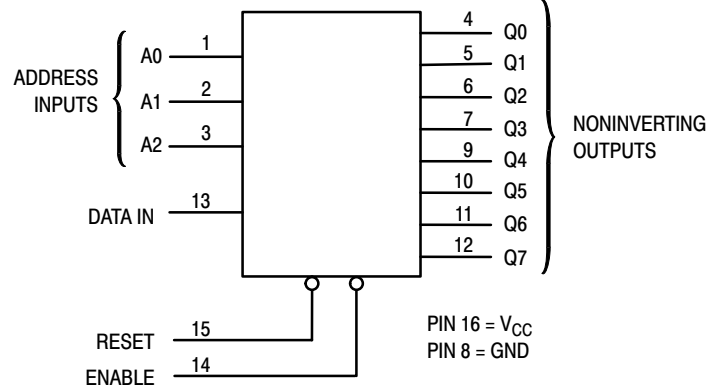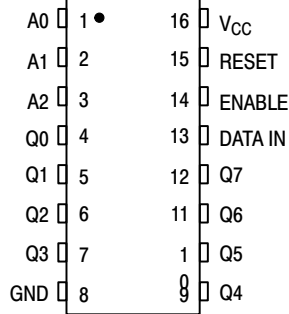
MODE SELECTION TABLE

Enable	Reset	Mode
L	H	Addressable Latch
H	H	Memory
L	L	8–Line Demultiplexer
H	L	Reset

LATCH SELECTION TABLE

Address Inputs			Latch Addressed
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

IEC LOGIC SYMBOL

BIN/OCT

A0 1 — 1
A1 2 — 2
A2 3 — 4

13 — ID
14 — EN
15 — R

0 — 4 — Q0
1 — 5 — Q1
2 — 6 — Q2
3 — 7 — Q3
4 — 8 — Q4
5 — 10 — Q5
6 — 11 — Q6
7 — 12 — Q7

DMUX

A0 1 — 0
A1 2 — 1 G $\frac{0}{7}$
A2 3 — 2

13 — ID
14 — EN
15 — R

0 — 4 — Q0
1 — 5 — Q1
2 — 6 — Q2
3 — 7 — Q3
4 — 8 — Q4
5 — 10 — Q5
6 — 11 — Q6
7 — 12 — Q7
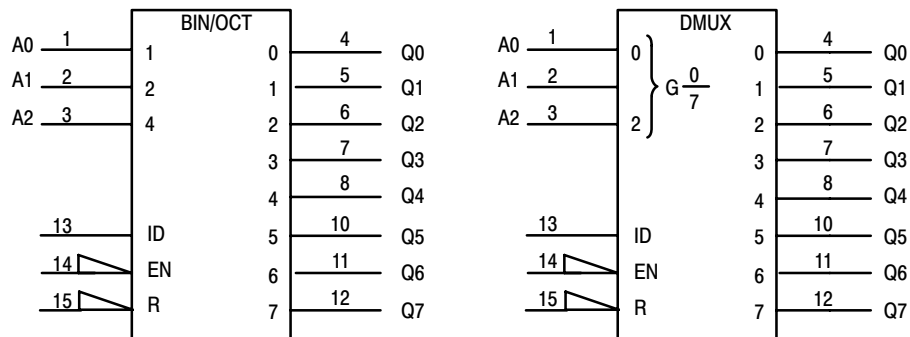
MC74VHCT259A

EXPANDED LOGIC DIAGRAM

DATA INPUT — 13

A0
A1   ADDRESS INPUTS
A2

3 TO 8 DECODER

ENABLE — 14

RESET — 15

D — 4 Q0
D — 5 Q1
D — 6 Q2
D — 7 Q3
D — 9 Q4
D — 10 Q5
D — 11 Q6
D — 12 Q7
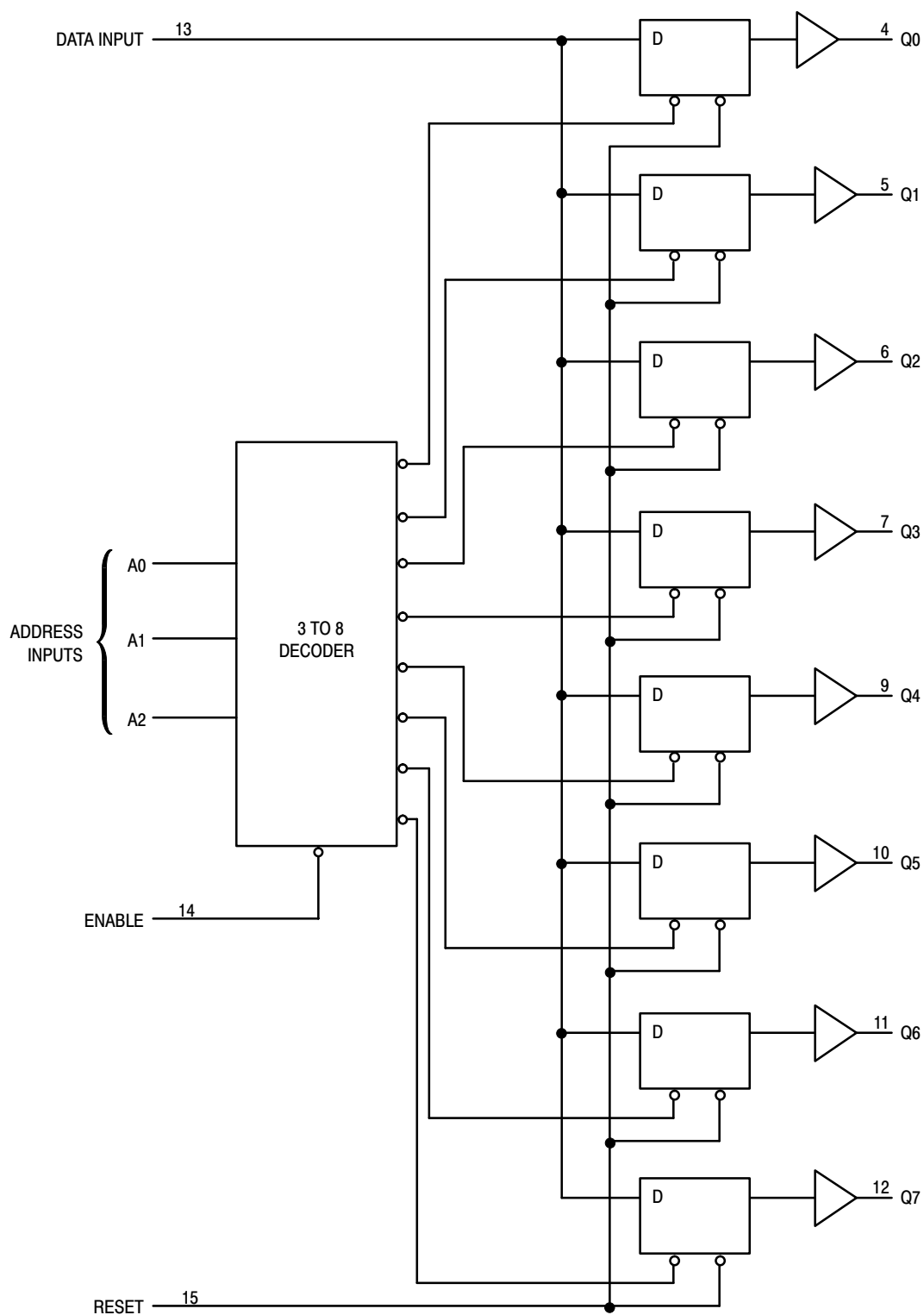
MC74VHCT259A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	− 0.5 to + 7.0	V
V_{in}	DC Input Voltage	− 0.5 to + 7.0	V
V_{out}	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	− 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	− 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: − 7 mW/°C from 65° to 125°C
                    TSSOP Package: − 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	3.0	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage V_{CC} = 0 High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature	− 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time V_{CC} =5.0V ±0.5V	0	20	ns/V

The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS
TIME TO 0.1% BOND FAILURES

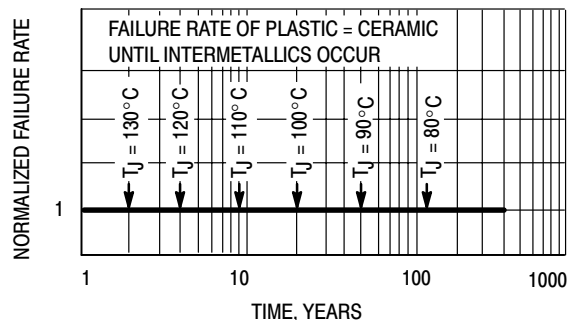| Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Figure 1. Failure Rate vs. Time
Junction Temperature

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A \leq 85°C$ Min	$T_A \leq 85°C$ Max	$T_A \leq 125°C$ Min	$T_A \leq 125°C$ Max	Unit
V_{IH}	Minimum High–Level Input Voltage		3.0 4.5 5.5	1.2 2.0 2.0			1.2 2.0 2.0		1.2 2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50 \mu A$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4$ mA $I_{OH} = -8$ mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50 \mu A$	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4$ mA $I_{OL} = 8$ mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5$ V or GND	0 to 5.5			± 0.1		± 1.0		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		40.0		40.0	μA
I_{CCT}	Quiescent Supply Current	Input: $V_{IN} = 3.4$ V	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	$V_{OUT} = 5.5$ V	0.0			0.5		5.0		10	mA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A \leq 85°C$ Min	$T_A \leq 85°C$ Max	$T_A \leq 125°C$ Min	$T_A \leq 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Data to Output Fig. 2. and 7.	$V_{CC} = 3.3 \pm 0.3$V	$C_L = 15$pF $C_L = 50$pF			11.0 16.0	1.0 1.0	13.0 18.0	1.0 1.0	13.0 18.0	ns
		$V_{CC} = 5.0 \pm 0.5$V	$C_L = 15$pF $C_L = 50$pF			8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Address Select to Output Fig. 3. and 7.	$V_{CC} = 3.3 \pm 0.3$V	$C_L = 15$pF $C_L = 50$pF			11.0 16.0	1.0 1.0	13.0 18.0	1.0 1.0	13.0 18.0	ns
		$V_{CC} = 5.0 \pm 0.5$V	$C_L = 15$pF $C_L = 50$pF			8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Enable to Output Fig. 4. and 7.	$V_{CC} = 3.3 \pm 0.3$V	$C_L = 15$pF $C_L = 50$pF			11.0 16.0	1.0 1.0	13.0 18.0	1.0 1.0	13.0 18.0	ns
		$V_{CC} = 5.0 \pm 0.5$V	$C_L = 15$pF $C_L = 50$pF			8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
t_{PHL}	Maximum Propagation Delay, Reset to Output Fig. 5. and 7.	$V_{CC} = 3.3 \pm 0.3$V	$C_L = 15$pF $C_L = 50$pF			11.0 16.0	1.0 1.0	13.0 18.0	1.0 1.0	13.0 18.0	ns
		$V_{CC} = 5.0 \pm 0.5$V	$C_L = 15$pF $C_L = 50$pF			8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
C_{IN}	Maximum Input Capacitance				6	10		10		10	pF

			Typical @ 25°C, $V_{CC} = 5.0$V	
C_{PD}	Power Dissipation Capacitance (Note 1.)		30	pF

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1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$			$T_A = \leq 85°C$		$T_A = \leq 125°C$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_w	Minimum Pulse Width, Reset or Enable Fig. 6.	$V_{CC} = 3.3 \pm 0.3V$	5.0			5.5		5.5		ns
		$V_{CC} = 5.0 \pm 0.5V$	5.0			5.5		5.5		
t_{su}	Minimum Setup Time, Address or Data to Enable Fig. 6.	$V_{CC} = 3.3 \pm 0.3V$	4.5			4.5		4.5		ns
		$V_{CC} = 5.0 \pm 0.5V$	3.0			3.0		3.0		
t_h	Minimum Hold Time, Enable to Address or Data Fig. 4. or 5.	$V_{CC} = 3.3 \pm 0.3V$	2.0			2.0		2.0		ns
		$V_{CC} = 5.0 \pm 0.5V$	2.0			2.0		2.0		
t_r, t_f	Maximum Input, Rise and Fall Times Fig. 2.	$V_{CC} = 3.3 \pm 0.3V$			400		300		300	ns
		$V_{CC} = 5.0 \pm 0.5V$			200		100		100	

SWITCHING WAVEFORMS
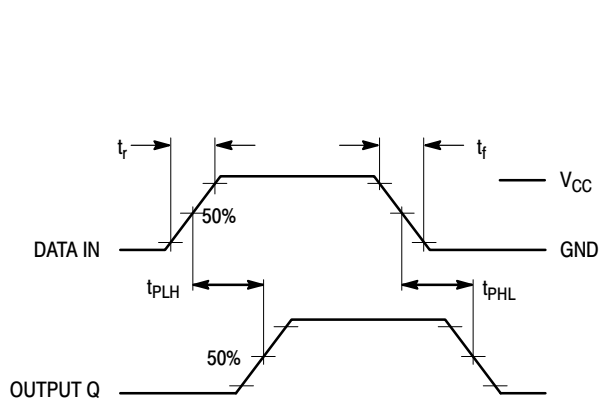
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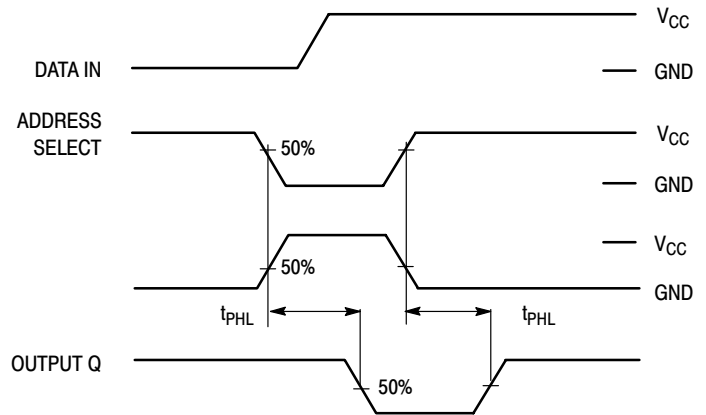
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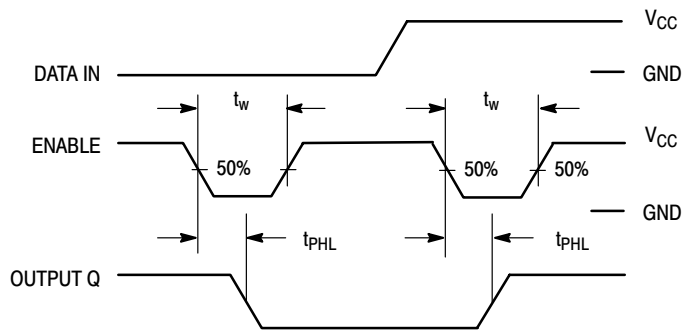
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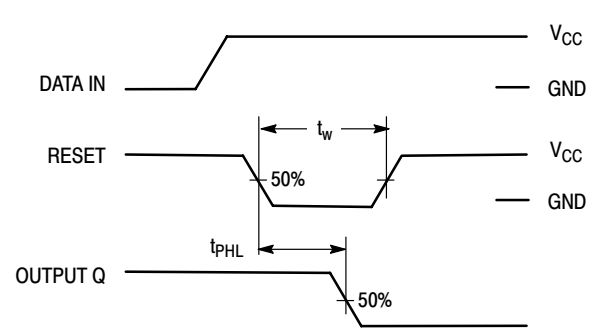
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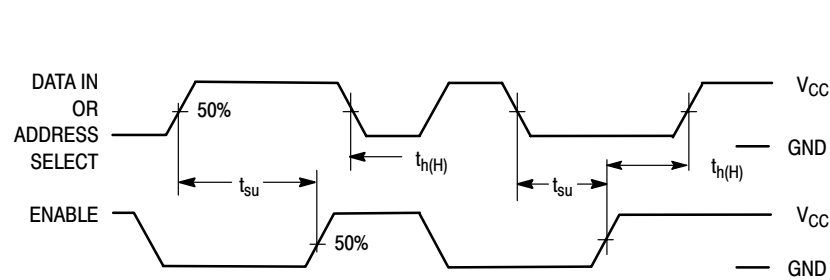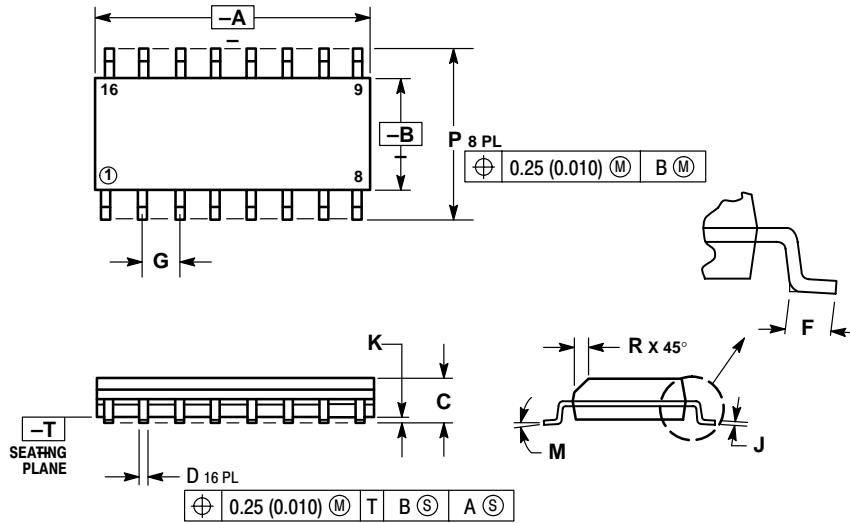

Figure 6.
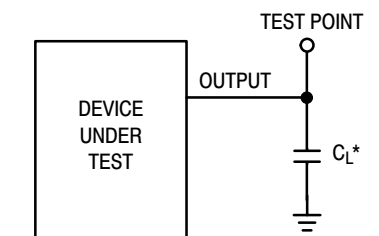
*Includes all probe and jig capacitance

Figure 7. Test Circuit

MC74VHCT259A

PACKAGE DIMENSIONS

SOIC–16
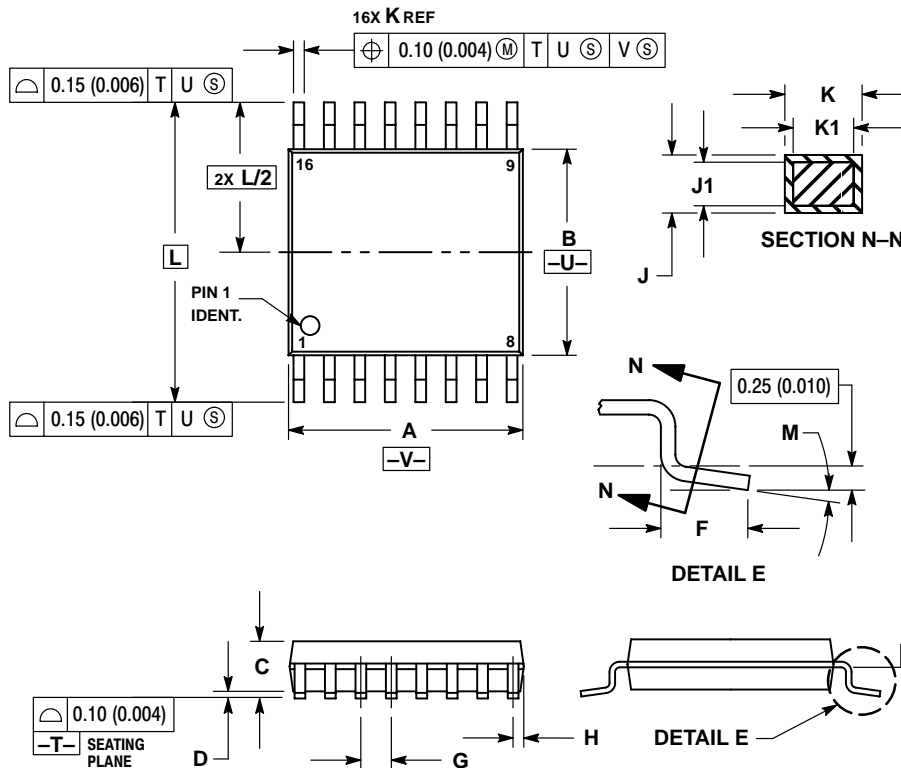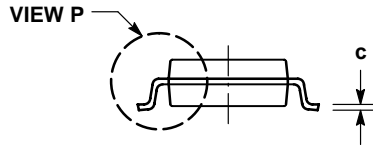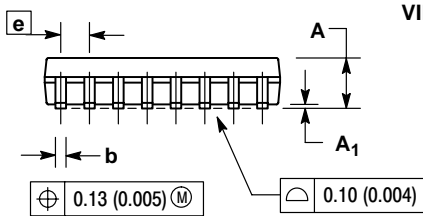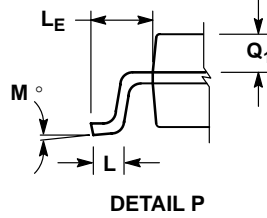**D SUFFIX**
CASE 751B–05
ISSUE J

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

TSSOP–16
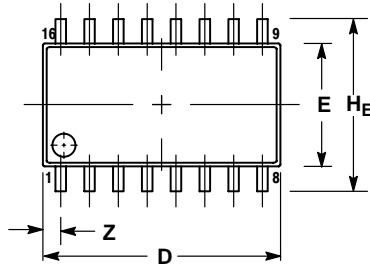**DT SUFFIX**
CASE 948F–01
ISSUE O

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

SECTION N–N

DETAIL E

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74VHCT259A

PACKAGE DIMENSIONS

SOIC EIAJ–16
M SUFFIX
CASE 966–01
ISSUE O

DETAIL P

VIEW P

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

Notes

<u>Notes</u>

PUBLICATION ORDERING INFORMATION

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