

MC74VHCT257A

Advance Information

Quad 2-Channel Multiplexer with 3-State Outputs

The MC74VHCT257A is an advanced high speed CMOS quad 2-channel multiplexer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

It consists of four 2-input digital multiplexers with common select (S) and enable (OE) inputs. When (OE) is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the A or B inputs get routed to the corresponding Y outputs.

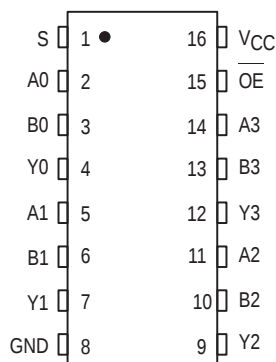
The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V because it has full 5 V CMOS level output swings.

The VHCT257A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage—input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

- High Speed: $t_{PD} = 4.1\text{ns}$ (Typ) at $V_{CC} = 5\text{V}$
- Low Power Dissipation: $I_{CC} = 4\mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- TTL-Compatible Inputs: $V_{IL} = 0.8\text{V}$; $V_{IH} = 2.0\text{V}$
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: $V_{OLP} = 0.8\text{V}$ (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.



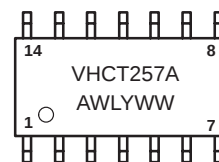
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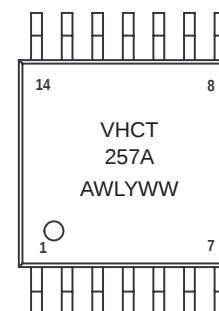
MARKING DIAGRAMS



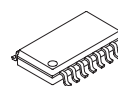
SOIC-14
D SUFFIX
CASE 751A



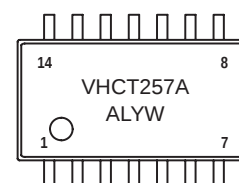
TSSOP-14
DT SUFFIX
CASE 948G



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week



SOIC EIAJ-14
M SUFFIX
CASE 965



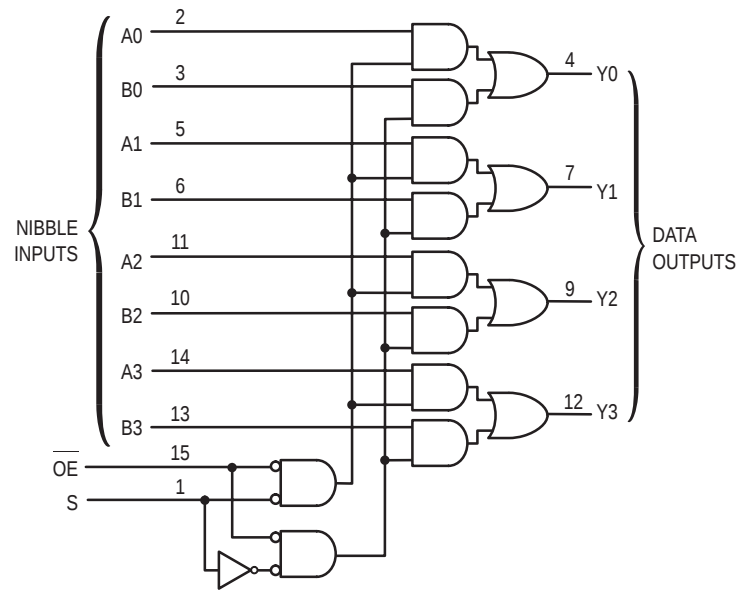
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74VHCT257AD	SOIC-14	55 Units/Rail
MC74VHCT257ADT	TSSOP-14	96 Units/Rail
MC74VHCT257AM	SOIC EIAJ-14	50 Units/Rail

MC74VHCT257A

EXPANDED LOGIC DIAGRAM

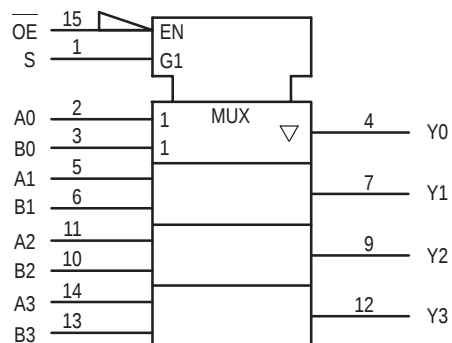


FUNCTION TABLE

Inputs		Outputs
OE	S	Y0 – Y3
H	X	L
L	L	A0–A3
L	H	B0–B3

A0 – A3, B0 – B3 = the levels of the respective Data-Word Inputs.

IEC LOGIC SYMBOL



MC74VHCT257A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V _{IN}	DC Input Voltage	– 0.5 to + 7.0	V
V _{OUT}	DC Output Voltage	– 0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current	– 20	mA
I _{OK}	Output Diode Current	± 20	mA
I _{OUT}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	3.0	5.5	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature	– 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time V _{CC} = 5.0 V ± 0.5 V	0	20	ns/V

The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

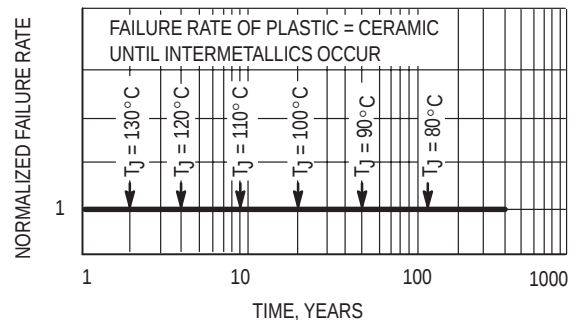


Figure 1. Failure Rate vs. Time Junction Temperature

MC74VHCT257A

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			T _A = ≤ 85°C		T _A = ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0		V
V _{IL}	Maximum Low-Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0		± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			2.0		40.0		40.0	μA
I _{CCT}	Quiescent Supply Current	Input: V _{IN} = 3.4 V	5.5			1.35		1.50		1.50	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0.0			0.5		5.0		5.0	mA
I _{OZ}	Maximum 3-State Leakage Current	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5			± 0.25		± 2.5		± 2.5	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A = ≤ 85°C		T _A = ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A or B to Y	V _{CC} = 3.3 ± 0.3V C _L = 15pF C _L = 50pF		5.8 8.3	9.3 12.8	1.0 1.0	11.0 14.5	1.0 1.0	11.0 14.5	ns
		V _{CC} = 5.0 ± 0.5V C _L = 15pF C _L = 50pF		3.6 5.1	5.9 7.9	1.0 1.0	7.0 9.0	1.0 1.0	7.0 9.0	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, S to Y	V _{CC} = 3.3 ± 0.3V C _L = 15pF C _L = 50pF		7.0 9.5	11.0 14.5	1.0 1.0	13.0 16.5	1.0 1.0	13.0 16.5	ns
		V _{CC} = 5.0 ± 0.5V C _L = 15pF C _L = 50pF		4.0 5.5	6.8 8.8	1.0 1.0	8.0 10.0	1.0 1.0	8.0 10.0	
t _{PZL} , t _{PZH}	Maximum Output Enable, Time, OE to Y	V _{CC} = 3.3 ± 0.3V C _L = 15pF R _L = 1 kΩ C _L = 50pF		6.7 9.2	10.5 14.0	1.0 1.0	12.5 16.0	1.0 1.0	12.5 16.0	ns
		V _{CC} = 5.0 ± 0.5V C _L = 15pF R _L = 1 kΩ C _L = 50pF		3.6 5.1	6.8 8.8	1.0 1.0	8.0 10.0	1.0 1.0	8.0 10.0	
t _{PLZ} , t _{PHZ}	Maximum Output Disable, Time, OE to Y	V _{CC} = 5.0 ± 0.5V C _L = 50pF R _L = 1 kΩ		8.6	12.0	1.0	13.5	1.0	13.5	ns
		V _{CC} = 5.0 ± 0.5V C _L = 50pF R _L = 1 kΩ		5.7	7.9	1.0	9.0	1.0	9.0	
C _{IN}	Maximum Input Capacitance			4	10		10		10	pF

C _{PD}	Power Dissipation Capacitance (Note 1.)	Typical @ 25°C, V _{CC} = 5.0 V	pF
		20	

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$, $C_L = 50\text{pF}$, $V_{CC} = 5.0\text{V}$)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.3	-0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS

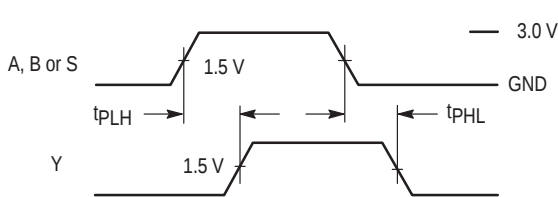


Figure 2.

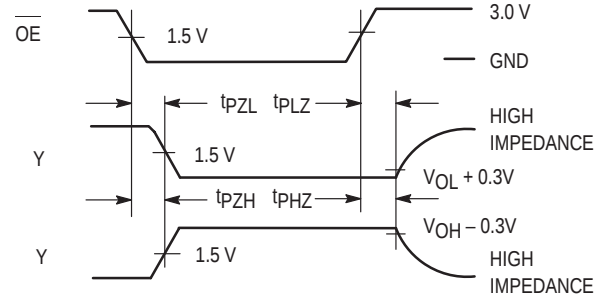
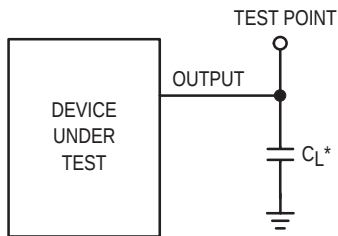
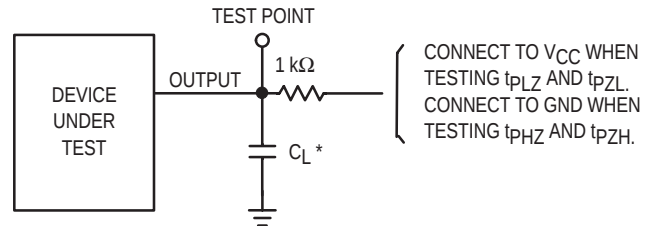


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit



*Includes all probe and jig capacitance

Figure 5. Test Circuit

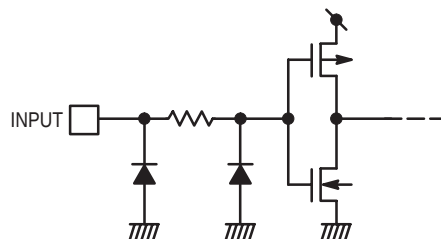
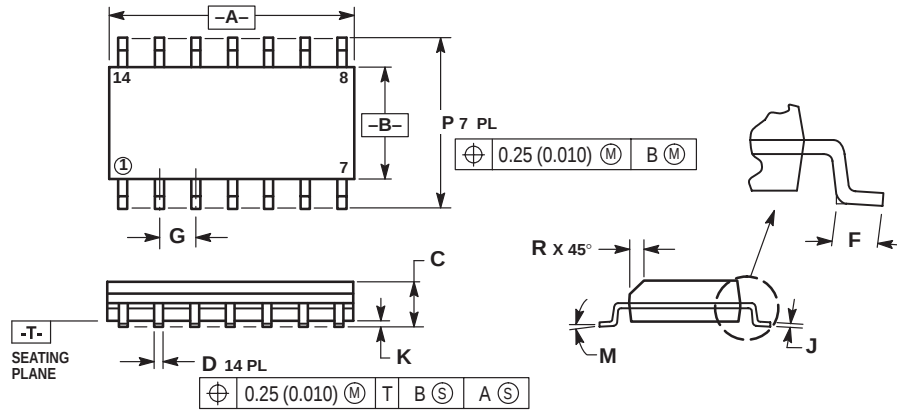


Figure 6. Input Equivalent Circuit

MC74VHCT257A

PACKAGE DIMENSIONS

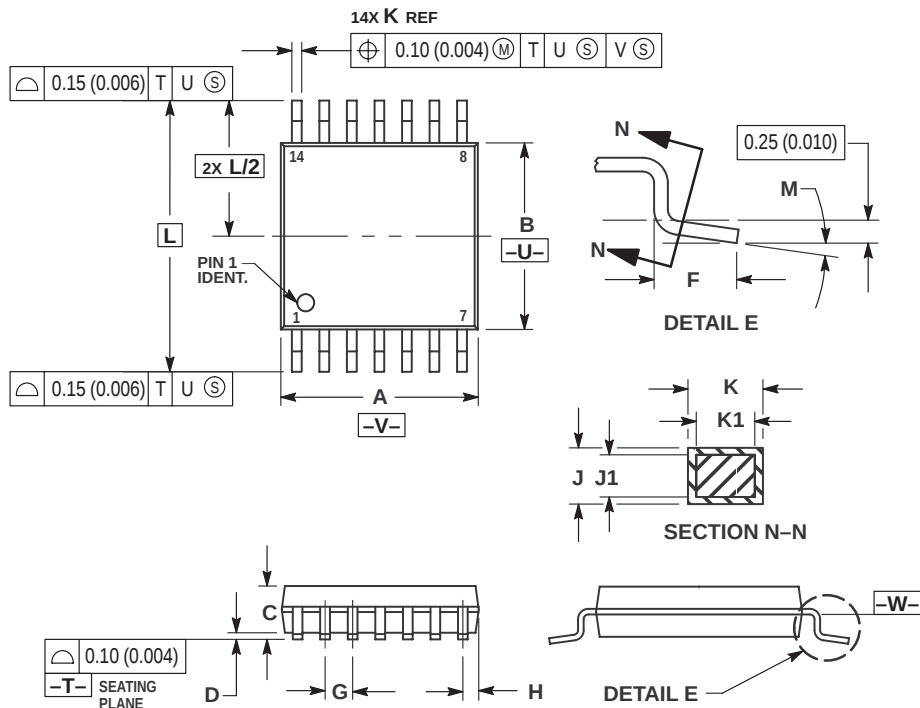
SOIC-14 D SUFFIX CASE 751A-03 ISSUE F



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

TSSOP-14 DT SUFFIX CASE 948G-01 ISSUE O



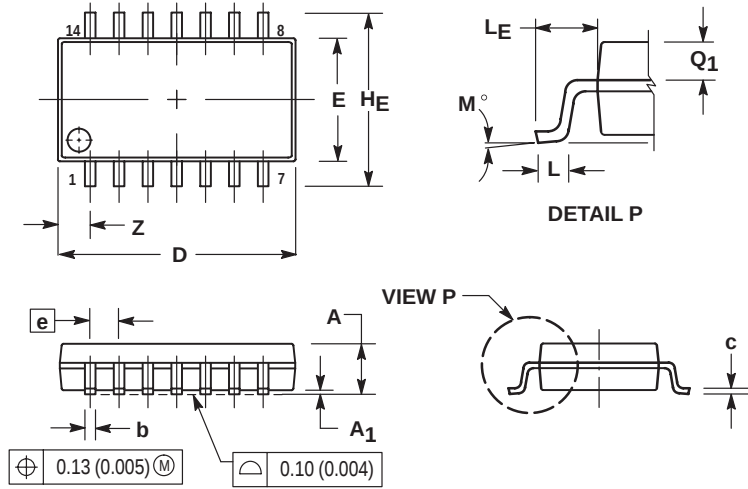
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74VHCT257A

PACKAGE DIMENSIONS

SOIC EIAJ-14
M SUFFIX
CASE 965-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	—	1.42	—	0.056

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