Advance Information

Analog Multiplexer/ Demultiplexer

High–Performance Silicon–Gate CMOS

MC74VHC4053

The MC74VHC4053 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to GND).

The VHC4053 is identical in pinout to the high–speed HC4053A, and the metal–gate MC14053B. The Channel–Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel–Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.

This device has been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal–gate CMOS analog switches.

For a multiplexer/demultiplexer with channel–select latches, see VHC4351.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Digital (Control) Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal–Gate Counterparts
- Low Noise
- In Compliance With the Requirements of JEDEC Standard No. 7A
- Chip Complexity: VHC4053 — 156 FETs or 39 Equivalent Gates

D SUFFIX
16–LEAD SOIC PACKAGE
CASE 751B–05

DT SUFFIX
16–LEAD TSSOP PACKAGE
CASE 948F–01

ORDERING INFORMATION

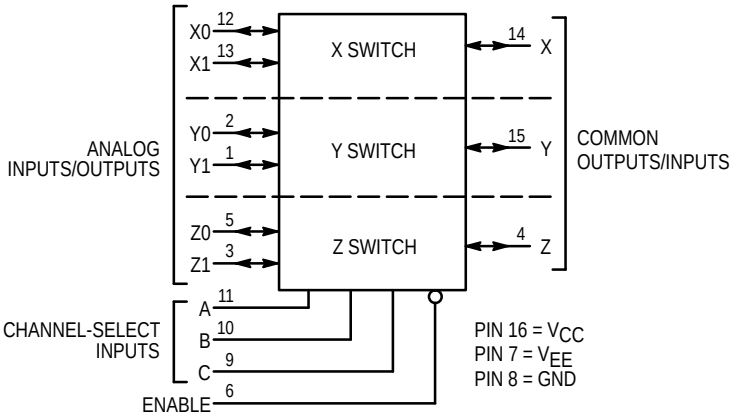
MC74VHCXXXXD	SOIC
MC74VHCXXXXDT	TSSOP

FUNCTION TABLE – MC74VHC4053

Control Inputs						
	Select					
Enable	C	B	A	ON Channels		
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	NONE		

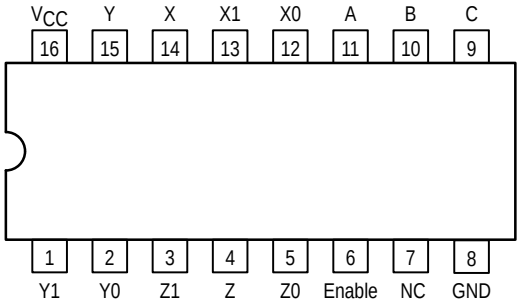
X = Don't Care

LOGIC DIAGRAM
MC74VHC4053
Triple Single–Pole, Double–Position Plus Common Off



NOTE: This device allows independent control of each switch. Channel–Select Input A controls the X–Switch, Input B controls the Y–Switch and Input C controls the Z–Switch

Pinout: MC74VHC4053 (Top View)



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{IS}	Analog Input Voltage	– 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	± 20	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IS}	Analog Input Voltage	0.0	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		100	mV
T_A	Operating Temperature Range, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs) V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	 0 0	 100 20	ns/V

* For voltage drops across switch greater than 100 mV (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
I_{in}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	V_{in} = V_{CC} or GND,	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V_{IS} = V_{CC} or GND; V_{IO} = 0 V	6.0	4	40	160	μA

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum “ON” Resistance	V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} to GND I_S ≤ 2.0 mA (Figures 1, 2)	3.0 4.5 6.0	25 18 15	30 23 20	35 28 25	Ω
		V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} or GND (Endpoints) I_S ≤ 2.0 mA (Figures 1, 2)	3.0 4.5 6.0	20 15 10	25 20 15	30 25 20	
ΔR_{on}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V_{in} = V_{IL} or V_{IH} V_{IS} = 1/2 (V_{CC} – GND) I_S ≤ 2.0 mA	3.0 4.5 6.0	15 8.0 4.0	20 12 7.0	25 15 10	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} or GND; Switch Off (Figure 3)	6.0	0.1	0.5	1.0	μA
	Maximum Off–Channel Leakage Current, Common Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} or GND; Switch Off (Figure 4)	6.0	0.1	1.0	2.0	
I_{on}	Maximum On–Channel Leakage Current, Channel–to–Channel	V_{in} = V_{IL} or V_{IH}; Switch–to–Switch = V_{CC} or GND; (Figure 5)	6.0	0.1	1.0	2.0	μA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 3 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.0 3.0 4.5 6.0	30 20 15 15	35 25 18 18	40 30 22 20	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0 3.0 4.5 6.0	4.0 3.0 1.0 1.0	6.0 5.0 2.0 2.0	8.0 6.0 2.0 2.0	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 6.0	30 20 15 15	35 25 18 18	40 30 22 20	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 6.0	20 12 8.0 8.0	25 14 10 10	30 15 12 12	ns
C_{in}	Maximum Input Capacitance, Channel–Select or Enable Inputs		10	10	10	pF
$C_{I/O}$	Maximum Capacitance — Analog I/O		35	35	35	pF
	(All Switches Off) — Common O/I		50	50	50	
	Feedthrough		1.0	1.0	1.0	

C_{PD}		Typical @ 25°C, V_{CC} = 5.0 V	pF
	Power Dissipation Capacitance (Figure 13)*	45	

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f_{in} = 1MHz Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{OS}; Increase f_{in} Frequency Until dB Meter Reads –3dB; R_L = 50Ω, C_L = 10pF	3.0 4.50 6.00	120 120 120	MHz
—	Off–Channel Feedthrough Isolation (Figure 7)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	3.0 4.50 6.00	–50 –50 –50	dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	3.0 4.50 6.00	–40 –40 –40	
—	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 8)	V_{in} ≤ 1MHz Square Wave (t_r = t_f = 6ns); Adjust R_L at Setup so that I_S = 0A; Enable = GND R_L = 600Ω, C_L = 50pF	3.0 4.50 6.00	25 105 135	mV_{PP}
		R_L = 10kΩ, C_L = 10pF	3.0 4.50 6.00	35 145 190	
—	Crosstalk Between Any Two Switches (Figure 12)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	3.0 4.50 6.00	–50 –50 –50	dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	3.0 4.50 6.00	–60 –60 –60	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1kHz, R_L = 10kΩ, C_L = 50pF $THD = THD_{measured} - THD_{source}$ V_{IS} = 2.0V_{PP} sine wave V_{IS} = 4.0V_{PP} sine wave V_{IS} = 5.5V_{PP} sine wave	3.0 4.50 6.00	0.10 0.08 0.05	%

* Limits not tested. Determined by design and verified by qualification.

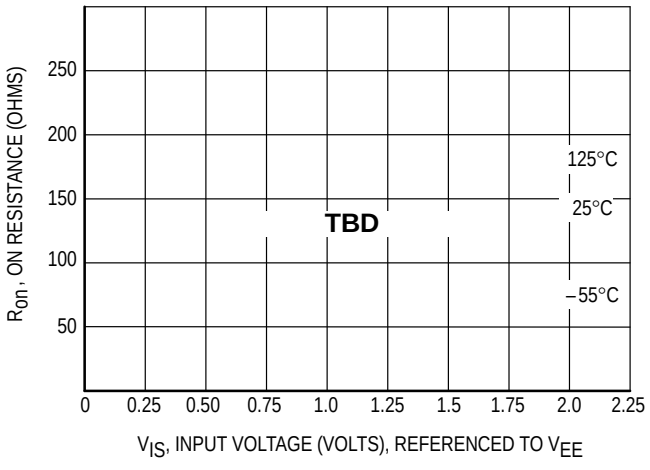


Figure 1a. Typical On Resistance, V_{CC} = 2.0 V

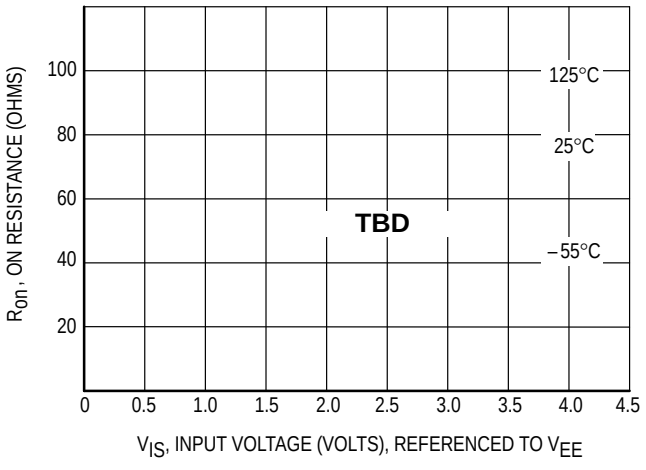


Figure 1b. Typical On Resistance, V_{CC} = 3.0 V

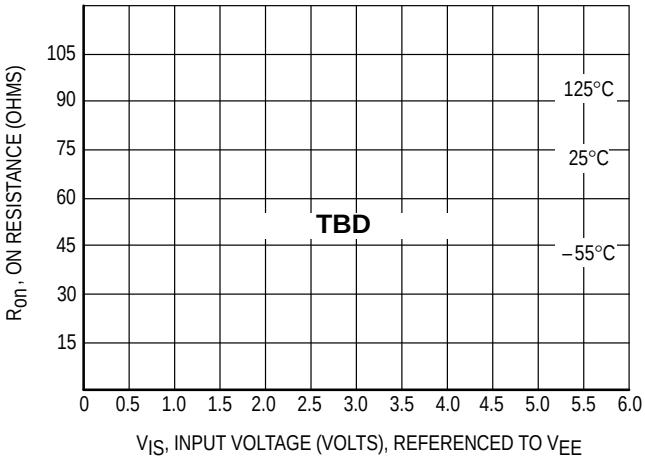


Figure 1c. Typical On Resistance, V_{CC} = 4.5 V

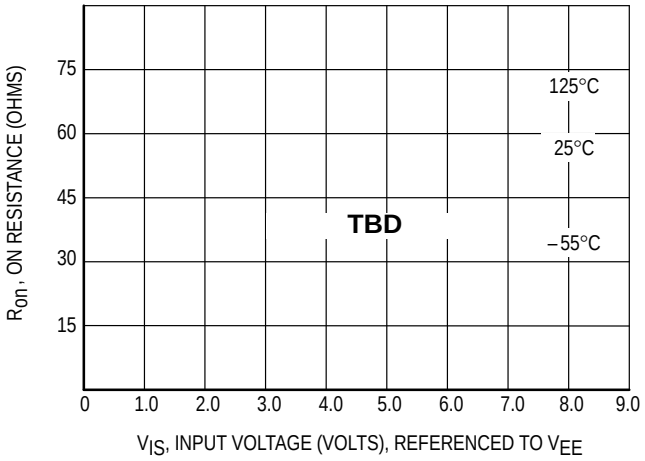


Figure 1d. Typical On Resistance, V_{CC} = 6.0 V

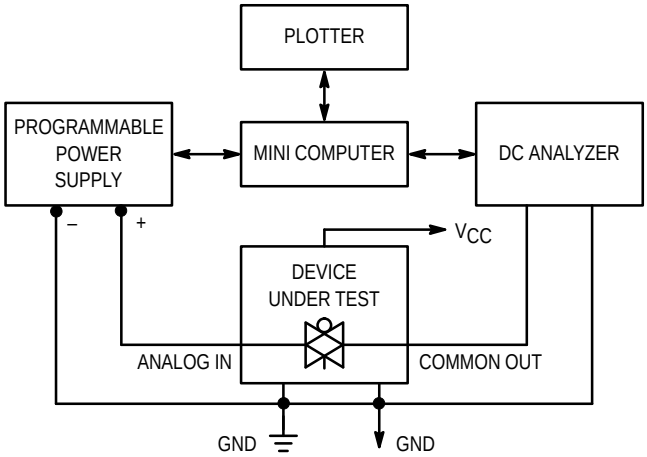


Figure 2. On Resistance Test Set–Up

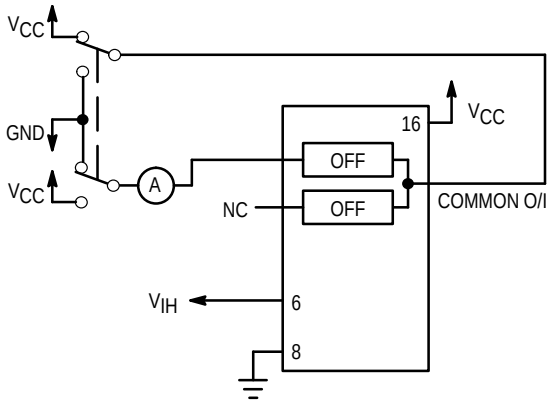


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

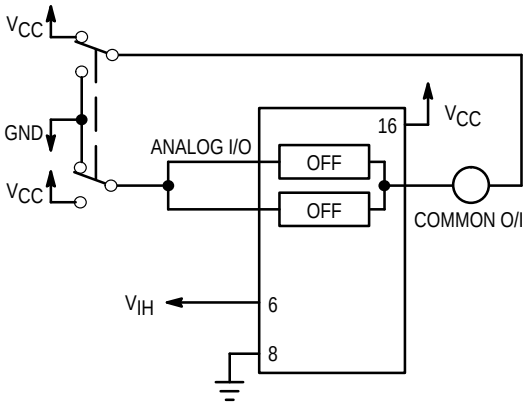


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set–Up

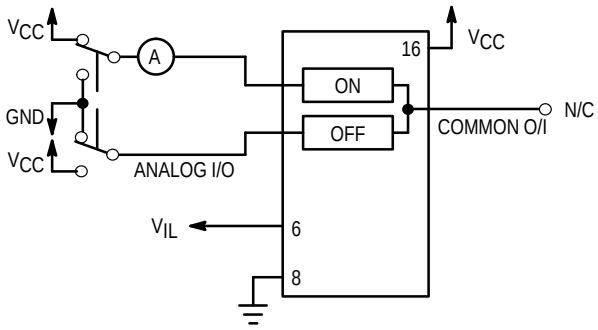
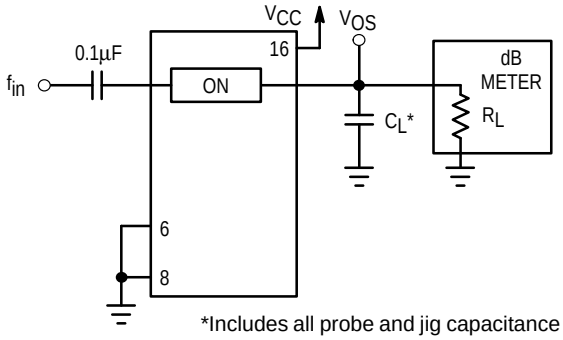
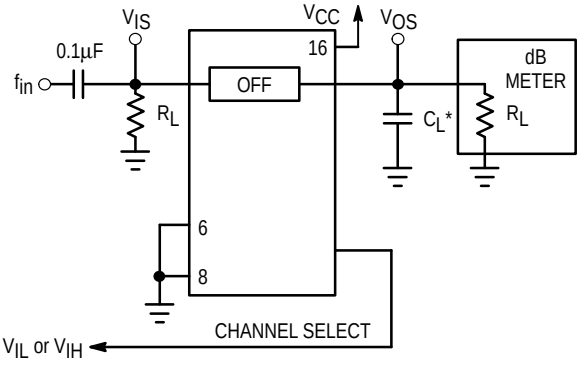


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up



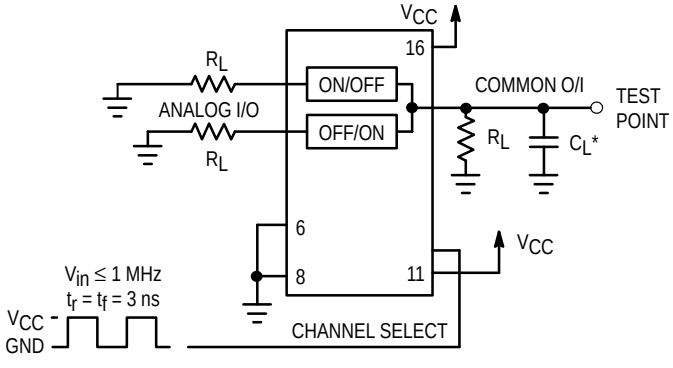
*Includes all probe and jig capacitance

Figure 6. Maximum On Channel Bandwidth, Test Set–Up



*Includes all probe and jig capacitance

Figure 7. Off Channel Feedthrough Isolation, Test Set–Up



*Includes all probe and jig capacitance

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set–Up

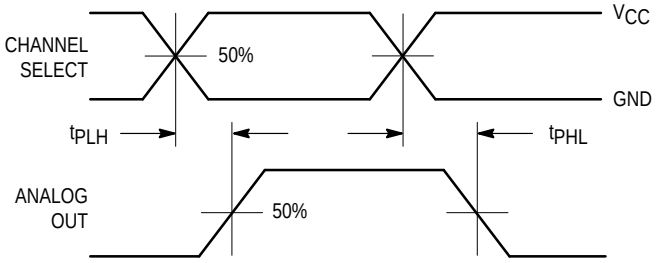
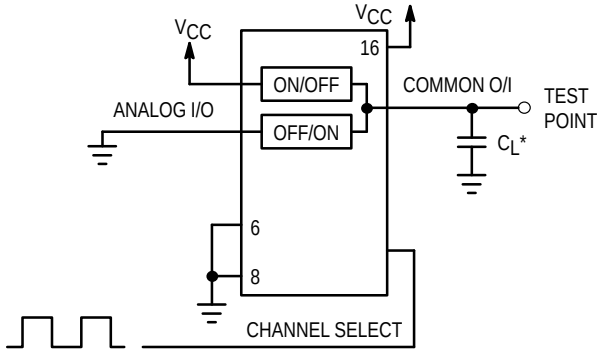


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set–Up Channel Select to Analog Out

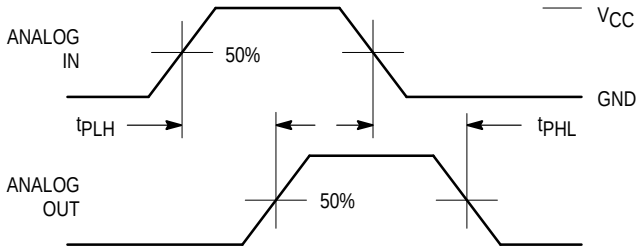
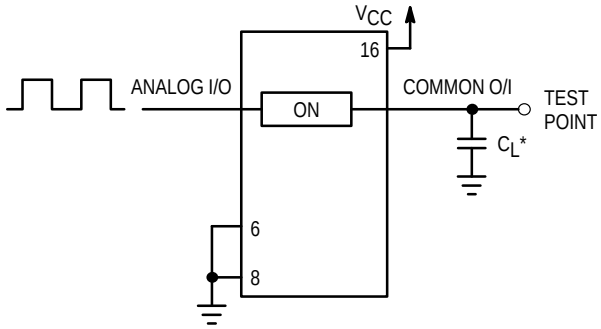


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 10b. Propagation Delay, Test Set–Up Analog In to Analog Out

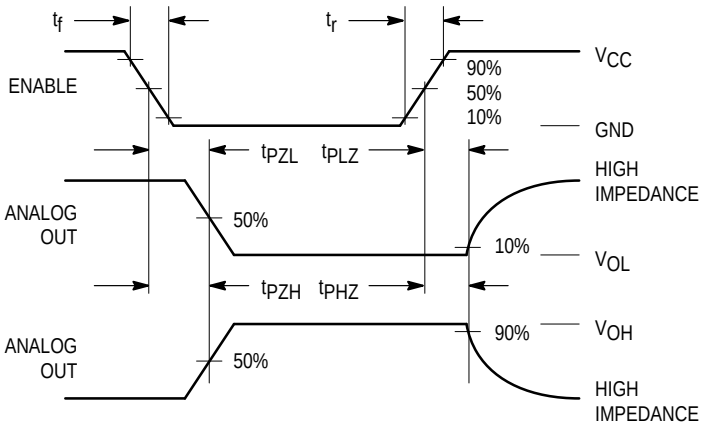


Figure 11a. Propagation Delays, Enable to Analog Out

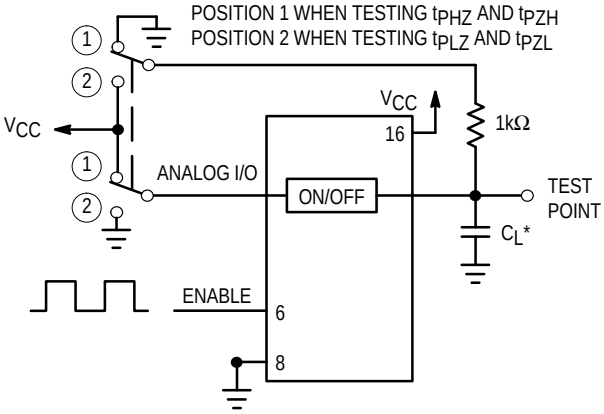
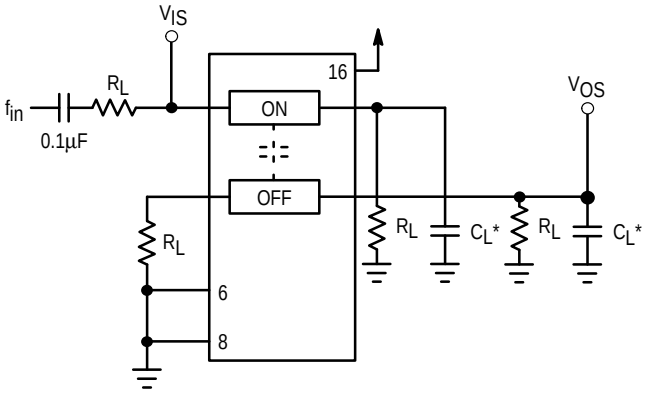


Figure 11b. Propagation Delay, Test Set–Up Enable to Analog Out



*Includes all probe and jig capacitance

Figure 12. Crosstalk Between Any Two Switches, Test Set–Up

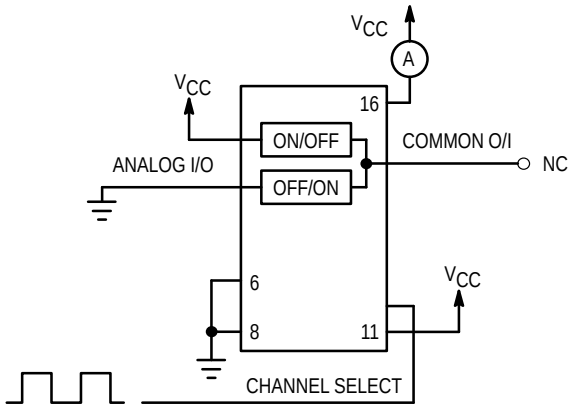
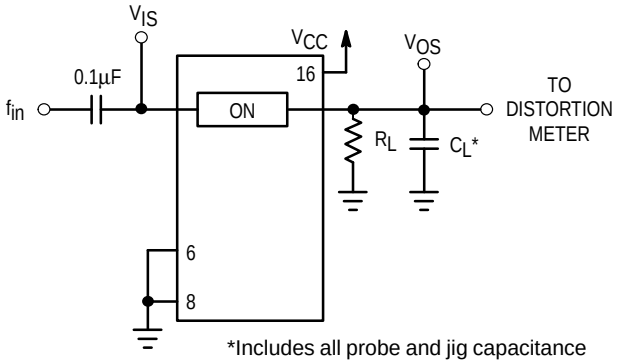


Figure 13. Power Dissipation Capacitance, Test Set–Up



*Includes all probe and jig capacitance

Figure 14a. Total Harmonic Distortion, Test Set–Up

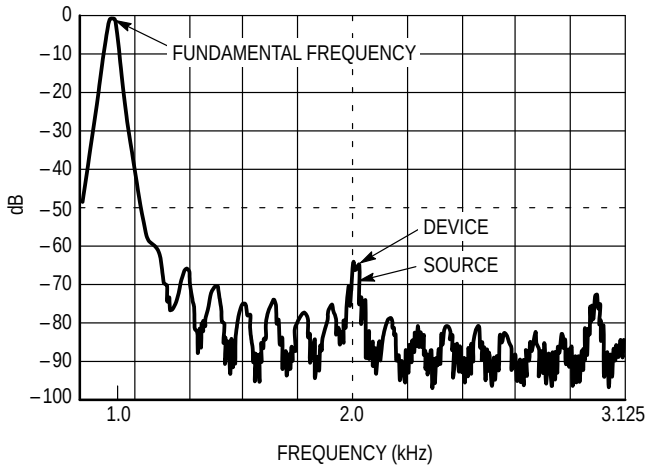


Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

V_{CC} = +5V = logic high
GND = 0V = logic low

The maximum analog voltage swing is determined by the supply voltages V_{CC}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below GND. In this example, the difference between V_{CC} and GND is five volts. Therefore, using the configuration of Figure 15, a maximum analog signal of five volts peak–to–peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

V_{CC} – GND = 2 to 6 volts

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external Germanium or Schottky diodes (D_X) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

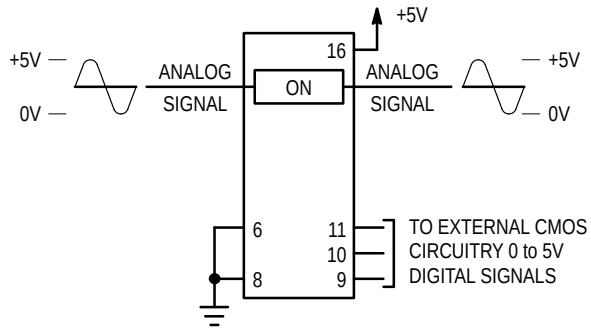


Figure 15. Application Example

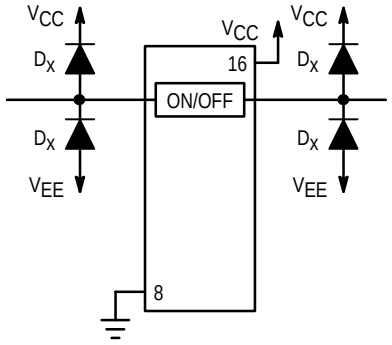
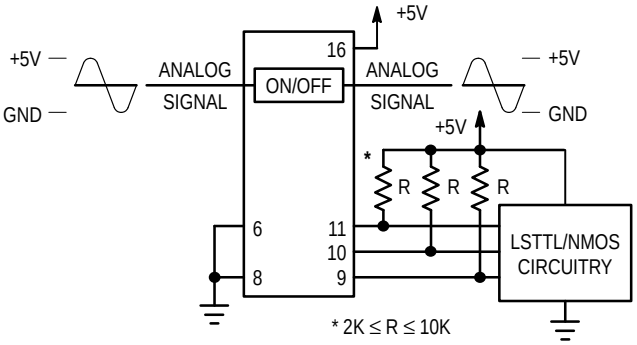
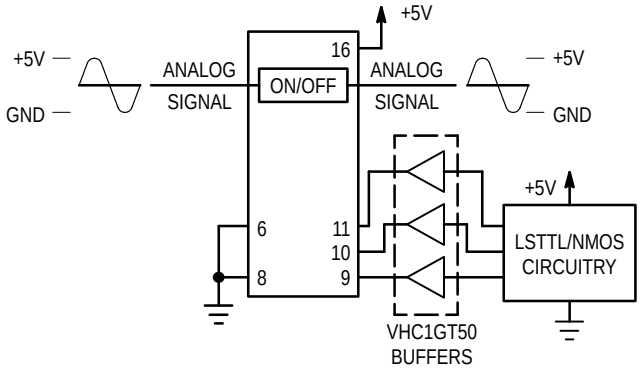


Figure 16. External Germanium or Schottky Clipping Diodes



a. Using Pull–Up Resistors



b. Using HCT Interface

Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

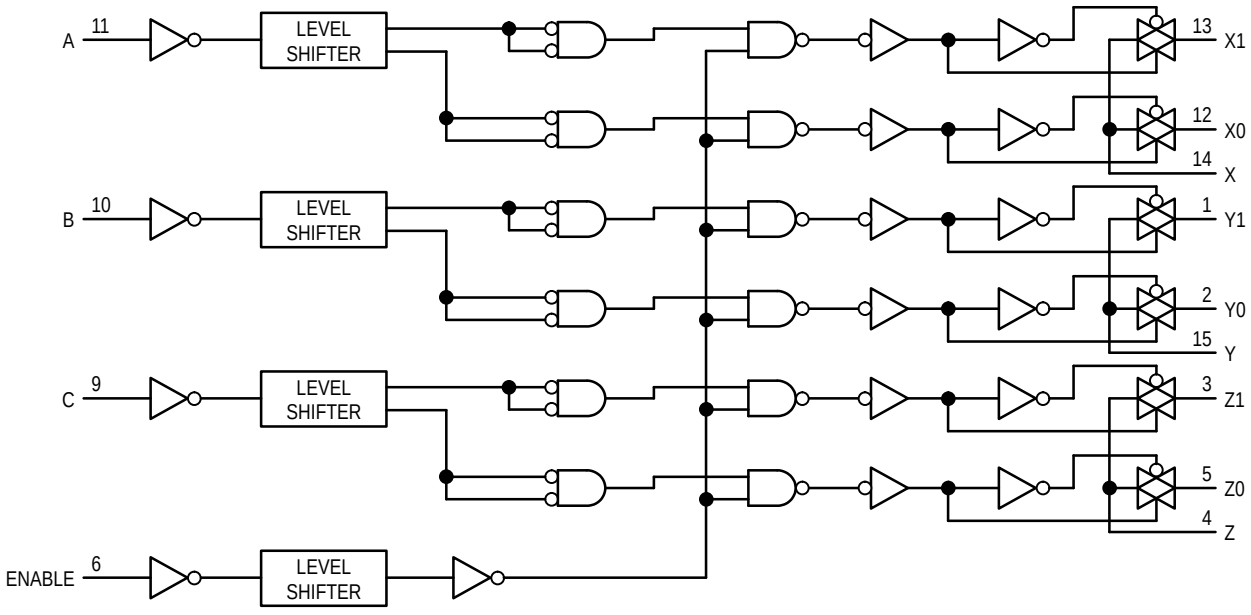
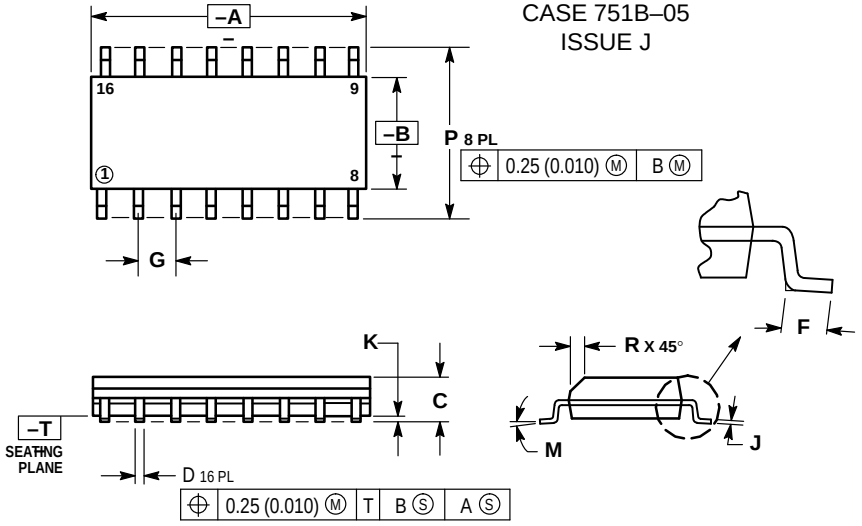


Figure 18. Function Diagram, VHC4053

OUTLINE DIMENSIONS

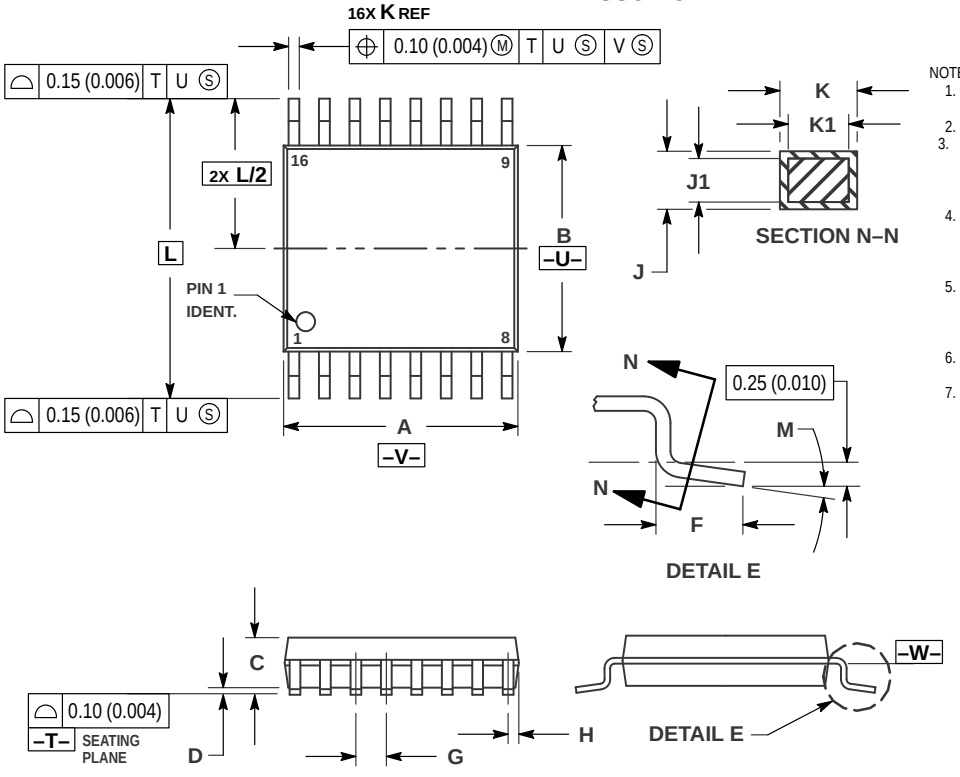
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

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