MC74VHC1GT125

Product Preview

Noninverting Buffer / CMOS Logic Level Shifter

with LSTTL–Compatible Inputs

The MC74VHC1GT125 is a single gate noninverting buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC1GT125 requires the 3–state control input ($\overline{OE}$) to be set High to place the output into the high impedance state.

The device input is compatible with TTL–type input thresholds and the output has a full 5V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic–level translator from 3.0V CMOS logic to 5.0V CMOS Logic or from 1.8V CMOS logic to 3.0V CMOS Logic while operating at the high–voltage power supply.

The MC74VHC1GT125 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1GT125 to be used to interface 5V circuits to 3V circuits. The output structures also provide protection when V_{CC} = 0V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: t_{PD} = 3.5ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- CMOS–Compatible Outputs: $V_{OH} > 0.8V_{CC}$; $V_{OL} < 0.1V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 1500V; MM > 200V

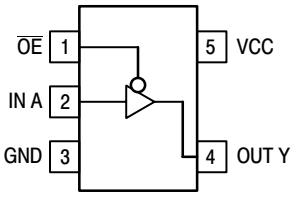

Figure 1. 5–Lead SOT–353 Pinout (Top View)

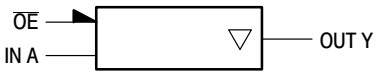

Figure 2. Logic Symbol

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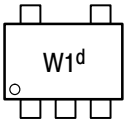
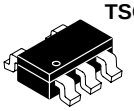
MARKING DIAGRAMS

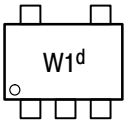
SC–88A / SOT–353/SC–70
DF SUFFIX
CASE 419A



Pin 1
d = Date Code



TSOP–5/SOT–23/SC–59
DT SUFFIX
CASE 483



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	$\overline{OE}$
2	IN A
3	GND
4	OUT Y
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

FUNCTION TABLE

A Input	$\overline{OE}$ Input	Y Output
L	L	L
H	L	H
X	H	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	3.0	5.5	V
DC Input Voltage	V_{in}	0	5.5	V
DC Output Voltage	V_{out}	0	V_{CC}	V
Operating Temperature, All Package Types	T_A	– 55	+ 125	°C
Input Rise and Fall Time V_{CC} =5.0V ±0.5V	t_r, t_f	0	20	ns/V

The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

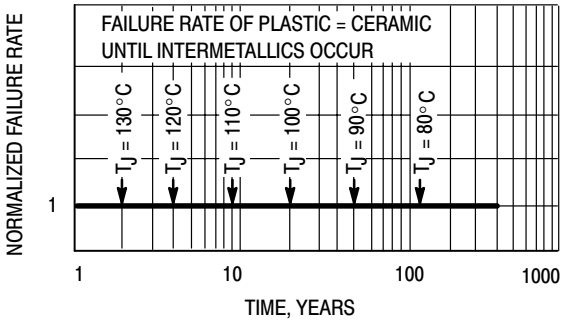


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			$T_A \le 85°C$		$T_A \le 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: V_{IN} = 3.4V	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = – 40 to 85°C		$T_A \le 125°C$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y (Figures 3. and 5.)	V_{CC} = 3.3 ± 0.3V C_L = 15pF C_L = 50pF		5.6 8.1	8.0 11.5	1.0 1.0	9.5 13.0		12.0 16.0	ns
		V_{CC} = 5.0 ± 0.5V C_L = 15pF C_L = 50pF		3.8 5.3	5.5 7.5	1.0 1.0	6.5 8.5		8.5 10.5	
t_{PZL}, t_{PZH}	Maximum Output Enable TIme, $\overline{OE}$ to Y (Figures 4. and 5.)	V_{CC} = 3.3 ± 0.3V C_L = 15pF R_L = 1kΩ C_L = 50pF		5.4 7.9	8.0 11.5	1.0 1.0	9.5 13.0		11.5 15.0	ns
		V_{CC} = 5.0 ± 0.5V C_L = 15pF R_L = 1kΩ C_L = 50pF		3.6 5.1	5.1 7.1	1.0 1.0	6.0 8.0		7.5 9.5	
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time, $\overline{OE}$ to Y (Figures 4. and 5.)	V_{CC} = 3.3 ± 0.3V C_L = 15pF R_L = 1kΩ C_L = 50pF		6.5 8.0	9.7 13.2	1.0 1.0	11.5 15.0		14.5 18.0	ns
		V_{CC} = 5.0 ± 0.5V C_L = 15pF R_L = 1kΩ C_L = 50pF		4.8 7.0	6.8 8.8	1.0 1.0	8.0 10.0		10.0 12.0	
C_{in}	Maximum Input Capacitance			4	10		10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High Impedance State)			6						pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	14	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per buffer). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

SWITCHING WAVEFORMS

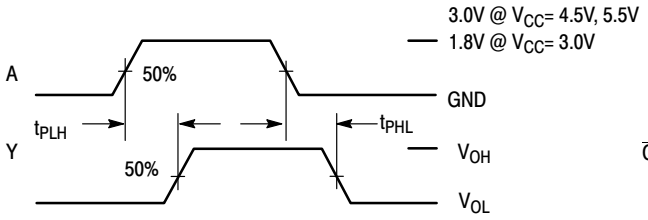


Figure 4.

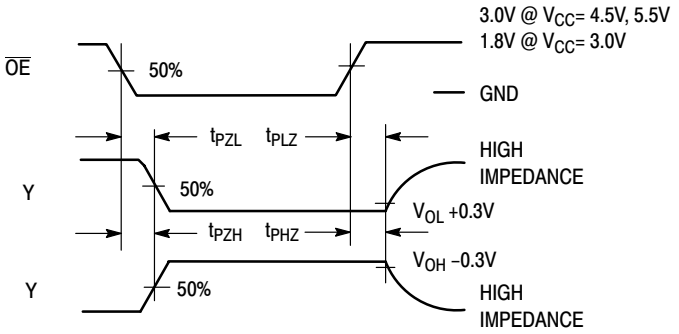
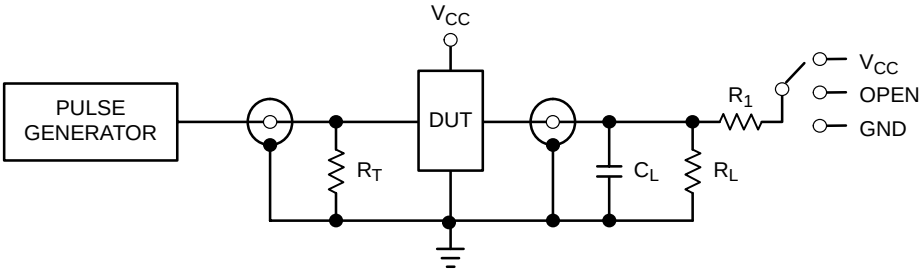


Figure 5.



TEST	SWITCH
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND
t_{PLH}, t_{PHL}	OPEN

C_L = 50 pF equivalent (Includes jig and probe capacitance) or 15 pF
R_L = R_1 = 500 Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 6. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technol-ogy	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GT125DFT2	MC	74	VHC1G	T125	DF	T2	SC–88A/ SOT–353 /SC–70	178mm (7”) 3000 Unit
MC74VHC1GT125DFT4	MC	74	VHC1G	T125	DF	T4	SC–88A/ SOT–353 /SC–70	330mm (13”) 100000 Unit
MC74VHC1GT125DTT1	MC	74	VHC1G	T125	DT	T1	TSOP5/ SOT–23 /SC–59	178mm (7”) 3000 Unit
MC74VHC1GT125DT3	MC	74	VHC1G	T125	DT	T3	TSOP5/ SOT–23 /SC–59	330mm (13”) 100000 Unit

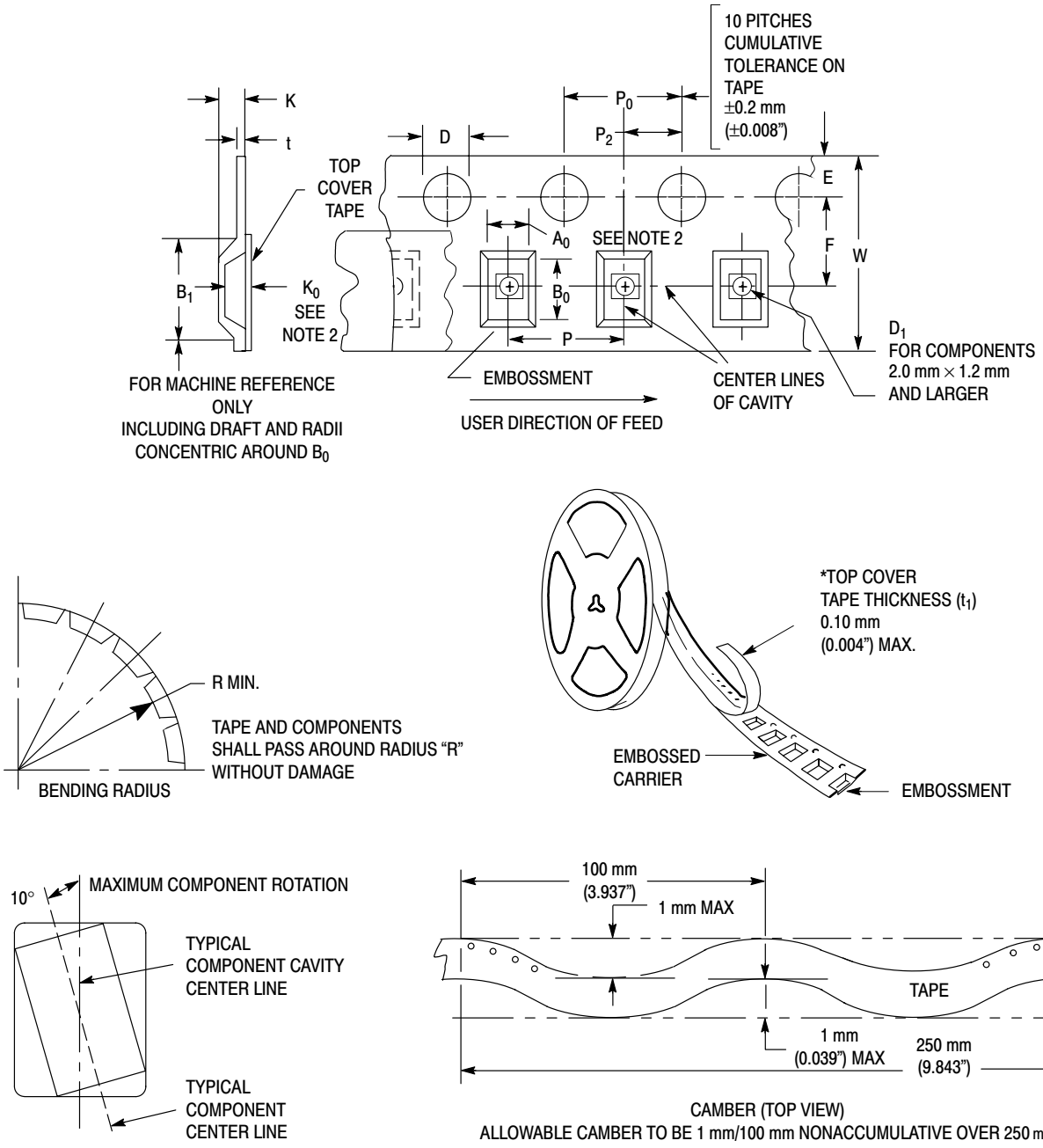


Figure 7. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 1 and 2)

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R	T	W
8 mm	4.35 mm (0.171")	1.5 +0.1/ −0.0 mm (0.059 +0.004/ −0.0")	1.0 mm Min (0.039")	1.75 ±0.1 mm (0.069 ±0.004")	3.5 ±0.5 mm (1.38 ±0.002")	2.4 mm (0.094")	4.0 ±0.10 mm (0.157 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.1 mm (0.079 ±0.002")	25 mm (0.98")	0.3 ±0.05 mm (0.01 +0.0038/ −0.0002")	8.0 ±0.3 mm (0.315 ±0.012")

1. Metric Dimensions Govern–English are in parentheses for reference only.
2. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

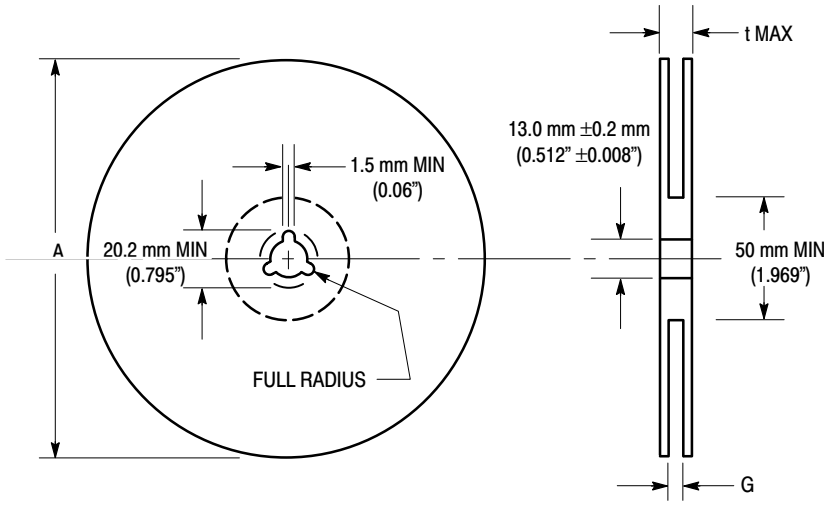


Figure 8. Reel Dimensions

REEL DIMENSIONS

Tape Size	T&R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7")	8.4 mm, +1.5 mm, −0.0 (0.33" + 0.059", −0.00)	14.4 mm (0.56")
8 mm	T3, T4	330 mm (13")	8.4 mm, +1.5 mm, −0.0 (0.33" + 0.059", −0.00)	14.4 mm (0.56")

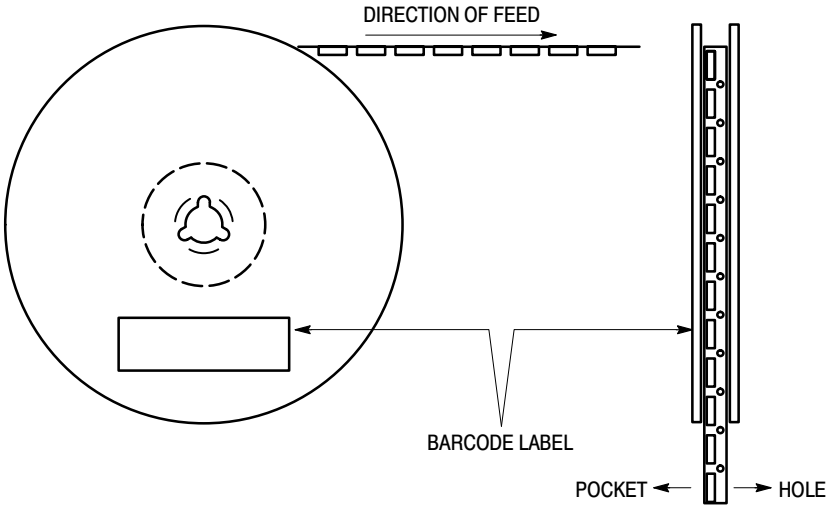


Figure 9. Reel Winding Direction

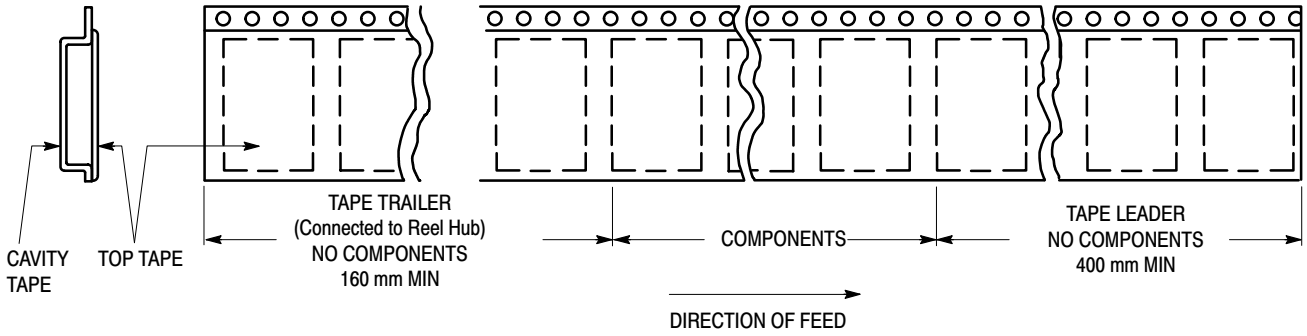


Figure 10. Tape Ends for Finished Goods

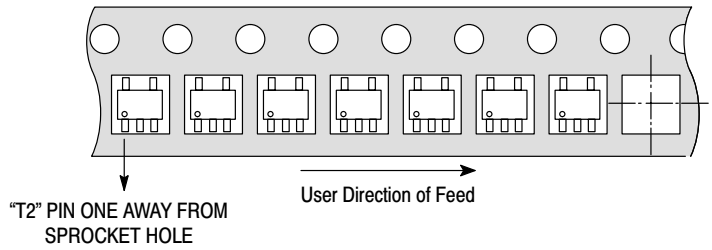


Figure 11. DFT2 and DFT4 (SC88A) Reel Configuration/Orientation

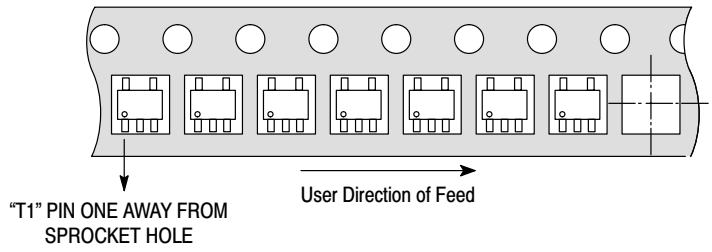
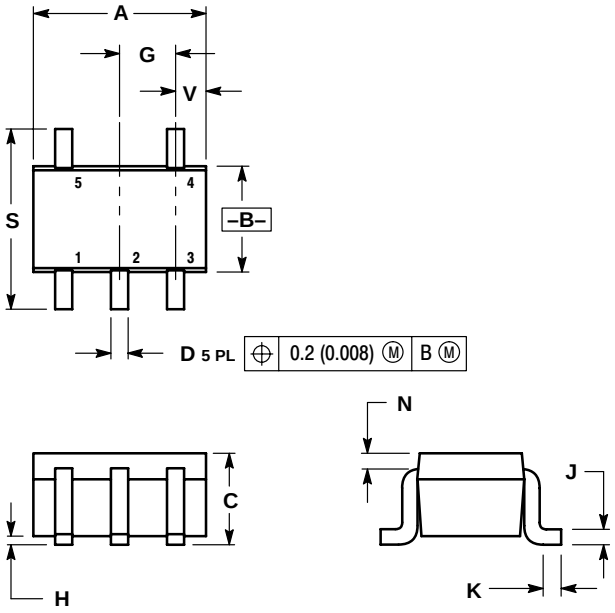


Figure 12. DTT1 and DTT3 (TSOP5) Reel Configuration/Orientation

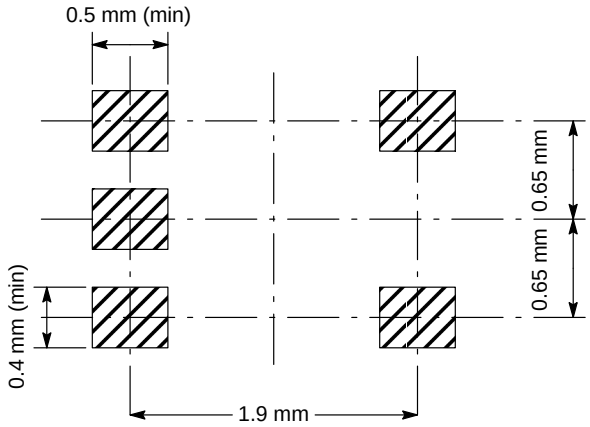
PACKAGE DIMENSIONS

SC–88A / SOT–353 / SC–70
DF SUFFIX
5–LEAD PACKAGE
CASE 419A–01
ISSUE B



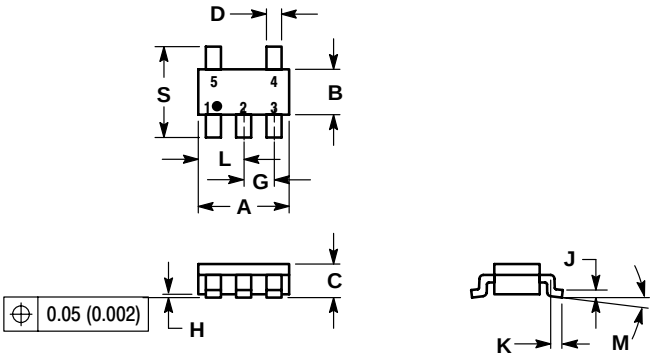
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40



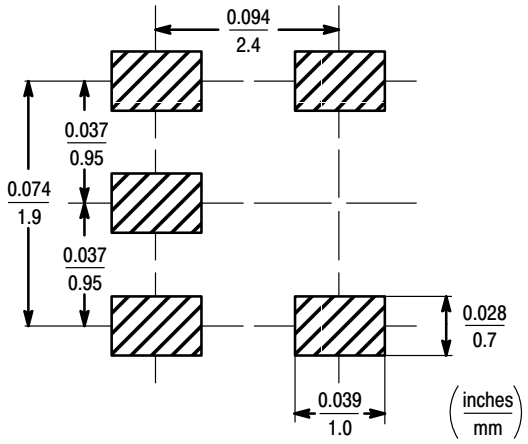
PACKAGE DIMENSIONS

TSOP–5 / SOT–23 / SC–59
DT SUFFIX
5–LEAD PACKAGE
CASE 483–01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.00	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181



Notes

Notes

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