MC74VHC1G135

2-Input NAND Schmitt-Trigger with Open Drain Output

The MC74VHC1G135 is a single gate CMOS Schmitt NAND trigger with an open drain output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including an open drain output which provides the capability to set the output switching level. This allows the MC74VHC1G135 to be used to interface 5V circuits to circuits of any voltage between V_{CC} and 7V using an external resistor and power supply.

The MC74VHC1G135 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage.

The MC74VHC1G135 can be used to enhance noise immunity or to square up slowly changing waveforms.

- High Speed: t_{PD} = 4.9ns (Typ) at V_{CC} = 5V
- Low Internal Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V

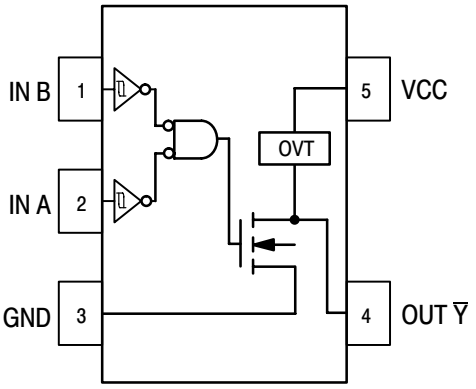


Figure 1. 5–Lead SOT–353 Pinout (Top View)

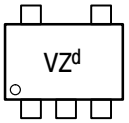
Figure 2. Logic Symbol

ON Semiconductor

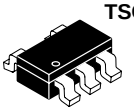
http://onsemi.com

MARKING DIAGRAMS

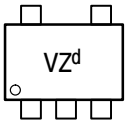
SC–88A / SOT–353/SC–70
DF SUFFIX
CASE 419A



Pin 1
d = Date Code



TSOP–5/SOT–23/SC–59
DT SUFFIX
CASE 483



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT $\overline{Y}$
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	**B**	**$\overline{Y}$**
L	L	Z
L	H	Z
H	L	Z
H	H	L

MAXIMUM RATINGS*

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	–0.5 to +7.0	V
DC Input Voltage	V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{OUT}	–0.5 to 7.0	V
Input Diode Current	I_{IK}	–20	mA
Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin	I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND	I_{CC}	+50	mA
Power dissipation in still air, SC–88A †	P_D	200	mW
Lead temperature, 1 mm from case for 10 s	T_L	260	°C
Storage temperature	T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	2.0	5.5	V
DC Input Voltage	V_{IN}	0.0	5.5	V
DC Output Voltage	V_{OUT}	0.0	7.0	V
Operating Temperature Range	T_A	–55	+125	°C

The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

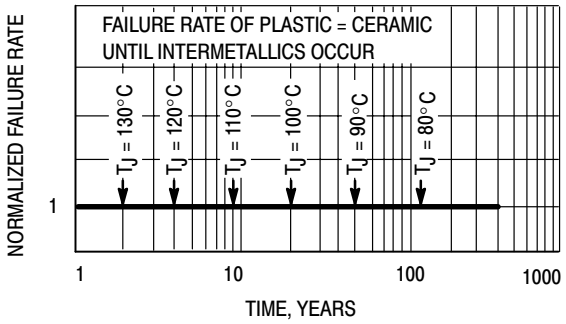


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{T+}	Positive Threshold Voltage		3.0 4.5 5.5	1.50 2.35 2.80	1.88 2.66 3.21	2.25 3.10 3.70	1.50 2.35 2.80	2.25 3.10 3.70	1.50 2.35 2.80	2.25 3.10 3.70	V
V_{T-}	Negative Threshold Voltage		3.0 4.5 5.5	0.65 1.10 1.45	1.03 1.62 2.02	1.40 2.10 2.60	0.65 1.10 1.45	1.40 2.10 2.60	0.65 1.10 1.45	1.40 2.10 2.60	V
V_H	Hysteresis Voltage		3.0 4.5 5.5	0.30 0.40 0.50	0.85 1.05 1.20	1.60 2.00 2.25	0.30 0.40 0.50	1.60 2.00 2.25	0.30 0.40 0.50	1.60 2.00 2.25	V
V_{OH}	Minimum High–Level Output Voltage I_{OH} = –50μA	V_{IN} = V_{IH} or V_{IL} I_{OH} = –50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		I_{OH} = –4mA I_{OH} = –8mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			2.0		20		40	μA
I_{OPD}	Maximum Off–state Leakage Current	V_{OUT} = 5.5V	0			0.25		2.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r/t_f = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PZL}	Maximum Output Enable Time, A or B to $\overline{Y}$	V_{CC} = 3.3 ± 0.3V, C_L = 15 pF R_L = 1KΩ, C_L = 50 pF		7.6 10.1	11.9 15.4	1.0 1.0	14.0 17.5	1.0 1.0	16.1 19.6	ns
		V_{CC} = 5.0 ± 0.5V, C_L = 15 pF R_L = 1KΩ, C_L = 50 pF		4.9 6.4	7.7 9.7	1.0 1.0	9.0 11.0	1.0 1.0	10.3 12.3	ns
t_{PLZ}	Maximum Output Disable Time	V_{CC} = 3.0 ± 0.3V, R_L = 1KΩ, C_L = 50 pF		10.1	15.4		17.5		19.6	ns
		V_{CC} = 5.0 ± 0.5V, R_L = 1KΩ, C_L = 50 pF		6.4	9.7		11.0		12.3	ns
C_{IN}	Maximum Input Capacitance			5.0	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	16	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

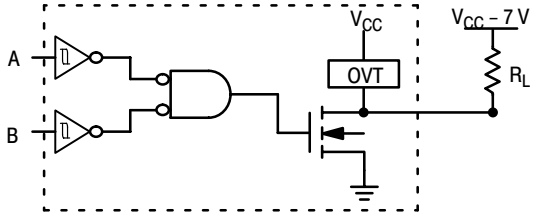


Figure 4. Output Voltage Mismatch Application

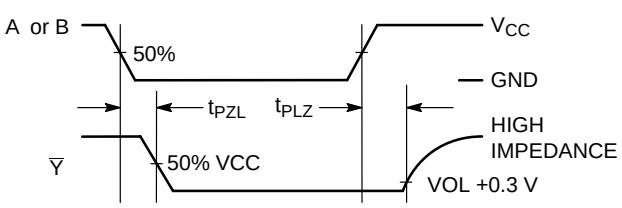
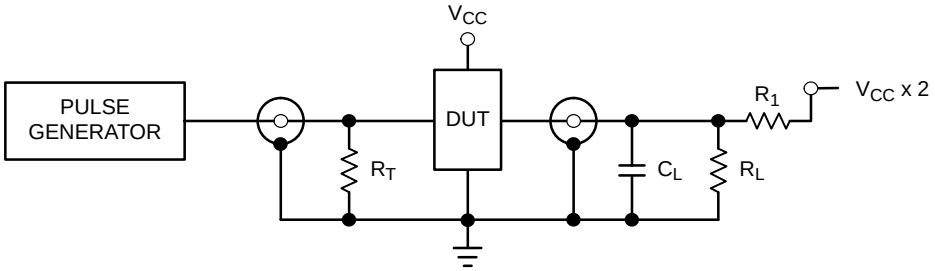


Figure 5. Switching Waveforms



C_L = 50 pF equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500 Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

Figure 6. Test Circuit

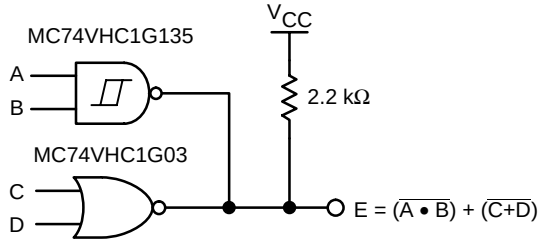


Figure 7. Complex Boolean Functions

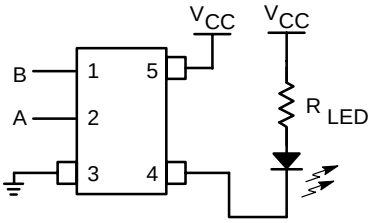


Figure 8. LED Driver

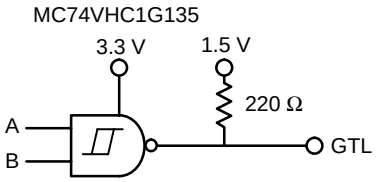


Figure 9. GTL Driver

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type (Name/SOT#/ Common Name)	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G135DFT2	MC	74	VHC1G	135	DF	T2	SC–88A / SOT–353 / SC–70	178 mm (7”) 3000 Unit
MC74VHC1G135DFT4	MC	74	VHC1G	135	DF	T4	SC–88A / SOT–353 / SC–70	330 mm (13”) 10000 Unit
MC74VHC1G135DTT1	MC	74	VHC1G	135	DT	T1	TSOPS / SOT–23 / SC–59	178 mm (7”) 3000 Unit
MC74VHC1G135DTT3	MC	74	VHC1G	135	DT	T3	TSOPS / SOT–23 / SC–59	330 mm (13”) 10000 Unit

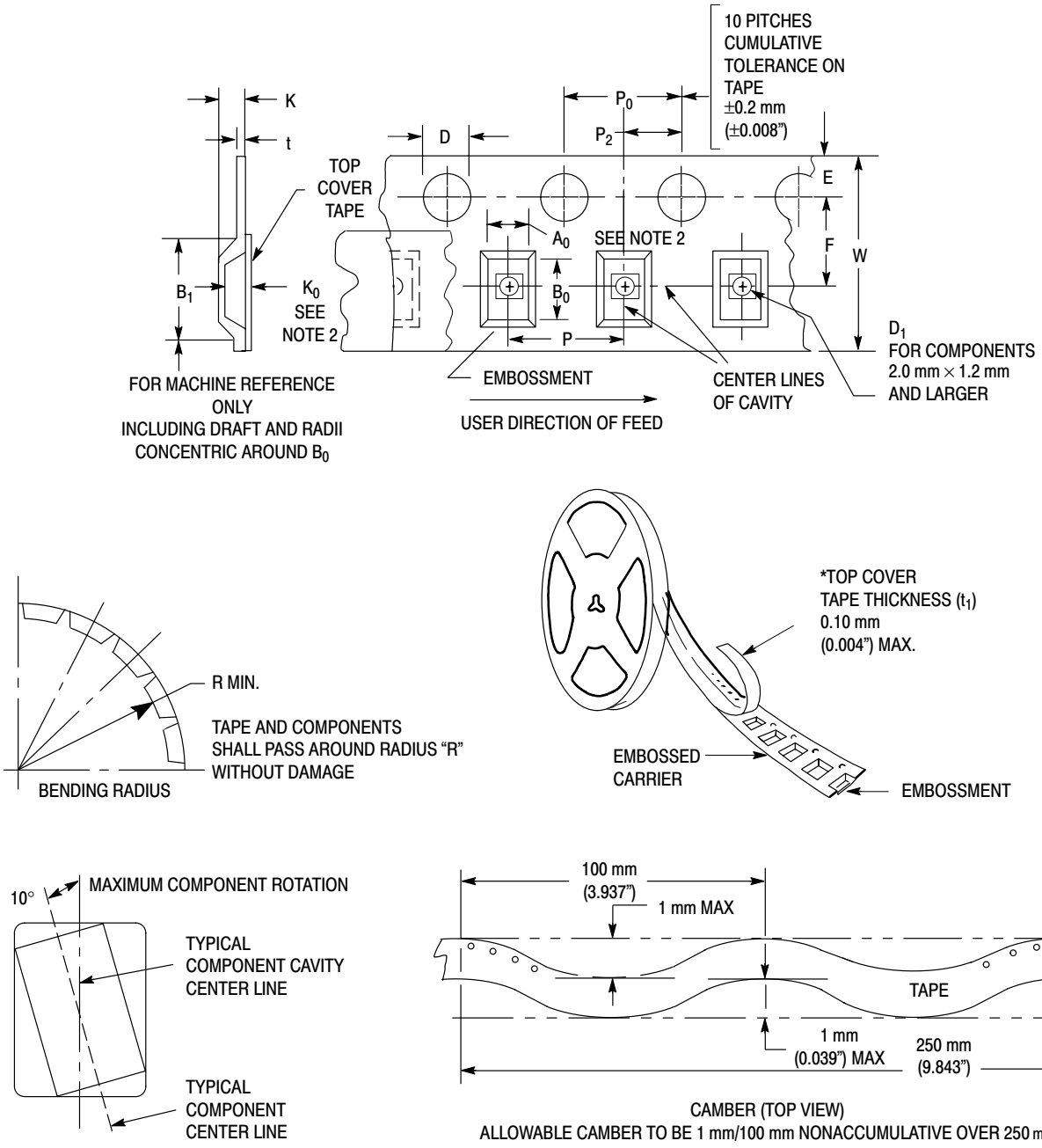


Figure 10. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 1 and 2)

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R	T	W
8 mm	4.35 mm (0.171")	1.5 +0.1/ −0.0 mm (0.059 +0.004/ −0.0")	1.0 mm Min (0.039")	1.75 ±0.1 mm (0.069 ±0.004")	3.5 ±0.5 mm (1.38 ±0.002")	2.4 mm (0.094")	4.0 ±0.10 mm (0.157 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.1 mm (0.079 ±0.002")	25 mm (0.98")	0.3 ±0.05 mm (0.01 +0.0038/ −0.0002")	8.0 ±0.3 mm (0.315 ±0.012")

1. Metric Dimensions Govern–English are in parentheses for reference only.
2. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

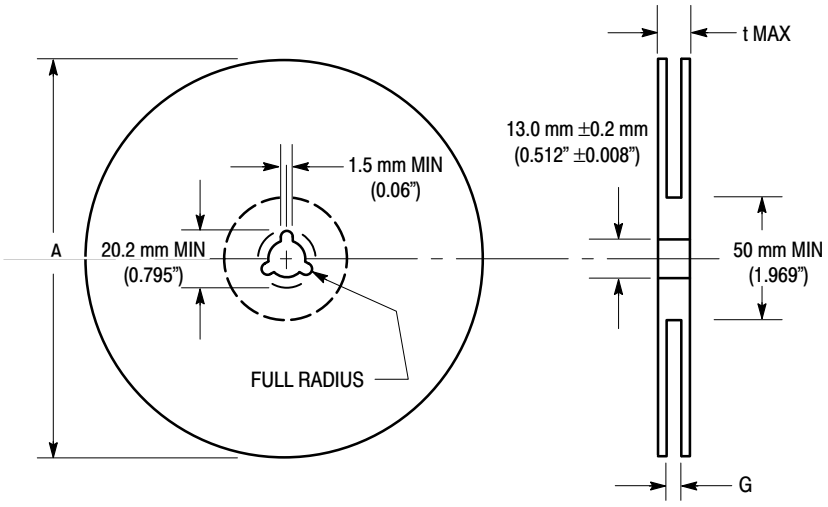


Figure 11. Reel Dimensions

REEL DIMENSIONS

Tape Size	T&R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7")	8.4 mm, +1.5 mm, −0.0 (0.33" + 0.059", −0.00)	14.4 mm (0.56")
8 mm	T3, T4	330 mm (13")	8.4 mm, +1.5 mm, −0.0 (0.33" + 0.059", −0.00)	14.4 mm (0.56")

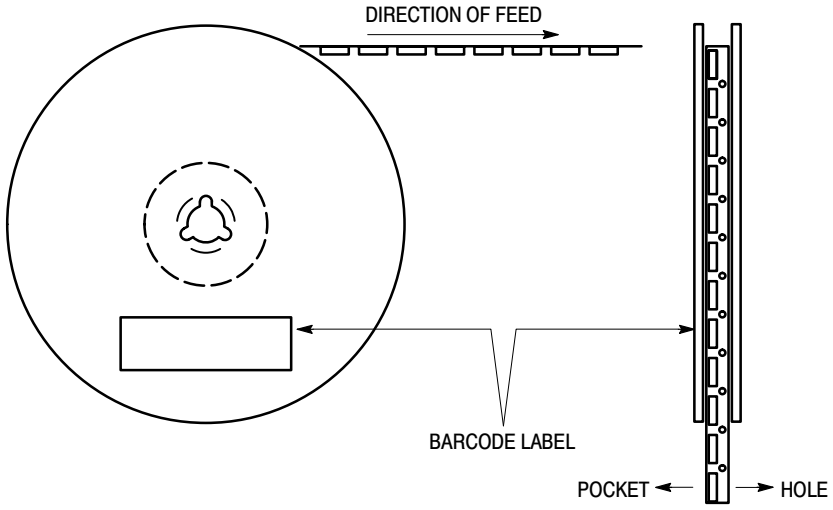


Figure 12. Reel Winding Direction

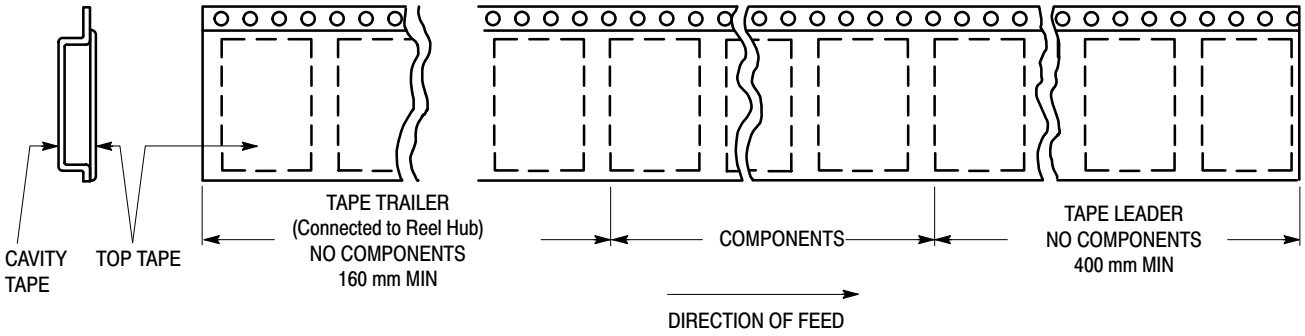


Figure 13. Tape Ends for Finished Goods

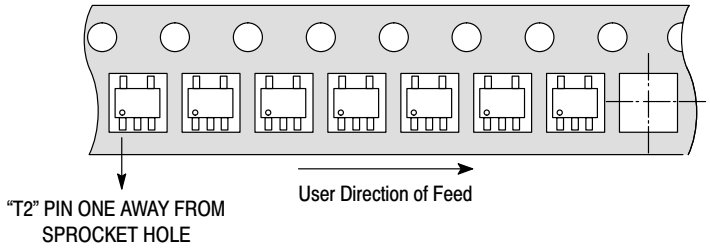


Figure 14. DFT2 and DFT4 (SC88A) Reel Configuration/Orientation

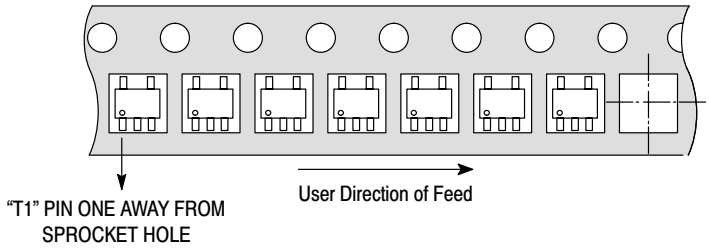
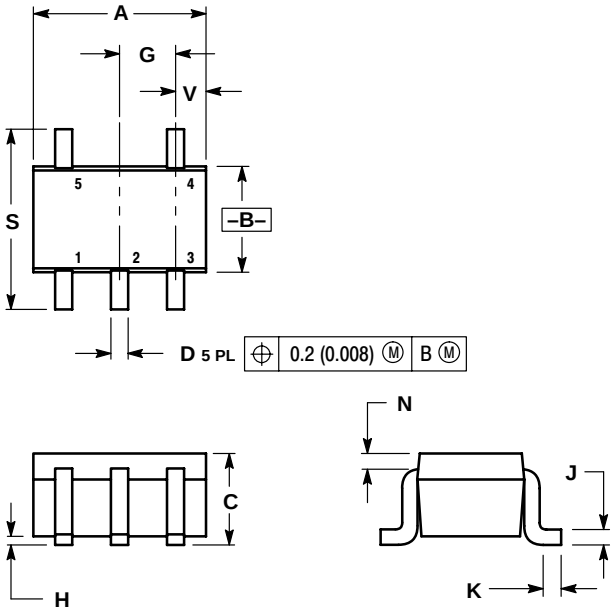


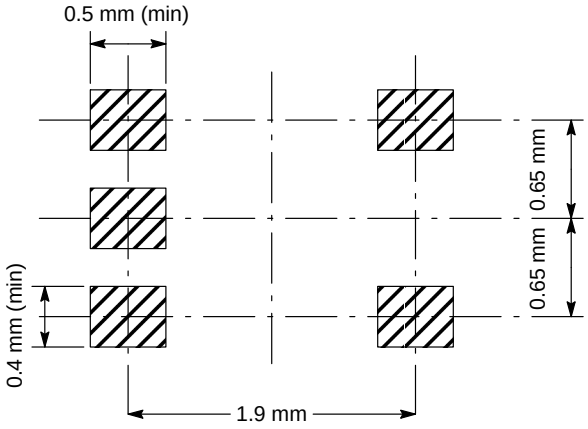
Figure 15. DTT1 and DTT3 (TSOP5) Reel Configuration/Orientation

SC–88A / SOT–353 / SC–70
DF SUFFIX
5–LEAD PACKAGE
CASE 419A–01
ISSUE B

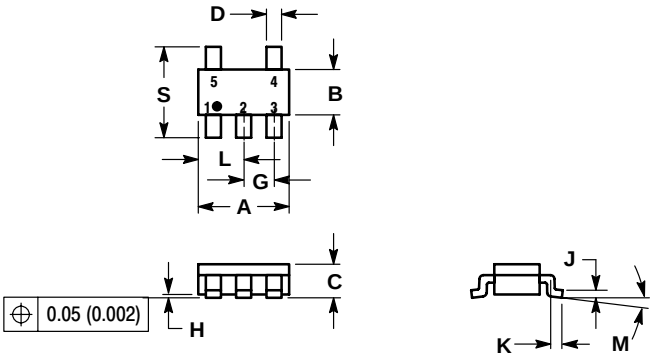


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

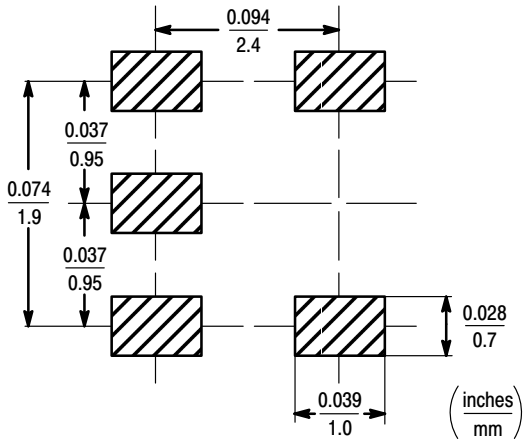


TSOP–5 / SOT–23 / SC–59
DT SUFFIX
5–LEAD PACKAGE
CASE 483–01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.00	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181



Notes

Notes

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